BENJAMIN HERSHBERG

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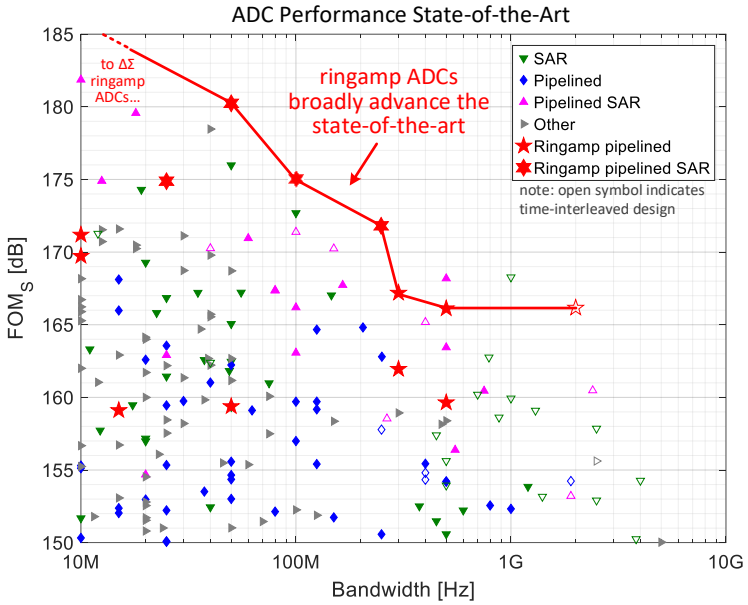
SUMMARY OF QUALIFICATIONS

- **Analog, Mixed-Signal, RF:** Specialty in ADCs with experience also in frequency synthesis and tunable RF frontends.
- **AI, Machine Learning:** Focus on algorithms and theory to bridge the CS / EE gap, offer unique cross-domain insight.
- **Execution & Delivery:** Attention to detail + Risk management = Perfect first-turn success rate on 15 fabricated designs.
- **Innovation Expertise:** Can connect the full innovation stack: understanding which problem to solve, bringing out the best ideas in others, identifying unconventional ideas and approaches, securing stakeholder buy-in and resources, leading the design team to successful implementation, test & validation, report-out, and refining to industrial maturity.
- **Strategic Risk Taker:** Initiated and led a long-term strategic research program that advanced ADC state-of-the-art by an order-of-magnitude. Proven track record of recognizing disruptive opportunities and orthogonal thinking.

INNOVATION ACHIEVEMENT: RING AMPLIFIERS

- Invented the "ringamp", a general block-level solution to a longstanding amplifier scaling problem.
- Idea arose during PhD; contributed another 10 years of strategic leadership on the topic to bring it to a point where the topic is now self-sustaining.
- Broadly advances the ADC state-of-the-art by up to an order-of-magnitude; enables new circuit applications and diversifies the design landscape.
- Worked closely with businesses to successfully integrate ringamp tech. into commercial products.
- Active topic with avg. 5 ringamp papers per year at ISSCC. Rapidly expanding into new areas: PLL, LDO, ΔΣ, NS-SAR, and new applications: cryo., high-volt.
- To learn more, see tutorial at: youtu.be/uPFCcgjS5Zk



EXPERIENCE

2023 - current **Analog Engineer at Intel** ***Hillsboro, OR, USA***

- Innovating solutions for next generation 448Gbps SerDes in angstrom-scale CMOS process technologies.

2022 - 2022 **Principal Engineer at Infinera** ***San Jose, California, USA***

- Contributed to the design of ADCs, DACs, and PLLs in 5nm CMOS for optical transceivers operating in the tens to hundreds of giga-samples. Strong exposure to product design principles and practices.

2022 - 2022 **Advisory Board Member at Ai Linear** ***San Jose, California, USA***

- Architecture definition, pathfinding, and circuit design at startup with focus on TinyML edge devices.

2021 - current **Machine Learning and AI** ***Portland, OR, USA***

- Conducting research while tracking key contemporary papers and results, especially in NLP and Computer Vision.
- Completed broad set of certified courses in DL and RL, supplemented with self-study and side projects. Experience with JAX, PyTorch, TensorFlow. Implemented a NN framework in Python from first principles for practice.

2013 – 2021 **Principal Scientist at imec** ***Leuven, Belgium***

- 2016-2021: Chief architect and chip lead for ringamp high-speed ADC program overseeing all aspects of design & test.

- Strategic roadmap for parallelized innovation: (1) core blocks, (2) architectures & circuits, (3) industrialization.
- Resulted in several key design wins and contracts, most profitable group in the division, doubled technical staff.
- Worked closely with clients to transfer technology to production.
- Outstanding output: 6 patents, 2x ISSCC (+best paper award), 3x VLSI, 6x JSSC, 1x TCAS, 2x CICC.
- Established multiple state-of-the-art breakthroughs: order-of-magnitude improvement in direct-RF ADC, best FoM of any ADC above 200MS/s, first ringamp to 1GS/s, first DT-ΔΣ to compete with wideband CT-ΔΣ.

▫ 2015-2016: design of pipe-SAR ADC with integrated reference stabilization in 16nm CMOS.

▫ 2013-2015: Tunable RF frontends for FDD. First >70dB IIP3 CMOS EBD, first true dual-frequency balance network.

▫ 2013: Wideband VCO for SDR. Successfully debugged and fixed architecture that had eluded the previous designers.

▫ Extensive design experience in 16nm FinFET, 28nm planar, and 180nm RF SOI.

▫ Wrote advanced software tool to enable best-practices for design and test. Open-sourced to IC design community.

▫ Mentored several PhD and Master students.

▫ More details about projects at: benjamin.hershberg.com/projects

2006 – 2012 **Graduate Student at Oregon State University** ***Corvallis, Oregon, USA***

▫ PhD research focused on scalable amplification solutions for switched capacitor circuits. Advisor: Dr. Un-Ku Moon.

▫ Invented ring amplification, split-CLS, and other notable ideas. First author on 2x ISSCC, 2x JSSC, 1x VLSI, as student.

▫ Designed & tested four successful prototype pipelined ADCs, described at benjamin.hershberg.com/projects.

▫ Internship at AKM in Atsugi, Japan developing novel SAR ADC techniques.

2003 – 2012 **Founder at Eradium Design** ***Corvallis, Oregon, USA***

▫ Funded college education by founding web development company with 3 employees.

▫ Excellent programming and software engineering skills. Python, Java, C, PHP, HMTL, CSS, SQL

▫ Experience with enterprise customers. Major clients: DAMA International, IEEE Magnetics Society.

PUBLICATIONS & PATENTS

53	10	14	11	1
conference papers, journal articles, and book chapters	patents issued or pending	top rank conference papers: ISSCC and VLSI (9 as first author)	top rank journal articles: JSSC (4 as first author)	ISSCC best paper award (top rank conference)

▫ Full list of downloadable papers at: benjamin.hershberg.com/publications

▫ Stats from Google Scholar page: citations: 1492, h-index: 22, i10-index: 28

▫ Peer reviewer for: JSSC, TCAS, ISSCC, VLSI, E. Letters, TVLSI

▫ Selected Publications:

- A 4-GS/s 10-ENOB 75-mW Ringamp ADC in 16-nm CMOS With Background Monitoring of Distortion
  JSSC, Aug. 2021. [pdf link]
- Ring Amplifiers for Switched Capacitor Circuits
  JSSC, Dec. 2012. [pdf link]

AWARDS AND HONORS

▫ ISSCC 2020 Invited Lecturer

▫ CICC 2020 Invited Lecturer

▫ AACD 2014 Invited Lecturer

▫ Prestigious ISSCC 2019 “best paper” award (first-author, #1 ranked conference)

▫ Analog Devices 2010 Student Design Award

▫ Broadcom 2012 University Research Competition (2nd place)

EDUCATION

PhD	Electrical Engineering	2012
BS Honors	Electrical Engineering	2006
BS Honors	Computer Engineering	2006
Minor	Computer Science	2006

All degrees granted by
Oregon State University, Corvallis, USA