Asynchronous CLS for Zero Crossing based Circuits

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***Abstract* — This paper introduces Asynchronous correlated level shifting (ACLS) for Zero Crossing based Circuits. ACLS technique for Zero crossing based circuits provides rail-to-rail, asynchronous operation for the estimation and level shifting phase. The current source non-linearity is reduced and the power supply rejection ratio is improved.**

***Index Terms*—ACLS, ZCBC, Rail-to-Rail operation**

I. Introduction

THIS paper introduces Asynchronous Correlated Level Shifting technique (ACLS) for Zero Crossing Based Circuits. The Correlated level shifting (CLS) technique provides rail-to-rail operation in Opamp based circuits and approximately squares the loop-gain as shown in [1]. The Zero-crossing based circuits (ZCBC) suffer from signal dependent variation of the current source and overshoot due to the comparator delays as shown in [2]. ACLS reduces the signal dependent variation of the current source by shifting the current source to a region with more headroom. The increased headroom for the current source can be optimized to provide highly linear current sources with large output impedances. This translates to a large loop-gain in ZCBC and a linear ramp source. This technique is useful in the deep sub-micron technologies, where the voltage headroom for current source is small. Sections II briefly describe CLS technique for opamp. Section III describes ZCBC circuits and enumerates the advantages of ACLS as compared to ZCBC circuits. Section V and VI provide simulation results and conclusion. The derivation for the approximated output voltage and the level-shifted output voltage are provided in the appendix.

II. Correlated Level Shifting (CLS)

CLS for opamp is implemented as shown in the figure 1. Detailed discussion can be found in [1]. The opamp based CLS technique operates in three phases. The input is sampled in Φ_1. The estimated output is generated at the end of Φ_{CLS}. The Level shifted output is generated at the end of Φ_2. The output of the opamp is shifted to the output common mode. This improves opamp linearity and the virtual ground at the input of the opamp.

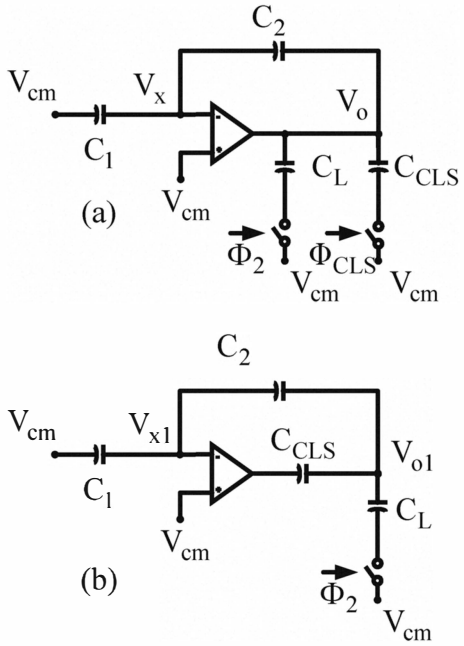

Figure 1 Opamp based CLS, (a) Estimation Phase and (b) Level Shift Phase

III. Asynchronous Correlated Level Shifting

One of the power consuming blocks in a pipelined ADC is opamp. In deep sub-micron technologies, the reduced supply voltage imposes stringent requirements for opamp design. By using a continuous time comparator which can detect the zero-crossing of the virtual node, the zero crossing circuits can be made power efficient, [2,3]. However, the zero crossing circuits suffer from several non-idealities. One of them is the signal dependent variation of the current source.

Asynchronous CLS allows rail-to-rail swing at the output and relaxes current source design requirements as compared to a conventional ZCBC circuits. The opamp based CLS requires three phase clock. However, the ACLS does not need a three phase

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clock. The signals P, E_1, E_2, E_{CLS} are generated asynchronously from the comparator output.

The correlated level shifting for zero crossing based circuits is described as follows. The input is sampled in Φ_1.

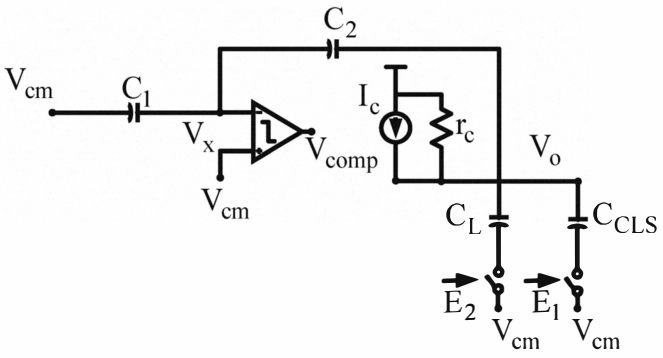

Figure 2: Estimation Phase

Figure 2 shows the estimation phase (E_1). At the end of estimation phase, the output voltage can be approximated by (2).

$$V_o \approx \frac{V_{in}C_1}{C_2}\frac{1}{\left(1+\frac{t_{d1}}{r_c(V_o)C_{eff1}}\right)} + \frac{I_c(V_o)\,t_{d1}}{C_{eff1}} \quad - (2)$$

$$C_{eff1} = C_{CLS} + C_L + \frac{C_1C_2}{C_1+C_2} \quad - (3)$$

Where V_o is the output voltage, r_c is the output resistance of the coarse current source, I_c. C_{eff1} is the effective load capacitance seen by the current source, I_c. t_{d1} is the time delay of the comparator at the end of estimation phase. In deep sub-micron technologies, the channel-length modulation causes variation in the current source value and its resistance. This causes non-linearity in (2). The derivation of (2) is presented in the appendix.

Figure 3 shows the level shift phase, where the fine current source is level shifted towards common-mode voltage. At the end of Level Shifting phase, the output voltage can be approximated by (4).

$$V_{o1} \approx \frac{V_{in}C_1}{C_2}\left(1 - \frac{t_{d2}}{r_fC_{eff2}}\frac{t_{d1}}{r_cC_{eff2}}\right) - \alpha\frac{I_f t_{d2}}{C_{eff2}} + \frac{I_c t_{d1} t_{d2}}{r_f C_{eff1} C_{eff2}} \quad - (4)$$

Where,

$$\alpha = \frac{C_{CLS}+C_{eff3}}{C_{CLS}},\ C_{eff3} = C_L + \frac{C_1C_2}{C_1+C_2},\ C_{eff2} = \frac{C_{eff3}C_{CLS}}{C_{CLS}+C_{eff3}}$$

t_{d2}, r_f, I_f are the corresponding terms for the level shifting phase. The derivation of (4) is presented in the appendix. However, the signal dependency of the output resistance is reduced by an order of magnitude.

A. Loop gain and Overshoot

The important difference between the opamp based CLS and the comparator based CLS can be identified from the loop gain in the level shifting phase.

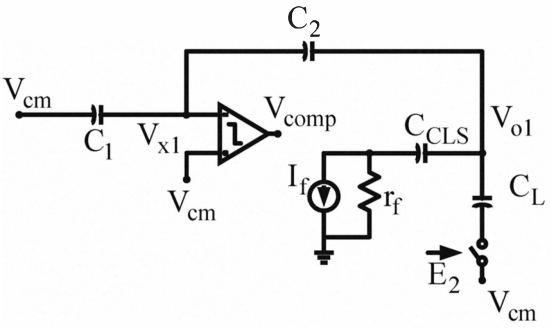

Figure 3: Level Shift Phase

According to [1], the opamp based CLS approximately squares the loop gain at the end of level shifting phase. A similar expression for ZCBC is also obtained as shown in equation (4).

Table 1 Loop Gain Comparison

Phase	Opamp Loop Gain	ZCBC Loop Gain
Estimation	$A\frac{C_2}{C_1+C_2}$	$\frac{r_cC_{eff1}}{t_{d1}}$
Level Shifting	$\approx\left(A\frac{C_2}{C_1+C_2}\right)^2$	$\frac{r_fC_{eff2}}{t_{d2}}\frac{r_cC_{eff1}}{t_{d1}}$

The fine current source begins the level-shifting phase with fixed voltage headroom. Thus, the current source can be cascoded to provide large loop gain and the linearity is improved by an order of magnitude.

The overshoot caused due comparator delay is given by the second term in (2) and (4). Thanks to ACLS, the variation of the fine current source is reduced by an order of magnitude. Thus, the overshoot is largely signal independent. The choice of CLS capacitor is the trade-off between loop-gain enhancement, linearity obtained and speed.

B. Power Supply Rejection

The power supply rejection ratio (PSRR) is an important issue due to the mismatch between two current sources in a differential circuit implementation of ZCBC. Figure 4 represents the small signal models for the conventional ZCBC and ACLS based ZCBC. The ACLS based ZCBC provides more attenuation as compared to the conventional ZCBC circuits. However, reducing the CLS capacitor will increase the swing seen by the fine current source. Figure 5, shows a comparison of PSRR between conventional ZCBC and ACLS based circuits.

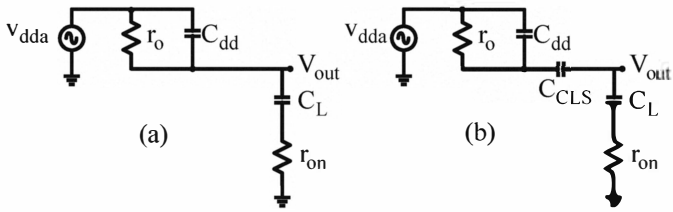

Figure 4 PSRR Model, (a) Conventional ZCBC, (b) ACLS ZCBC

The PSRR for the conventional ZCBC and ACLS ZCBC is given by equations (5) and (6) respectively. The ACLS ZCBC provides better PSRR and allows an independent control of the PSRR shape through CLS capacitor.

$$\frac{v_o}{v_{dda}} \approx \frac{(1+sC_L r_{on})(1+sC_{dd} r_o)}{(1+sC_{dd} r_{on})(1+sC_L r_o)} \quad - \quad (5)$$

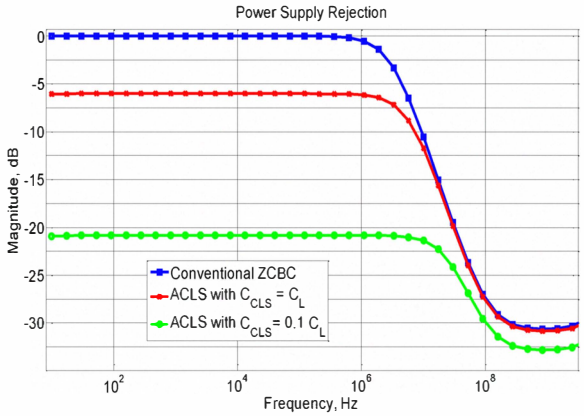

Figure 5 PSSR, Conventional, ACLS with CLS=CL, ACLS with CLS=0.1CL

The PSRR for the ACLS based ZCBC can be approximated as follows,

$$\frac{v_o}{v_{dda}} \approx \frac{C_{CLS}}{C_{CLS}+C_L} \frac{(1+sr_o C_{dd})}{(1+s/p_1)(1+s/p_2)} \quad - \quad (6)$$

Where, $p_1 = -\frac{1}{r_{on} C_L}$, $p_2 = -\frac{(C_{CLS}+C_L)}{r_o C_{CLS} C_L}$

The CLS capacitor can be optimized with respect to linearity, PSRR and level-shifting period. However, improving PSRR comes at the cost of increasing the swing requirement for the fine current source and reduced linearity.

IV. Simulation Results

Conventional ZCBC and ACLS circuit were simulated in an S/H configuration. The clock frequency was chosen to be 20 MHz. The comparator bandwidth was chosen to be 2-5 times larger than the clock frequency. The current source was implemented as a single MOSFET transistor. The CLS capacitor (C_{CLS}) was chosen to be the same as the load capacitor (C_L).

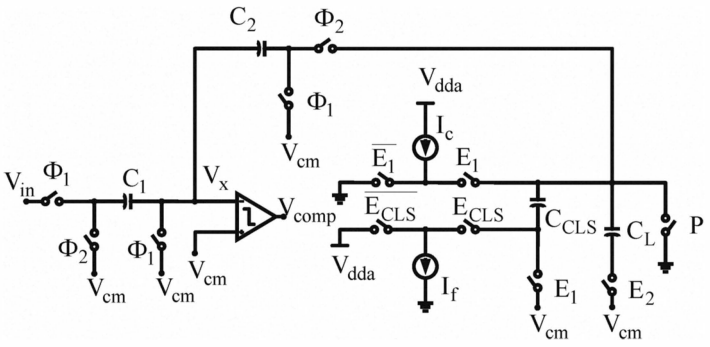

Figure 6 S/H Configuration of ACLS

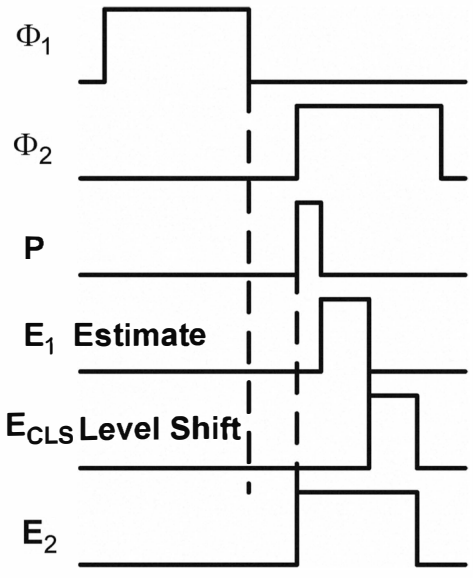

Figure 7 Timing Diagram

The schematic of the S/H is shown in figure 6. The clock phases are shown in figure 7. The gain error is shown in the figure 8. The gain error of an S/H block shows 40 dB

improvements as compared to a conventional ZCBC. THD simulation result is shown in figure 9.

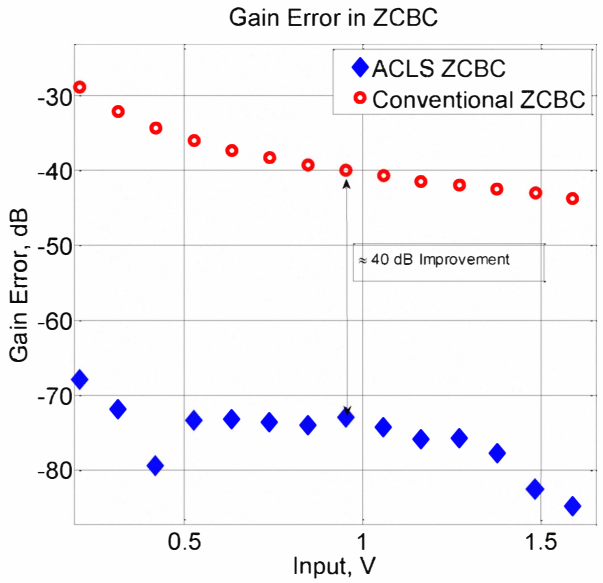

Figure 8 Gain Error, Conventional and ACLS

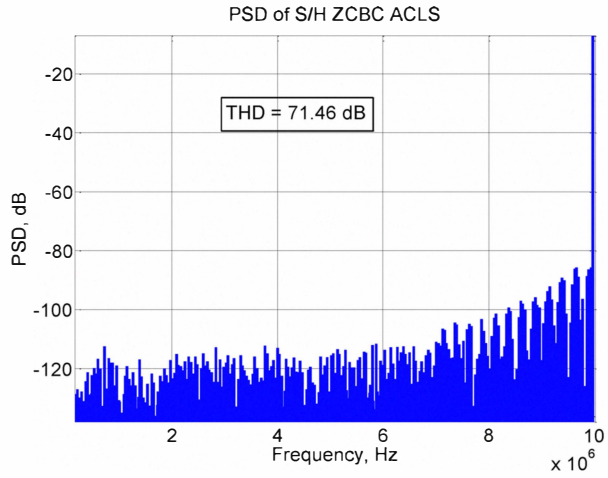

Figure 9 PSD of S/H Stage of ACLS based ZCBC, THD = 71.46 dB

V. Conclusion

An Asynchronous CLS technique for ZCBC was presented. This technique provides better linearity for the current source as compared a conventional ZCBC. Simulation results indicate more than 10bit linearity with single transistor current source. Therefore, the design requirements for the current source are reduced as compared to a conventional zero crossing based circuits. The design trade-off between linearity, speed, PSRR and power consumption were briefly discussed with respect to the choice of CLS capacitor.

VI. Appendix

The output voltage at the end of estimation phase can be derived as follows,

$$V_{o,ideal}(t_1) = I_c r_c (1-e^{-t_1/r_c C_{eff1}}) = \frac{V_{in} C_1}{C_2} \quad - \quad (7)$$

Where, I_c is the coarse current source value, r_c is the finite output resistance of coarse current source, C_{eff1} is the effective load capacitance in (3) and t_1 denotes the end of estimation phase. The above expression assumes that comparator is ideal with zero-delay and the current source is turned-off as soon as the comparator input crosses virtual ground. With finite comparator delay (7) can be re-written as follows,

$$V_{o,delay}(t_1+t_{d1}) = I_c r_c (1-e^{-(t_1+t_{d1})/r_c C_{eff1}}) \approx \frac{V_{in} C_1}{C_2}\left(1-\frac{t_{d1}}{r_c C_{eff1}}\right) + \frac{I_c t_{d1}}{C_{eff1}} \quad - \quad (8)$$

Assuming that the comparator delay is much smaller as compared to the time constant at the output, (8) represents the simplified first-order approximated output. The output at the end of level shifting phase can be derived as

$$V_{o2}(t_2+t_{d2}) = -I_f R_f \alpha (1-e^{-(t_2+t_{d2})/r_f C_{eff2}}) + V_{o,delay}(t_1+t_{d1}) \quad (9)$$

Where I_f is the fine current source, r_f is the output impedance of fine current source, $\alpha = \frac{C_{eff3}+C_{CLS}}{C_{CLS}}$, t_{d2} is the delay of the comparator at the end of level shifting phase, C_{eff2} is defined in (4), t_2 is the end of level shifting phase. Assuming the time delay of the comparator is small as compared to the time constant in the level shifting phase, (9) can be approximated to (4).

VII. Acknowledgement

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