# PDF Folding for Stochastic Flash ADCs

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***Abstract*—A circuit is presented that halves the number of comparators required for a two-group stochastic flash ADC. In a two-group stochastic flash ADC, two Gaussian PDFs are shifted left and right by applying a global offset reference to the two groups of comparators. This creates a virtual uniform distribution of comparator offset between the two global offsets. Over half of the comparators fall outside of the virtual uniform distribution and are not used. The proposed circuit inverts the polarity of each comparator offset until it is within the useful range, creating a virtual uniform distribution of comparator offsets with few comparators wasted.**

## I. Introduction

There is a strong trend for CMOS process technology to scale device geometries to smaller and smaller physical dimensions and we can expect this trend to continue [1][2]. Shrinking the physical dimensions of transistors creates many benefits as well as challenges. There are benefits in speed, power, and area for digital circuits, yet reduction in intrinsic device gain and lower supply voltage make it difficult to migrate previous analog designs to the next technology node. In fact, scaling analog circuits does not necessarily lower power or area [3].

Flash architecture based analog-to-digital converters (ADCs) are the preferred ADC architecture for high-speed applications [4][5]. Flash-based ADCs consist of an input that is connected to a set of comparators that are all given different references, which are typically equally spaced by a least-significant-bit (LSB) voltage. In order to achieve high speed in a new technology, it is desirable to aggressively scale the comparator to take advantage of the increased speed available on a new process; however, aggressive scaling of the comparator leads to a larger input-referred offset due to random device variation. This offset acts like an error in the comparator reference. To avoid an incorrect output code, comparator offset should be smaller than the LSB level. This requires that each comparator consume a large area footprint, or offset-canceling circuit techniques such as autozeroing or output offset storage must be implemented as described in [6]. Due to low intrinsic device gain multiple cascaded gain stages are typically used [7]–[9].

A stochastic ADC [10] is one solution to avoid large area comparators and high power preamplifiers. A stochastic ADC does not provide separate LSB references to each comparator, but instead allows each comparator to use its random input-referred offset as its reference. It has been demonstrated in [11] that it is possible to obtain a roughly linear transfer function by using two sets of comparators, each with a applied global offset of $\pm 1.078\sigma$, where $\sigma$ is the standard variation of comparator offset. The resulting probability density function (PDF) of comparator offsets is shown in Fig. 1. One disadvantage of this technique is that although a near uniform distribution is generated between the two means of the Gaussian distributions, it comes at a cost of wasted comparators. On average, 48% of comparator thresholds will reside in the useful region. This leaves 52% of comparators outside the range of the signal. These comparators continue to function and consume power, yet provide no additional information since they will always evaluate "high" or "low" whether they are in the left PDF or right PDF, respectively. This paper describes a technique that folds each Gaussian PDF about its center to bring almost all of the comparators into the useful region.

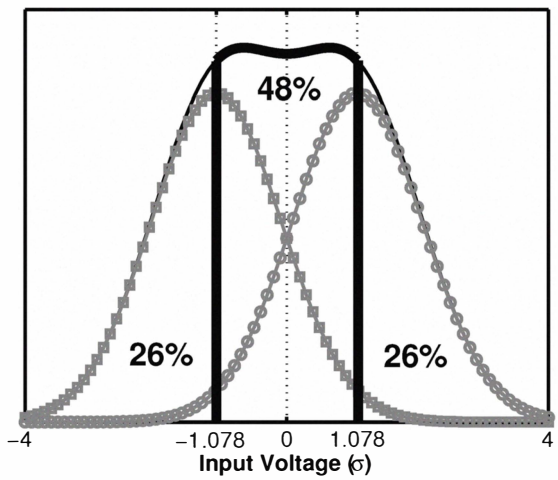



Fig. 1. This is the combined probability density function (PDF) of comparator offset for a two-group stochastic flash ADC. Gaussian PDFs are shifted left and right by applying a global offset reference to the two groups of comparators. This creates a virtual uniform distribution between the two global offsets. Over half of the comparators fall outside of the virtual uniform distribution and are not used.

## II. PDF Folding

Consider a comparator that has a $+100$mV input-referred offset. If this comparator lies in the "left" group of comparators a as defined in Fig. 1, then its output will always be "high" since the lowest differential voltage input in the signal range is 0V with respect to this comparator group. This comparator might as well always output "low" since either way it only contributes to a constant offset in the output code. Since the comparator offset is differential, if we can swap the polarity of the differential inputs, then the polarity of the offset will also be inverted. Fig. 2 shows an example of two different offsets of equal magnitude, but opposite polarity. It is apparent that

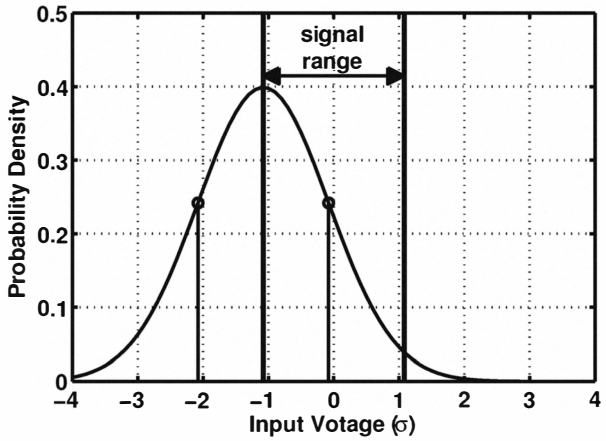



Fig. 2. For clarity, only the left PDF is shown. The two circles indicate two random comparator offsets that are equal in magnitude but have opposite polarity. After the global offset is applied, only one will fall in the useful signal range. By inverting both the comparator input and output, the polarity of the comparator offset is inverted.

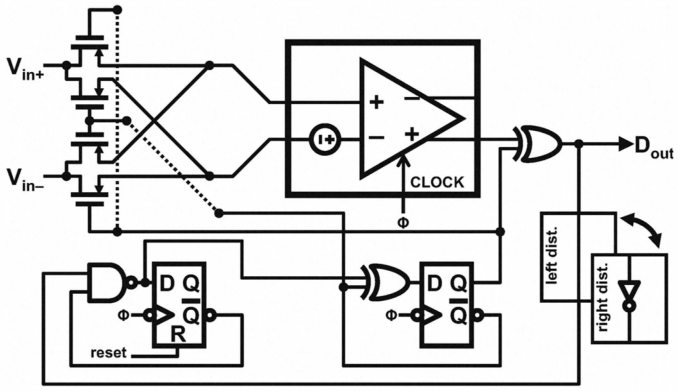
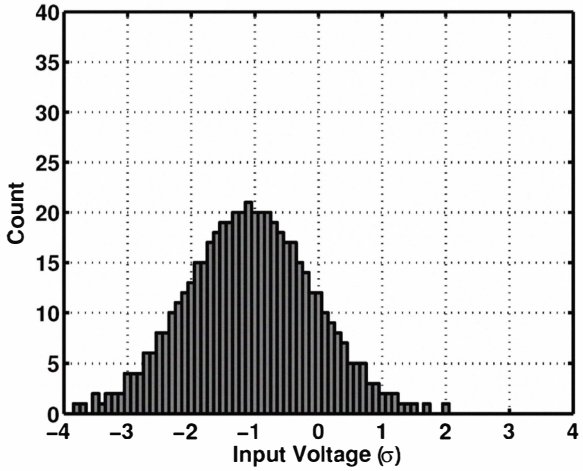


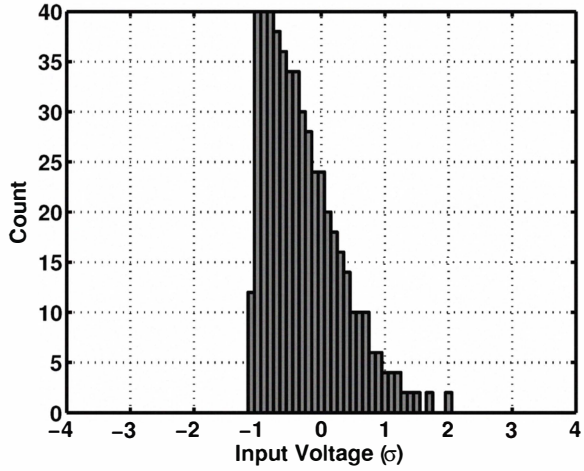

Fig. 3. This circuit implements the comparator offset polarity inversion seen in Fig. 2. The circuit causes the analog inputs to be swapped and the digital output to be inverted each clock cycle. Once the digital output indicates that the comparator offset is in the useful range, the polarity of the input/output remains fixed.

one offset is within the signal range and is desired, while the other lies outside of the signal range.

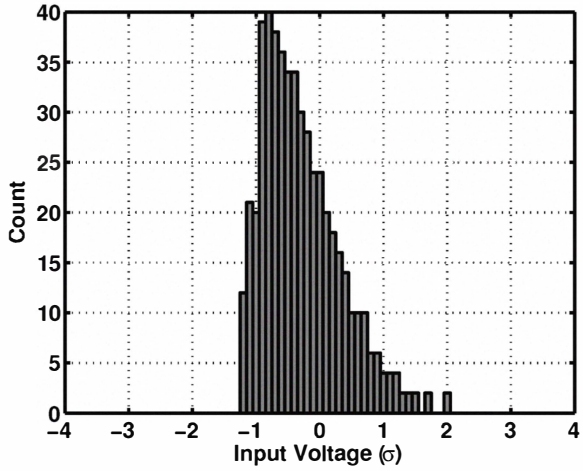
A circuit that effectively folds all of the offsets that lie outside the signal range into the useful area can be seen in Fig. 3. If the common-mode of the input is high enough, than four PMOS switches can provide the ability to swap the polarity of the input differentially. The output of one D-flip-flop controls whether the input path is differentially inverting or non-inverting. When the other "lock" flip-flop is reset, then the input will change polarity every clock cycle. We can not invert the input; however, without also inverting the digital output, so the flip-flop that controls the input polarity also inverts the output polarity through an XOR. The final digital output is fed back to the "lock" flip-flop. If the digital output is ever "low," then it is known that the offset is within the useful range, therefore "low" causes the "lock" flip-flop to output "high" indicating that the circuit is locked, and the




(a)

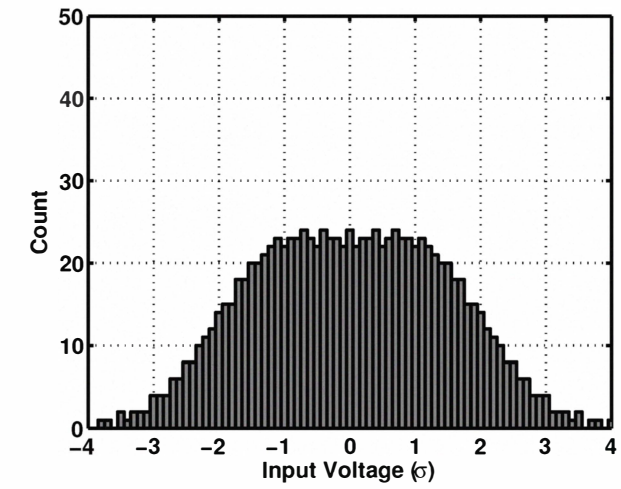



(b)

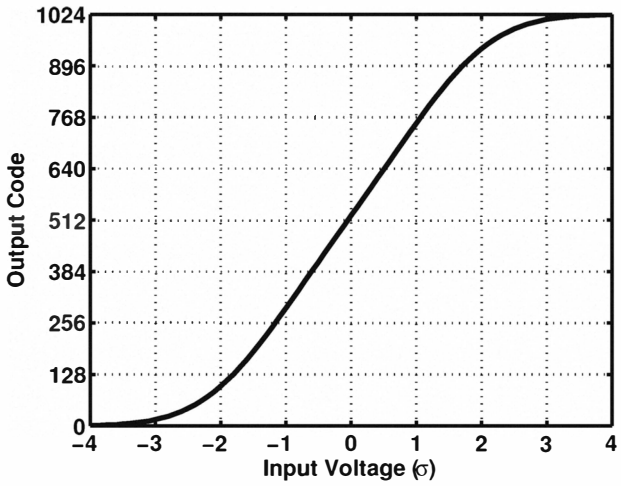



(c)

Fig. 4. a) This is a histogram of 512 Gaussian comparator offsets. b) This histogram shows the 512 offsets after PDF folding has been applied. c) This histogram also shows the 512 offsets after PDF folding has been applied but in the presence of noise.

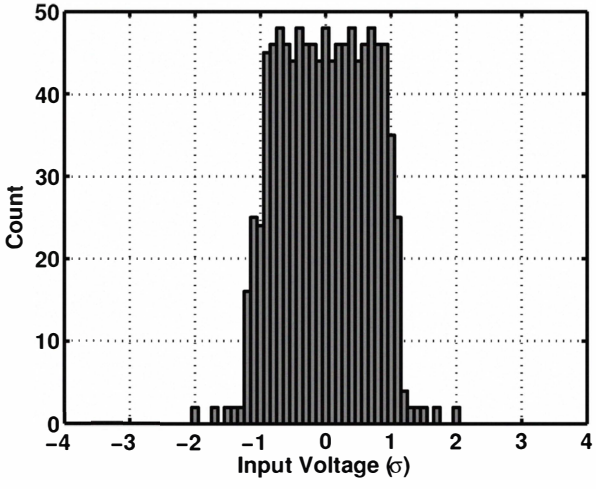



(a)

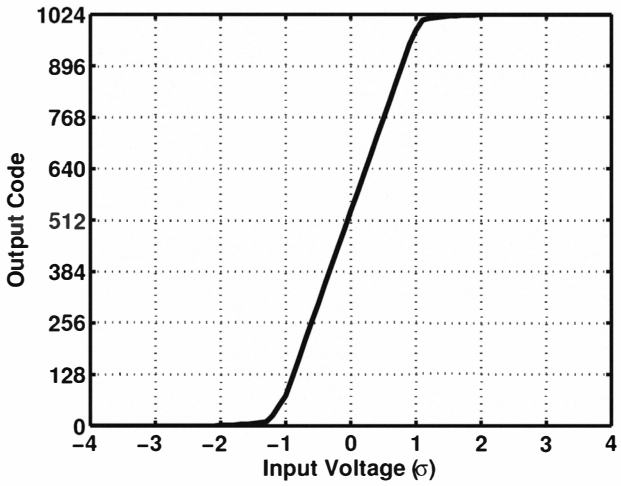



(b)

Fig. 5. a) This is a histogram of 1024 Gaussian comparator offsets in two groups of 512 and separated with global offsets as in Fig. 1. b) This is the corresponding transfer function for this set of comparator offsets.




(a)




(b)

Fig. 6. a) This is a histogram of the same offsets as in Fig. 5(a) after PDF folding has been applied. b) This is the corresponding transfer function for this set of comparator offsets.

input polarity will remain fixed. For the "right" group of comparators, the circuit inverts the output of the XOR that is fed back to the "lock" flip-flop as shown in Fig. 3.

An example of the result of PDF folding can be seen in Fig. 4. Fig.4(a) is a histogram of 512 normally distributed comparator offsets shifted "left" with a global reference of $-1.078\sigma$. A full scale sine-wave is applied with the PDF folding circuits running. Once the PDF folding circuits have all locked, the resulting distribution ideally appears as in Fig. 4(b). In reality there will be noise in the comparator that could cause comparators with small magnitude offsets to lock onto the incorrect side (Fig. 4(c)). Locking onto the incorrect side is still acceptable. Since noise caused the offset to appear to be in the signal range,the comparator will continue to be able to give information as noise causes it to appear within the signal range.

The final result of PDF folding can be seen by comparing Fig. 5 and Fig. 6. Fig. 5 shows the overall PDF and resulting transfer function for 1024 comparators as a 512-per-group two group stochastic flash ADC. As described before, only 48% of the comparators lie within the linear range of the converter. After PDF folding is applied for the same comparator offsets, the result is a virtual uniform distribution and shown in Fig. 6. In the end, PDF folding cuts the number of comparators required for a design in half.

It should be noted that while PDF folding reduces the number of comparators required, the PDF folding circuit adds a significant amount of area attributed to each comparator. If the PDF folding circuitry has comparable area to a single comparator then the area consumption of the two implementations would be comparable; however, if the comparator is a minimum-sized "digital-cell" comparator, then there will most likely be an increase in area. The savings comes in reduced

power consumption. Once all of the PDF folding circuits have locked into their final state, they will consume very little power, leaving only the power consumed by the comparator. Whereas, comparators that are outside the useful range will continue to consume power since they will reevaluate the signal every clock cycle.

## III. Conclusion

A circuit was presented that halves the number of comparators required for a two-group stochastic flash ADC. In a two-group stochastic flash ADC, two Gaussian PDFs are shifted left and right by applying a global offset reference to the two groups of comparators. This creates a virtual uniform distribution of comparator offset between the two global offsets. Over half of the comparators fall outside of the virtual uniform distribution and are not used and lead to increased power consumption. By inverting both the comparator input and output, the polarity of the comparator offset can inverted. The proposed circuit causes the differential analog inputs to be swapped and the digital output to be inverted each clock cycle until the digital output indicates that the comparator offset is in the useful range, then the polarity of the input/output remains fixed. Finally a virtual uniform distribution of comparator offsets is generated with a very small number of comparators wasted.


## Acknowledgment

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