Stochastic Flash Analog-to-Digital Conversion

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***Abstract*—A stochastic flash analog-to-digital converter (ADC) is presented. A standard flash uses a resistor string to set individual comparator trip points. A stochastic flash ADC uses random comparator offset to set the trip points. Since the comparators are no longer sized for small offset, they can be shrunk down into digital cells. Using comparators that are implemented as digital cells produces a large variation of comparator offset. Typically, this is considered a disadvantage, but in our case, this large standard deviation of offset is used to set the input signal range. By designing an ADC that is made up entirely of digital cells, it is a natural candidate for a synthesizable ADC. Comparator trip points follow the nonlinear transfer function described by a Gaussian cumulative distribution function, and a technique is presented that reduces this nonlinearity by changing the overall transfer function of the stochastic flash ADC. A test chip is fabricated in 0.18-μm CMOS to demonstrate the concept.**

***Index Terms*—Analog–digital conversion, comparators, statistical analysis, stochastic systems.**

I. Introduction

As CMOS DESIGNS are scaled to smaller technology nodes, many benefits arise, as well as challenges. There are benefits in speed and power due to decreased capacitance and lower supply voltage, yet reduction in intrinsic device gain and lower supply voltage make it difficult to migrate previous analog designs to smaller scaled processes. Moreover, as scaling trends continue, the analog portion of a mixed-signal system tends to consume proportionally more power and area and have a higher design cost than the digital counterpart. This tends to increase the overall design cost of the mixed-signal design. Automatically synthesized digital circuits get all the benefits of scaling, but analog circuits get these benefits at a large cost. The technique presented in this paper will be discussed in the context of the scaling of flash analog-to-digital converters (ADCs) to future digital CMOS processes.

All comparators have some input-referred offset due to random device mismatch. In a flash ADC, minimizing comparator offset is critical to the overall accuracy of the converter. This requires that each comparator consume a large-area footprint in an effort to reduce device mismatch, or offset-canceling circuit techniques such as autozeroing or output offset storage must be implemented as described in [1]. The latter technique requires storing offset values on capacitors at the output of gain stages. Due to low intrinsic device gain, multiple cascaded gain stages are typically used [2]–[4]. Instead of suppressing comparator offset, it is possible to use the random nature of the offset as part of a stochastic ADC.

Flash ADCs typically use a reference ladder to generate the comparator trip points that correspond to each digital code. First proposed in [5], a stochastic ADC uses comparators' inherent input-referred offset due to device mismatch as the trip points. It has been proposed in [6] that, by determining the offset of each comparator, it is possible to choose comparators with offsets that correspond to a desired transfer function. Choosing only the best of redundant comparators was also performed in the past in [7]. This solution requires a computationally expensive foreground calibration to generate a transfer function. In [6], the calibration logic consumed more area than the rest of the ADC combined, not including the computation engine which was off chip. If comparator offset follows a distribution that is nearly linear, then the resulting comparator offsets can be used as the transfer function, and none of this calibration hardware is required.

II. Theoretical Stochastic ADC

A. Single Comparator Group

In a basic flash ADC, an input signal is connected to the inputs of a group of comparators. The threshold of each comparator is set precisely, usually by a resistor string, such that all comparator thresholds are equally spaced by 1 LSB. In reality, there is also a random offset in each comparator that, in effect, readjusts each comparator threshold by a random amount. This random offset, due to device mismatches, will be assumed to be a Gaussian distribution with a mean (μ) of zero and a variance (σ^2) inversely proportional to the comparator area.

In a stochastic flash ADC, an input signal is also connected to the inputs of a group of comparators. However, the comparator thresholds are not precisely set by design but rather are allowed to be random. In the case of a standard flash, the comparator outputs after a conversion can be expected to be a thermometer code since the comparator thresholds are monotonically increasing by design. If each comparator threshold is random, however, then the comparator outputs cannot be expected to have any order. The total number of comparators that evaluate high will still be monotonically increasing with an increase in the input, so a ones adder is required to decode the output. This basic architecture with a group of comparators with random offsets followed by a ones adder is the basic stochastic flash ADC [Fig. 1(b)].

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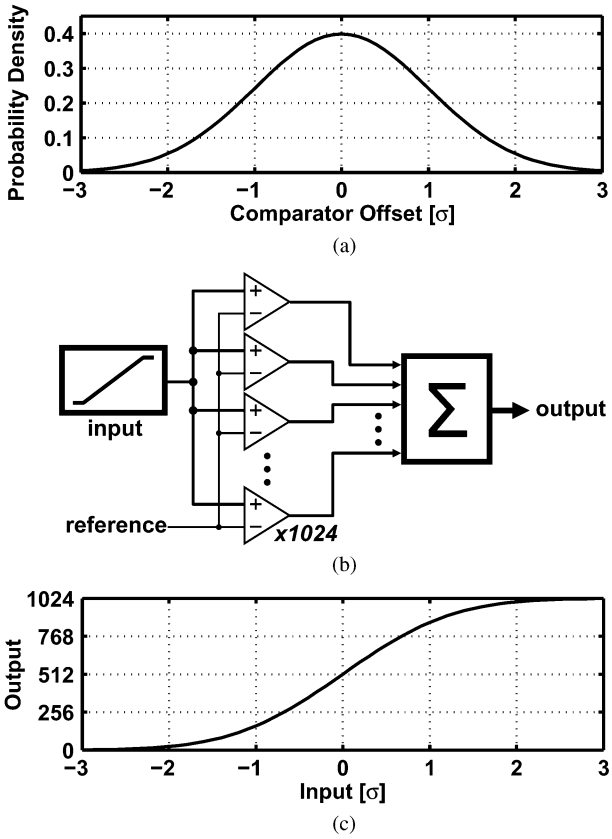


Fig. 1. (a) PDF of comparator offset in terms of standard deviation σ assuming Gaussian distribution. (b) 1024 comparators connected in parallel with a single fixed reference and a ramp input. This is the basic stochastic flash ADC. (c) Idealized output of the basic stochastic flash ADC with ramp input in terms of σ. In reality, having a finite set of comparators will cause the transfer function to not look smooth unless the number of comparators is very large.

The probability density function (pdf) of random comparator offset is influenced by many factors such as random variation of threshold voltage and current factor [8]. The central limit theorem [9] indicates that, since comparator offset is a sum of independent random variables with finite mean and variance, the pdf will be approximately Gaussian [Fig. 1(a)]. When a ramp signal is applied to the input of a basic stochastic flash ADC, the output will follow the cumulative distribution function (CDF) of comparator offset; therefore, the voltage transfer function of a basic stochastic flash ADC is the CDF of the random comparator offset [Fig. 1(c)]. The number of comparators in the stochastic flash ADC must be enough such that the actual transfer function resembles the comparator offset CDF to the desired degree.

B. Number of Comparators Required

In a standard flash ADC, the number of comparators required to obtain N bits of quantization is $2^N - 1$. Since, in a stochastic flash ADC, the comparator levels are not set deliberately but allowed to be random, a designer needs to know how many random comparator levels are required to obtain a desired accuracy. To analyze this, consider the case where comparator offset is random with a uniform pdf. The transfer function for a near-infinite number of comparators will merely be the CDF of this random offset, which will be a perfect line. Due to the random placement of each comparator level, a typical set of a smaller number of comparators will not give perfect linearity (Fig. 2).

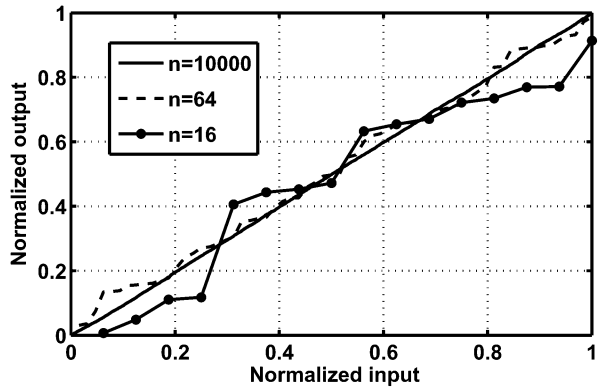


Fig. 2. Normalized transfer function of a basic stochastic flash ADC with uniformly distributed comparator offsets for three cases, where n is the number of comparators.

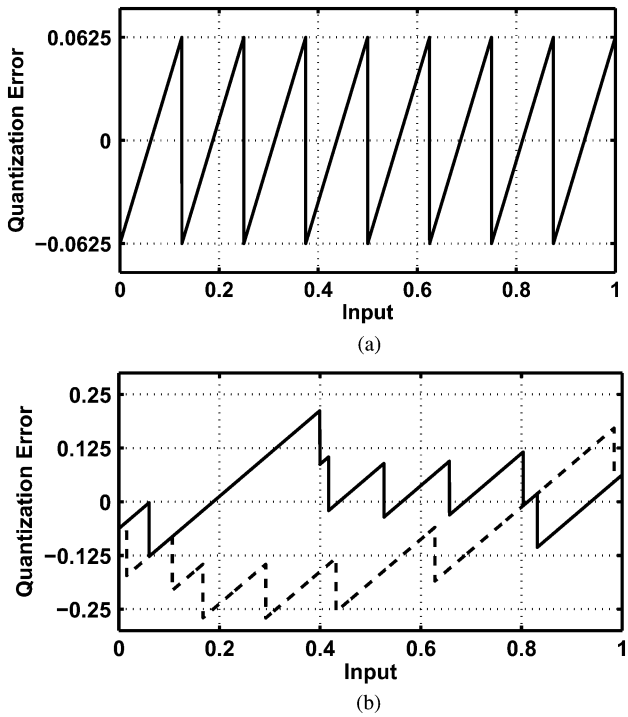


Fig. 3. (a) Quantization error of an ideal 3-bit flash ADC normalized to full scale. (b) Two examples of quantization error of a 3-bit flash with uniformly random comparator thresholds normalized to full scale.

Let us consider a theoretical ADC where comparator threshold is a uniformly distributed random variable between the range zero and one, and the input is also normalized to the range zero to one. If it is chosen to have n comparators, the comparator offsets will not be equally spaced between zero and one, but the average spacing will be $1/(n+1)$. For comparison, an ideal flash ADC has comparator spacing that is always equal to $1/(n+1)$. Quantization error, which is the residue from subtracting the output from the input, can be described by a ramp that is bounded between $-1/2$ LSB and $+1/2$ LSB [Fig. 3(a)]. This is because quantization error increases with a ramp input, but when the ramp passes above a comparator threshold, $1/(n+1)$ is subtracted from the error (i.e., the

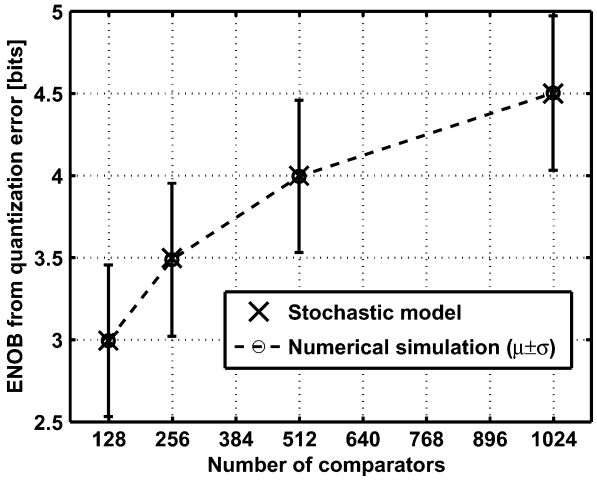


Fig. 4. ENOB as a function of number of comparators, where comparator thresholds are uniformly distributed across the input range. Note that the standard deviation (σ) of ENOB is 0.46 bits regardless of the number of comparators.

output increases by $1/(n+1)$). When the ramp passes above k comparator thresholds, the total $k/(n+1)$ is subtracted. This means that quantization error can be described for the input t as

$$q_{\text{error}}(t) = \left(t - \frac{k}{n+1}\right) \tag{1}$$

where k is a function of t and is, in fact, the transfer function of the ADC. Since, in the ideal case, quantization error is a periodic ramp, the root-mean-square (rms) error over the range between two comparator levels will be equal to the rms error over the entire range; we can find ideal quantization error by

$$V_{\text{rms,ideal}} = \sqrt{\frac{\int_{-1/(2(n+1))}^{1/(2(n+1))}(t)^2 dt}{1/(n+1)}} = \frac{1}{\sqrt{12}(n+1)}. \tag{2}$$

Now, by comparing the rms of quantization error to that of full scale by the definition of an ideal ADC and solving

$$V_{\text{rms,ideal}} = \frac{V_{\text{LSB}}}{\sqrt{12}} = \frac{\frac{1}{2^N}}{\sqrt{12}} \tag{3}$$

we find that the number of comparators (n) required to achieve N effective bits is (as expected)

$$n = 2^N - 1. \tag{4}$$

In a stochastic flash ADC, the plot of quantization error from a ramp input signal will look different than an ideal flash ADC due to random comparator level placement [Fig. 3(b)]. Let t be an input value between zero and one. Since comparator thresholds are random and uniformly distributed, the probability that a given random comparator threshold will be between 0 and t is equal to t. This exactly describes a binomial random variable [10]. Therefore, the probability that k comparator thresholds out of n total comparators are between 0 and t can be described by the binomial pdf, i.e.,

$$pdf_{\text{binomial}} = \binom{n}{k}(t)^k(1-t)^{n-k}. \tag{5}$$

Given this, we can determine the quantization error power. We square (1), multiply by the pdf (5), and sum over all values of k to obtain the variance of quantization error as a function of the input t

$$\text{Var}\left(q_{\text{error}}(t)\right) = \sum_{k=0}^{n}\left(t - \frac{k}{n+1}\right)^2\binom{n}{k}(t)^k(1-t)^{n-k}. \tag{6}$$

Now, integrate over the input range of t to obtain the total variance (power) of quantization error for the converter

$$q_{\text{error,power}} = \int_0^1 \text{Var}\left(q_{\text{error}}(t)\right) dt = \frac{n+2}{6(n+1)^2}. \tag{7}$$

Converting this into an rms voltage by taking the square root gives the rms quantization error, i.e.,

$$V_{\text{rms,stochastic}} = \sqrt{q_{\text{error,power}}} = \frac{1}{\sqrt{6}(n+1)}\sqrt{n+2}. \tag{8}$$

Again, by solving

$$V_{\text{rms,stochastic}} = \frac{V_{\text{LSB}}}{\sqrt{12}} = \frac{\frac{1}{2^N}}{\sqrt{12}} \tag{9}$$

we are able to obtain that, for a stochastic flash ADC with comparator thresholds that are uniformly distributed, the average number of comparators (n) required to achieve N effective bits is

$$n = 4^N - 1 + \sqrt{4^{2N} + 2^{2N+1}}. \tag{10}$$

For $N > 2$, this is approximately

$$n \approx 2 \cdot 4^N. \tag{11}$$

In a standard flash ADC, the number of comparators must be increased by a factor of two to obtain additional 1 bit of accuracy. This analysis shows that, to increase the accuracy of a uniformly random stochastic ADC by 1 bit, the number of comparators must be increased by a factor of four. This result can be easily verified with numerical simulation by taking n samples of a uniform random variable and using these values as the references for an ideal flash ADC. After applying a full-scale ramp input, the rms quantization error can be calculated empirically, finally giving the resulting effective number of bits (ENOB). Repeating this test many times, to satisfy the law of large numbers [11], allows us to find the average ENOB and standard deviation for a given number of comparators n. The plots of both the theoretical result and numerical simulation result are shown in Fig. 4. This analysis assumes not canceling any dc offset in the quantization error; if this offset is removed (as in a sine-wave test), the rms quantization error will be decreased by 3 dB [12]. It is also relevant to note that the standard deviation of ENOB is approximately 0.46 bits regardless of the number of comparators.

C. Multiple Comparator Groups

The actual distribution of comparator thresholds is not uniform but rather a Gaussian distribution, so this section will demonstrate how to effectively realize a uniform distribution of comparator thresholds. The transfer function of the basic

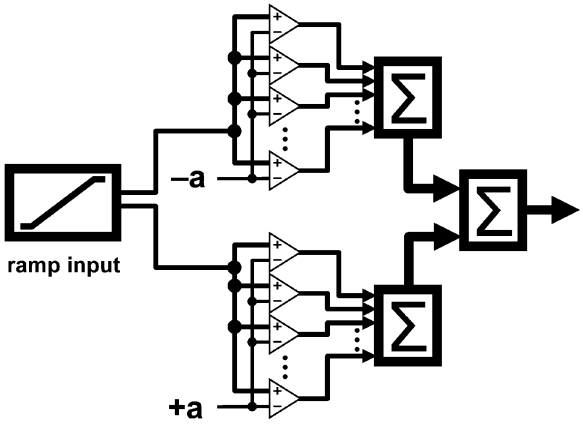


Fig. 5. By splitting the total number of comparators into two groups and applying an offset to each group, the shape of the transfer function can be controlled. For example, one group is given an offset of $+a$, and the other is $-a$.

stochastic flash ADC is the CDF of a Gaussian distribution. A Gaussian CDF is not linear [Fig. 1(c)], so linearization must be implemented in order to achieve a desirable linear transfer characteristic. Here, we will consider using two basic stochastic flash ADCs, each with a Gaussian CDF transfer function but with a different mean (Fig. 5). This can be implemented by adding a constant intentional offset to a group of comparators.

Changing the mean of comparator thresholds merely shifts the input-to-output transfer function along the input axis by applying a constant offset to all comparators in that ADC. The outputs of each ADC are summed to obtain the overall output of this two-group stochastic flash ADC. As the two pdf's are shifted such that the difference of their means increases, a somewhat linear region appears when the input is bounded between the means of the two pdf's (Fig. 6). The equation for a Gaussian CDF is

$$f(x) = \frac{1}{2}\left(1 + \text{erf}\left(\frac{x-\mu}{\sigma\sqrt{2}}\right)\right) \tag{12}$$

where

$$\text{erf}(x) = \int_{-\infty}^{x} \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-(u-\mu)^2}{2\sigma^2}} du. \tag{13}$$

Since the transfer function in which we are interested is for a two-group stochastic flash ADC, we will let $\mu = \pm a$, where an offset of a is applied to one ADC and an offset of $-a$ is applied to the other. We can let $\sigma = 1$, causing a to be in units of *number of standard deviations*, for simplicity without loss of generality. Therefore, the transfer function of a two-group stochastic flash ADC can be described by

$$g(x) = \frac{1}{4}\left(2 + \text{erf}\left(\frac{x-a}{\sqrt{2}}\right) + \text{erf}\left(\frac{x+a}{\sqrt{2}}\right)\right). \tag{14}$$

Since we are interested in when the input is bounded between $-a$ and a, we can find the integral nonlinearity (INL) by removing the constant linear portion and the overall offset of the transfer function by

$$\text{INL}(x) = g(x) - x\frac{g(a) - g(-a)}{2a} - \frac{1}{2}. \tag{15}$$

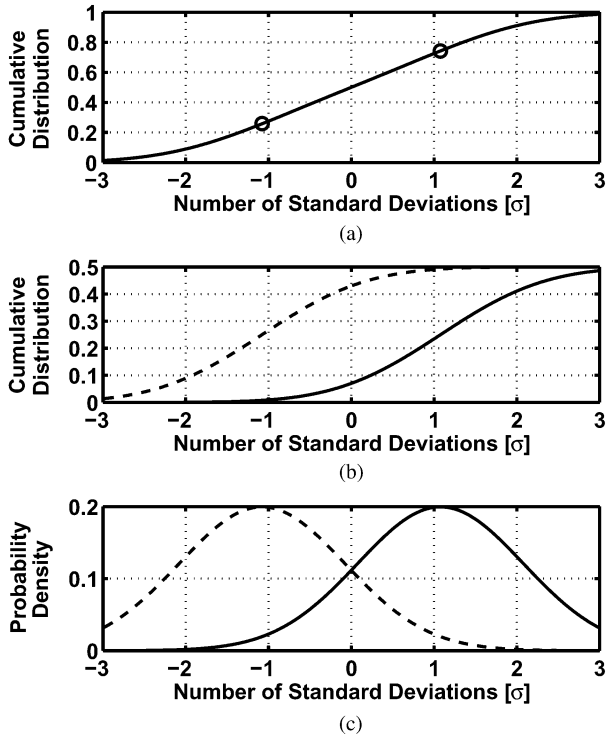


Fig. 6. (a) Resulting overall transfer function for a two-group stochastic flash ADC. By giving each group an offset, a more linear region appears between these two offsets (denoted by the circles on the transfer function). (b) Transfer function of each group before being combined into the overall transfer function. (c) Resulting pdf's of each comparator group after global offset is applied.

The rms value of this INL as a function of a is then

$$V_{\text{rms,INL}}(a) = \sqrt{\frac{\int_{-a}^{a} (\text{INL}(x))^2\, dx}{2a}}. \tag{16}$$

By relating this rms value of INL to the LSB voltage by (9), we are able to obtain the optimal value for a and what the maximum achievable number of bits (MANOB) is for a two-group stochastic flash ADC

$$\text{MANOB}(a) = \log_2\left(\frac{g(a) - g(-a)}{\sqrt{12}V_{\text{rms,INL}}(a)}\right). \tag{17}$$

The closed-form solution of (17) is rather cumbersome, and we would gain no additional insight by writing it out here; thus, a plot of (17) is shown in Fig. 7. There is a maximum of approximately 8.97 bits when a is approximately 1.078 standard deviations. This result means that the linear region between two offset Gaussian distributions, even if the number of comparator levels was infinite, is inherently limited to 8.97 bits. More importantly, if the targeted resolution is significantly less than 8.97 bits, then the comparator levels in the linear region between two offset Gaussian distributions are effectively uniformly distributed. Therefore, (11) can be applied if scaled by the inverse of the fraction of the comparator levels that will exist within the useful range.

D. Noise

The comparators used in a stochastic flash ADC must have a smaller area footprint than those used in a standard flash in order

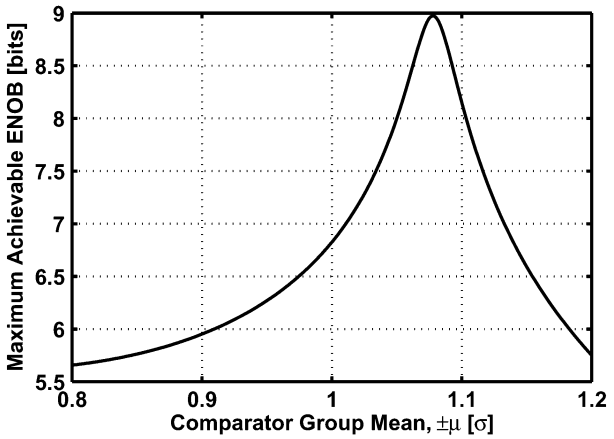


Fig. 7. Maximum achievable linearity as number of bits for a two-group stochastic flash ADC with comparator group offsets of $\pm a$. The input is also set to the range $\pm a$. The maximum of this function is 8.97 bits when $a = 1.078$ standard deviations.

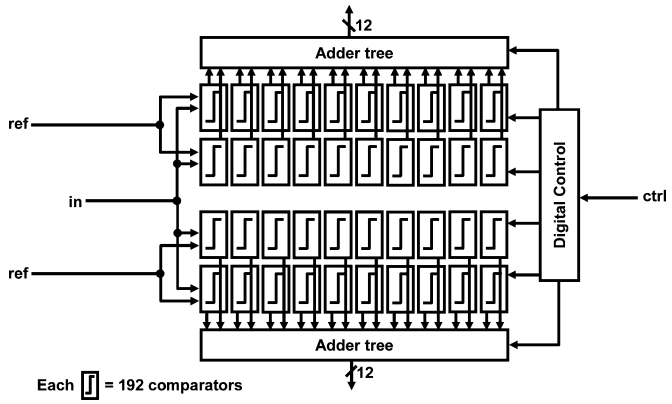


Fig. 8. Block diagram of the test chip. It is a two-group stochastic flash ADC with 3840 comparators in each group. These groups are then subdivided 20 times into 192 comparators per block. In this manner, the effective total number of comparators can be changed by digital control by independently enabling and disabling blocks of comparators.

to occupy the same comparator area since more comparators are required for the same resolution. Smaller area implies that there will be more flicker noise in these comparators. Moreover, lower transconductance of the input pairs due to smaller W/L implies that there will be more thermal noise. Notwithstanding that there will be more thermal and flicker noise per comparator, the overall input-referred noise of the ADC is not limited by the noise of any single comparator. It is reduced by an averaging effect of having many comparators.

III. System Level Consideration

The system level block diagram of our test chip is shown in Fig. 8. There are two separate groups of comparators, each with its own comparator reference. This is to implement the two-group stochastic flash ADC structure in Fig. 5. Adjusting the comparator reference for a group of comparators effectively changes the mean of the comparator offset CDF. In this manner, we can adjust the two comparator group references such that their means are $\pm 1.078\sigma$, yielding maximum linearity. As many comparators as possible were implemented on a chip; there are 3840 comparators in each group. Each group is then subdivided into 20 subgroups of 192 comparators each that can be independently enabled or disabled by digital control.

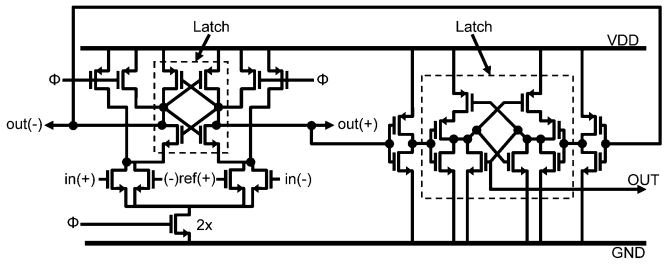


Fig. 9. Schematic of the comparator with a secondary latch to maintain digital output when the comparator is reset. All transistor sizes are $W/L = 0.22\ \mu\text{m}/0.18\ \mu\text{m}$ (the minimum allowed in this 0.18-μm process) with the exception of the indicated "2x" transistor which is $W/L = 0.42\ \mu\text{m}/0.18\ \mu\text{m}$.

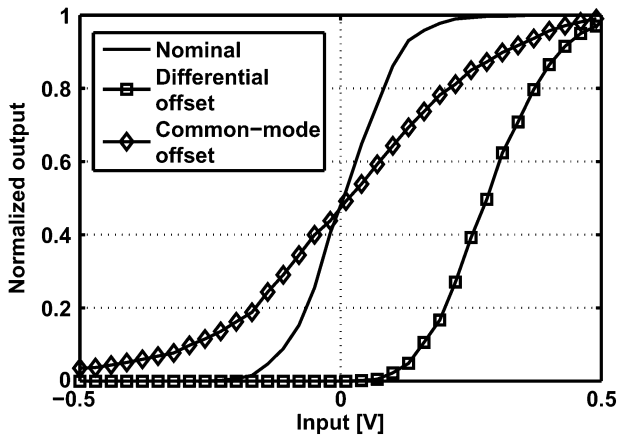


Fig. 10. Measured change in the transfer function of a basic stochastic flash ADC by changing the global comparator reference differentially and by changing the common mode.

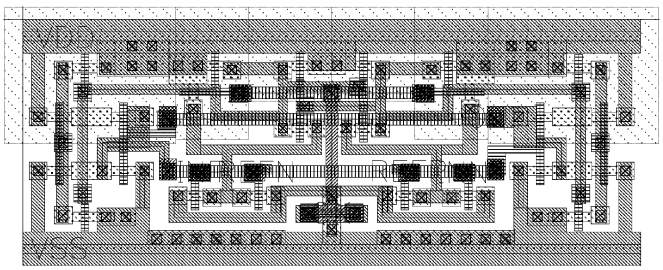
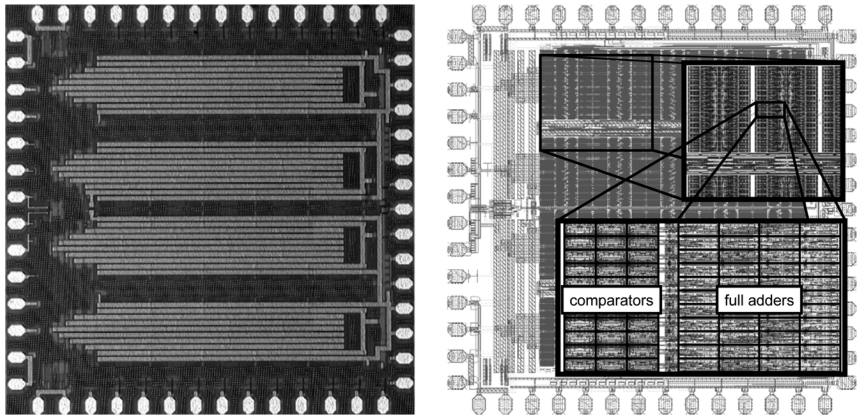


Fig. 11. Layout of the comparator and secondary latch. Minimum-sized devices are used, and the supply rail pitch matches digital library cells to allow for fully automated synthesis. Cell dimensions are 14.55 μm by 5.84 μm.

IV. Comparator Design

The schematic of the comparators that were implemented in the test chip is shown in Fig. 9. The comparator is followed by a secondary latch so that the digital output is maintained even when the comparator is reset. There is an interesting benefit in using a differential reference for the comparator in regard to control of the comparator offset distribution. Shown in Fig. 10, a differential change to the reference will cause a shift in the mean of the comparator offset CDF. A change to the common mode of the reference changes the standard deviation of comparator offset because this will increase/decrease the dynamic offset.



(a) (b)

Fig. 12. (a) Die photograph. Die dimensions are 2.4 mm by 2.4 mm. (b) Layout screen capture showing detail of functional blocks. Note the comparator size in relation to full adders.

This implies that, by controlling the two comparator group references, not only can the mean of the CDF be controlled but the shape as well.

The comparator and secondary latch are made with minimum-sized devices and incorporated into a digital cell (Fig. 11) that is comparable in size to a single full adder. The comparator cell has supply rails that match the pitch of the digital library rails to allow for automated synthesis. This design was not synthesized (software not ready), but it was implemented in this manner to highlight that synthesis is possible.

V. Digital Addition Tree

To perform the digital sum of all of the comparator outputs for each group, a pipelined Wallace tree ones adder was implemented [13]. Each comparator output is a single digital bit that is added with its two nearest neighbors by a 1-bit adder. The 2-bit result from this adder is then added with a neighboring 2-bit result to yield a 3-bit result. This continues until, finally, there is a single 12-bit digital result. Adder stages are separated by D flip-flops to pipeline the addition in order to minimize the time required for the adder tree to resolve each clock cycle.

VI. Measured Results

The test chip was fabricated in 0.18-μm CMOS (Fig. 12) with a total area of 5.76 mm^2. Each 192-comparator block devotes 0.017 mm^2 to analog comparators with a 0.022-mm^2 digital overhead for the full adders associated with that block. It can be seen in Fig. 13 that increasing the number of active comparators yields a measured increase in ENOB calculated from signal to noise and distortion ratio (SNDR). For each data point, 500 random combinations of comparator groups were enabled on four different chips to obtain an average ENOB and standard deviation for a given number of comparators. As a point of reference, simulated ENOB is also plotted. The simulation setup was two Gaussian random variables with $\mu = \pm 1.078\sigma$ and the same number of instances as comparators in the measurement setup. By taking many iterations of this simulation, we find the expected value and standard deviation of ENOB. The measured data are consistent with the simulated results.

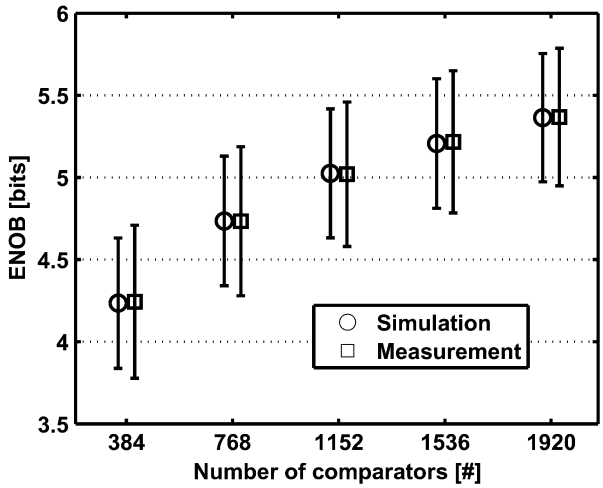


Fig. 13. Measured ENOB plotted against number of comparators activated. For comparison, numerically simulated results for the same setup are plotted. Error bars indicate $\pm\sigma$ of ENOB.

Since these digital cell comparators are made up of minimum-sized transistors, the standard deviation (σ) of comparator offset is expected to be quite large. In fact, measurement shows that, for our test setup with, for example, a supply voltage of 900 mV, $\sigma \approx 140$ mV. Because the signal range is approximately $-\sigma$ to $+\sigma$, the resulting signal range is 280 mV. Without the use of analog offset cancellation techniques, it would not be possible to build a standard flash ADC with comparator offsets of this magnitude. This is a major benefit in terms of synthesis since it would be very difficult to synthesize analog offset cancellation. Although the comparator offsets do not need to be calibrated, this technique does require two differential references to set the global mean of each comparator group. Fig. 14 shows that these differential references do not need to be absolutely accurate if the design is limited by quantization noise. For example, a servo loop could set the references in the background by comparing the digital output of each comparator group and slowly adjusting the two global references until the $+\sigma$ code of one group corresponds to the $-\sigma$ of the other group.

The two-group stochastic flash ADC linearization is shown in Fig. 15. For this example, we will choose 1152 comparators.

TABLE I
PERFORMANCE SUMMARY

Technology	0.18μm CMOS
Resolution	6b
Max Sampling Rate	18MS/s
Supply Voltage	900 mV
Comparator Offset Standard Deviation	140 mV
Input Range	280 mVpp (differential)
SNDR / SFDR @ f_S=8 MHz f_{in}=1 MHz	33.59 dB / 42.86 dB
DNL @ f_S=8 MHz	-0.38 / +0.50 LSB
INL @ f_S=8 MHz	-1.06 / +1.07 LSB
Analog Power @ f_S=8 MHz	182μW
Digital Adder Power @ f_S=8 MHz	261μW
Clock Driver Power @ f_S=8 MHz	188μW
Total Power @ f_S=8 MHz	631μW
Core Active Area	0.43 mm^2

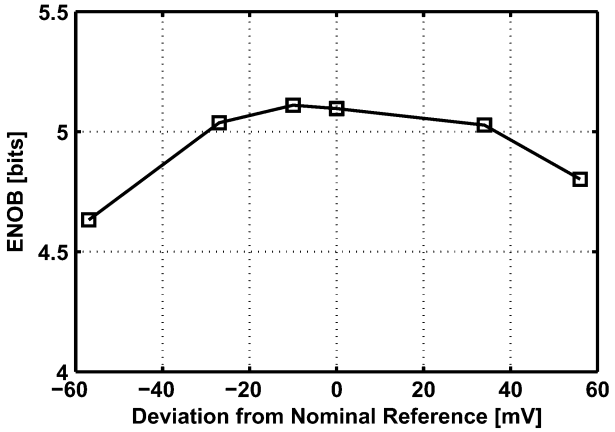


Fig. 14. Measured ENOB for two groups of 576 comparators each as a function of deviation from the nominal differential references $\pm 1.078\sigma$. The range -60 to $+60$ mV is equivalent to $\pm 0.8\sigma$ and $\pm 1.2\sigma$, respectively.

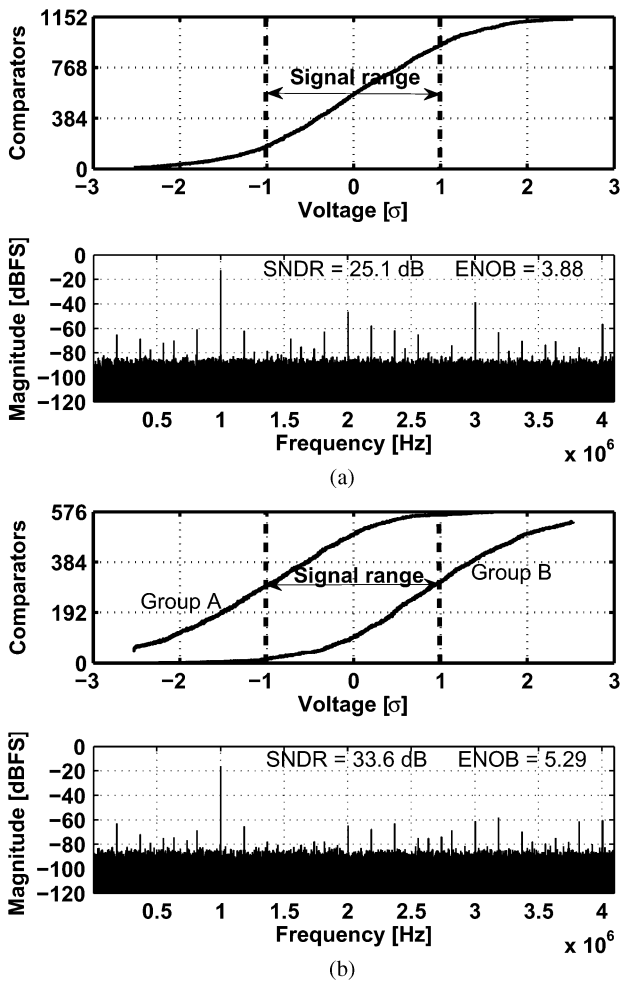


Fig. 15. (a) Measured transfer function of a single group of 1152 parallel comparators ($\sigma \approx 140$ mV) and fast Fourier transform (FFT) of the 1-MHz sine input. $f_S = 8$ MHz. (b) Measured transfer function of the same parallel comparators as two groups of 576 with differing fixed references set to $\approx -1.078\sigma$ and $\approx +1.078\sigma$ for groups A and B, respectively. FFT of the output from the sum of groups A and B of the 1-MHz sine input. $f_S = 8$ MHz.

With all 1152 comparators acting as a single parallel group, sweeping the input with a linear ramp reveals a transfer function that is indeed a Gaussian CDF. An SNDR of 25.1 dB is achieved with a 1-MHz sine-wave input and a sampling frequency of 8.192 MHz. Using the exact same comparators under the same conditions but merely dividing them into two groups with differing references ($\approx \pm 1.078\sigma$), an 8.5-dB improvement in SNDR can be seen.

Power consumption for the analog portion is 182 μW. Digital power is 449 μW with 188 μW consumed by clock drivers, leaving 261 μW consumed by the pipelined ripple-carry adder tree (see Table I).

An additional thing that can be measured is the input-referred noise as a function of the number of comparators (Fig. 16). Measuring the input-referred noise of a single regenerating latch comparator is not trivial [14]. For a stochastic flash ADC, measuring the input-referred noise can be done by applying a dc input and clocking the comparators multiple times. Since each comparator level is equated to some effective voltage change, rms noise is calculated by the square root of the variance of the output code. As expected, the input-referred noise decreases as the number of comparators increases due to an averaging effect of the noise.

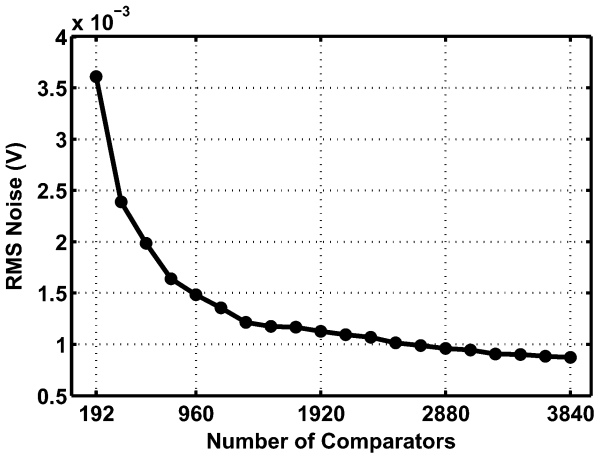


Fig. 16. Measured input-referred noise as a function of the total number of comparators.

VII. Conclusion

A stochastic flash ADC has been presented. The use of digital cell comparators allows such an all-digital design to be a natural candidate to be a synthesizable ADC. Using minimum-sized comparators that are implemented as digital cells produces a large variation of comparator offset. Typically, this is considered a disadvantage, but in our case, this large standard deviation of offset is used to set the trip point of each comparator and, in the end, the input signal range. Comparator trip points follow the nonlinear transfer function described by a Gaussian CDF. A technique has been presented that reduces this nonlinearity by changing the overall transfer function by building a two-group stochastic flash ADC. Setting the references of two comparator groups to have approximately $\pm 1\sigma$ of comparator offsets allows higher linearity to be achieved. By not correcting the individual comparator offsets, the number of comparators required to achieve N bits is on the order of 4^N as opposed the familiar 2^N; however, the calibration hardware required to calibrate individual comparator offsets can be prohibitively large and even exceed the size of the ADC itself. Since the comparators used have no preamplifiers, they will be highly scalable into deep submicrometer compared to autozeroing flash techniques which require analog amplification. In the future, as scaling trends continue, this type of ADC will become even more viable.

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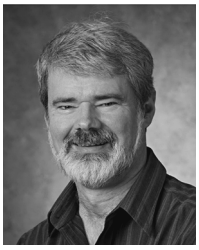

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