Domino-Logic-Based ADC for Digital Synthesis

Skyler Weaver, Benjamin Hershberg, Nima Maghari, and Un-Ku Moon

***Abstract*—A low-power synthesizable analog-to-digital converter (ADC) is presented. By cascading many digital-like domino-logic cells whose propagation delay is influenced by an analog input voltage, a digital value is obtained at the end of the allowed ripple period by determining the number of cells that the ripple passed through. The sample-and-hold is simply a bootstrapped switch into a small sampling capacitor. As each domino-logic cell passes the ripple, charge is kicked back onto the input capacitor, which creates a significant second harmonic. Distortion caused by even harmonics is canceled by implementing a pseudodifferential structure. A test chip is fabricated in 0.18-μm CMOS. The test chip achieves over 5.4-bit effective number of bits up to 50 MS/s with a 1.3-V supply. With a sampling frequency of 50 MS/s and a 24-MHz input, a 34.2-dB signal-to-noise-plus-distortion ratio is achieved while consuming 433 μW and occupying only 0.094 mm^2.**

***Index Terms*—Analog-digital conversion, low power, scaling, synthesis.**

I. Introduction

THERE IS A strong trend for CMOS process technology to scale device geometries to smaller and smaller physical dimensions, and we can expect this trend to continue [1]. By shrinking the physical dimensions of transistors, there is an innate reduction in the power–delay product for a given digital design, in addition to an overall area reduction [2]. By porting to a scaled technology, a digital circuit should have better performance; moreover, the design cost to port a digital design to a new process is relatively low since the design can be synthesized: that is, the physical layout is automatically generated. Analog circuits do not scale as effortlessly as their digital counterparts. While scaling improves digital circuits, scaling analog circuits gives increased speed but decreased gain and not necessarily lower power or area [2]. Porting an analog design to a new technology implies a large design cost, and since classic analog circuits are very sensitive to their physical layout, automated synthesis is impossible.

An analog-to-digital converter (ADC) architecture that can achieve low-to-medium resolution and be also synthesizable is therefore very desirable, with its main benefit being a very low design cost and high portability. One solution that has merit in this regard is a stochastic Flash ADC [4] and other Flash ADCs that use random comparator offset to generate voltage references [5], [6]. The main drawback of these types of ADCs is that they require a large area for either stochastic averaging or calibration hardware. A delay-cell-based ADC architecture is another solution that is highly digital [7], [8]. This work uses a chain of dynamic "domino-logic" cells to create a low-power low-cost ADC with the intention of being a candidate for a synthesizable ADC.

Manuscript received June 15, 2010; revised September 22, 2010 and December 31, 2010; accepted August 26, 2011. Date of current version November 23, 2011. This work was supported in part by the Semiconductor Research Corporation and in part by the Center for Design of Analog-Digital Integrated Circuits. This paper was recommended by Associate Editor J. Paramesh.

The authors are with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA (e-mail: weaversk@eecs.oregonstate.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2011.2168019

II. Circuit Implementation

A. Principle of Operation

A domino-logic-based ADC is a cascade of several dynamic delay cells such as that in Figs. 1 and 2 to create a circuit, as depicted in Fig. 3. The basic operation is as follows: A clock Φ is used to trigger the ADC such that, when $\Phi = 1$ ($\bar{\Phi} = 0$), all of the domino cells are reset, and the input voltage is sampled with a sample-and-hold into node $V_{\rm in}$. The domino cells are reset through small nMOS and pMOS switches with inputs of Φ and $\bar{\Phi}$, respectively. This resets the internal nodes of all of the cells and creates a high-impedance state between input $V_{\rm in}$ and the gate of pMOS M_p. After sampling, $\Phi = 0$ ($\bar{\Phi} = 1$), and every domino cell is in a ready state with all of the transistors off and in a high-impedance state. The first cell in the chain is triggered by $\bar{\Phi}$, as shown in Fig. 3. This causes nMOS M_n to turn on and create a conduction path between $V_{\rm in}$ and the gate of M_p. In this implementation, the sample-and-hold is a simple bootstrapped nMOS switch [9]; therefore, $V_{\rm in}$ is not actively being driven. This causes charge sharing with the parasitic capacitance at the gate of M_p and the capacitance at node $V_{\rm in}$. If the voltage at $V_{\rm in}$ is sufficiently low, the device M_p will turn on and trigger the next cell. The cells continue to trigger each other in series, and then, they are reset in parallel on $\bar{\Phi} = 1$. Digital outputs D_0 through D_n, just before resetting, is a thermometer code that can be encoded into binary as the ADC result.

B. Implementation Details

Since the sampling rate of this ADC depends on the number of cells and the rate at which they can propagate the digital ripple, we want to design the cell to have as small of a delay as possible in order to achieve a high sampling rate. The critical transistors in the delay path are M_n and M_p, whereas the reset switches and the digital buffer are less critical and only add unwanted parasitic capacitance to the internal nodes of the domino cell. Therefore, the reset transistors are minimum sized, and the critical transistors are slightly larger. Increasing the sizes of M_n and M_p will also add parasitic capacitance

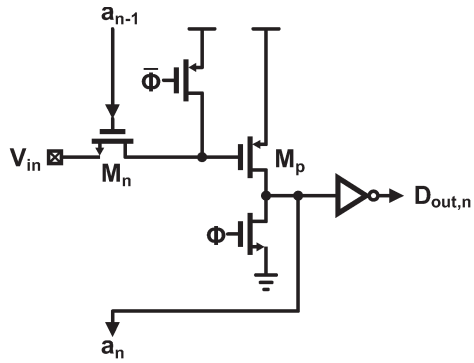

Fig. 1. Single "domino" cell. Input $V_{\rm in}$ is sampled when $\Phi = 1$ (i.e., $\bar{\Phi} = 0$) while the cell is reset. On the transition to $\Phi = 0$, the first domino cell is triggered such that $a_{n-1} = 1$, which causes $a_n = 1$ after some short delay that is dependent on input $V_{\rm in}$. This transition continues to propagate through the chain until the evaluation period is over, and once more, $\Phi = 1$.

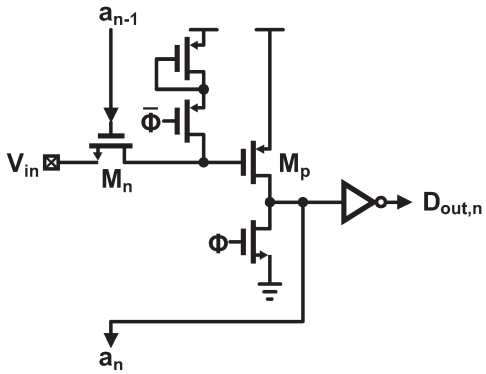

Fig. 2. Single "domino" cell with a shorter delay. The diode-connected device causes the gate of pMOS M_p to be reset to a voltage lower than supply voltage V_{DD} since there is a $V_{\rm TH}$ voltage drop across the diode. By presetting the gate of M_p close to its threshold, the device is on the verge of tripping. Charge injection from the pMOS connected to $\bar{\Phi}$ raises the voltage slightly so that the cell does not trip early.

that needs to be charged and discharged during operation. As this adds to power consumption, our design uses device widths for M_n and M_p that are just below twice the minimum for the process.

Fig. 1 shows that the gate of the device M_p is reset to positive supply V_{DD}. This means that, when M_n is turned on, enough charge must be shared with $V_{\rm in}$ in order to drop the gate voltage of M_p to $V_{DD} - V_{\rm TH}$, where $V_{\rm TH}$ is the threshold voltage for a pMOS before M_p starts to turn on M_n of the next domino cell. This takes a certain amount of time. By adding a diode-connected device in series with the pMOS reset switch (see Fig. 2), the gate of M_p will be reset to near $V_{DD} - V_{\rm TH}$ instead. This reduces the amount of charge that needs to be moved from the gate of M_p and, ultimately, the amount of time before M_p starts to turn on M_n. This would be a dangerous scenario, with M_p right at the tipping point of triggering the next cell. This could prematurely start a second "false" ripple further down the chain before the "true" ripple ever reached the cell. However, when the pMOS reset switch closes, there is enough charge injection that it guarantees that M_p will be off. This allows the design to operate at a higher speed without increasing power consumption by eliminating this "waste voltage."

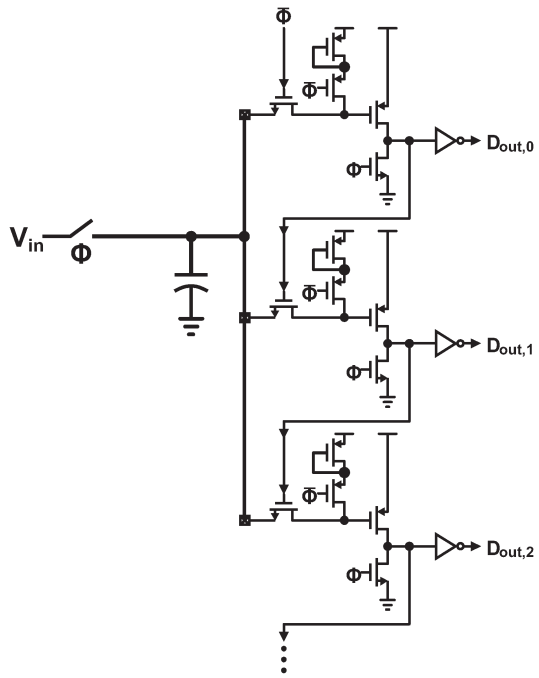

Fig. 3. This is an example of how multiple domino delay cells are combined to form an ADC. During $\Phi = 1$, the input is sampled onto the input capacitance while all of the domino cells are reset. When $\Phi = 0$, all of the cells are ready to trigger, and the first cell (designated by its output, i.e., $D_{\rm out,0}$) is automatically triggered since the gate of its nMOS is tied to $\bar{\Phi} = 1$. This starts a chain reaction as the cells begin to trigger in series until the end of the evaluation time. The number of cells that the trigger propagates through is related to the input.

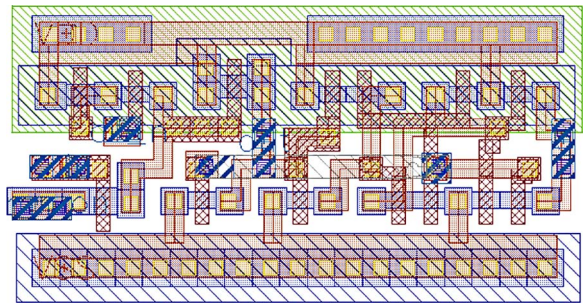

Fig. 4. Screen capture of the physical layout of a single domino cell. It consists of the circuit in Fig. 2 with the inverter replaced with a TSPC D-flip-flop all incorporated into a single digital cell. By using minimum-sized devices, the dimensions of this cell are only 4.08 μm $\times$ 9.36 μm in 0.18-μm CMOS.

Since the domino cells evaluate in a serial manner and are reset in parallel, more time is needed in the evaluation phase than the reset phase. Therefore, the sampling/reset time is created by a pulse generator, thus devoting most of the period to the cascading domino evaluation phase. The thermometer-coded output generated by the domino cells is latched into rising-edge triggered D-flip-flops that are latched on the rising edge of Φ. This feeds into a thermometer-to-binary converter and is given an entire clock cycle to resolve. True-single-phase-clock (TSPC) D-flip-flops [10] are incorporated into each domino cell, as shown in Fig. 4. The thermometer-to-binary converter chosen is a simple multiplexer-based decoder [11].

By itself, this ADC suffers from high nonlinearity in the form of a dominant second harmonic. This should come as no surprise since the speed at which each cell propagates has a

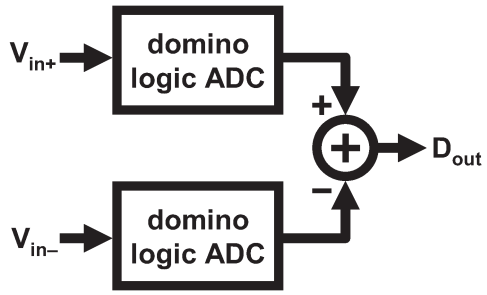

Fig. 5. By implementing two identical domino-logic ADCs and subtracting their digital output, the final result has a significantly reduced second harmonic. Otherwise, the performance would be limited by this second harmonic.

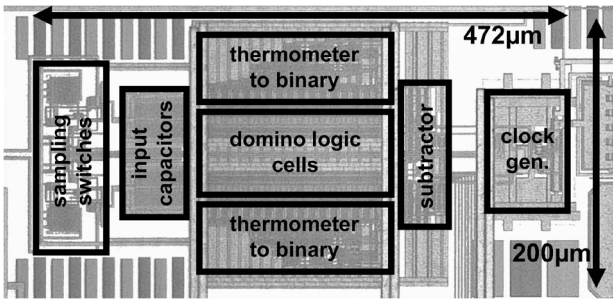

Fig. 6. Detailed die micrograph. Dimensions are 472 μm $\times$ 200 μm.

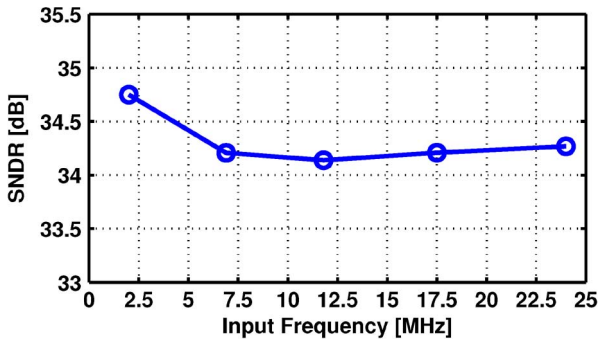

Fig. 7. The SNDR is well behaved over the Nyquist range of the converter. This measurement was taken with a sampling rate of 50 MS/s.

nonlinear relationship to $V_{\rm in}$; moreover, as each cell switches, the small amount of charge sharing with the parasitic capacitance at the gate of M_p causes the voltage at $V_{\rm in}$ to increase over time in a nonlinear way. Fortunately, most of the power of the second harmonic can be canceled by implementing a pseudodifferential structure, as shown in Fig. 5. The required subtraction is implemented as a digital binary adder with one of the ADC's outputs inverted by its two's complement.

A random mismatch can be expected to cause some variation in the delay of each cell. When compared with the nonlinearity from the previously mentioned sources, however, even large random mismatches correspond to relatively small differential nonlinearity (DNL) errors. Therefore, a mismatch should have little effect on the performance of the ADC. Monte Carlo simulations of random mismatches confirm this observation.

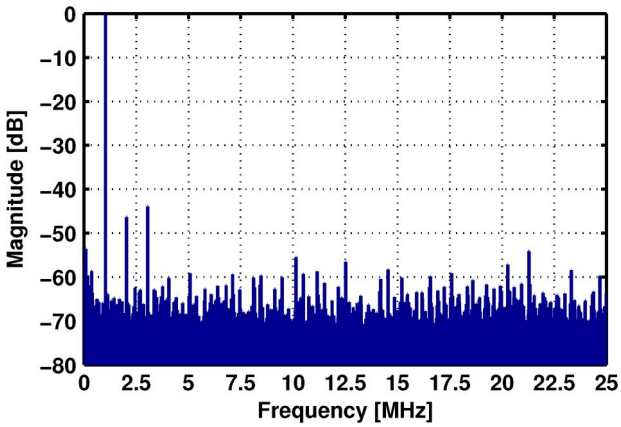

Fig. 8. Spectral fast Fourier transform (FFT) plot normalized to the input with an input of 1 MHz taken at 50 MS/s. The SNDR is 35.6 dB, and the spurious-free dynamic range (SFDR) is 44.0 dB.

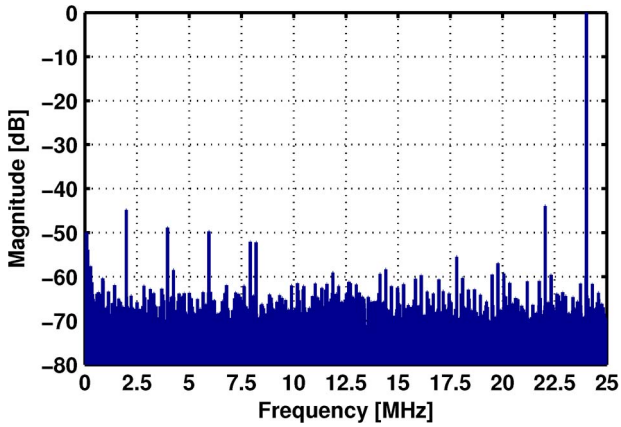

Fig. 9. Spectral FFT plot normalized to the input with an input of 24 MHz taken at 50 MS/s. The SNDR is 34.2 dB, and the SFDR is 44.0 dB.

III. Measurement Results

A test chip was fabricated in a 0.18-μm digital CMOS process (see Fig. 6). The chip has dimensions of 472 $\times$ 200 μm, consuming a total area of 0.0944 mm^2. The ADC is implemented as two domino-logic-based ADCs in a pseudodifferential configuration, each with 63 domino cells. The two 6-bit outputs are subtracted using a 6-bit ripple carry binary adder, which produces a 7-bit result that is sent off-chip. With a supply voltage of 1.3 V, a sampling rate of 50 MHz is achieved. A signal-to-noise-plus-distortion ratio (SNDR) is relatively consistent at above 34 dB across the input frequency even up to the Nyquist frequency, as shown in Fig. 7. Two spectral plots are provided in Figs. 8 and 9 to show the spectral output for a low frequency and a near-Nyquist frequency at the same sampling rate of 50 MS/s. Plots of DNL and integral nonlinearity (INL) are shown in Figs. 10 and 11, respectively. It is apparent from the INL plot that the performance is much more limited by the converter linearity rather than random variation. Power consumption varies with input frequency, with 312 μW consumed for a 1-MHz input and 433 μW for a 24-MHz input. This is due to the fact that, for low-frequency inputs, the thermometer-to-binary decoder switches less, particularly for the most significant bits since they change state less often. For

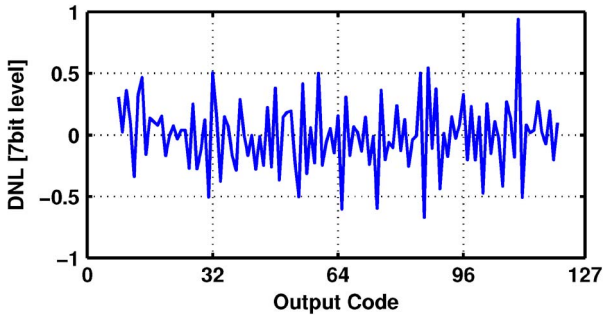

Fig. 10. Measured 7-bit level DNL.

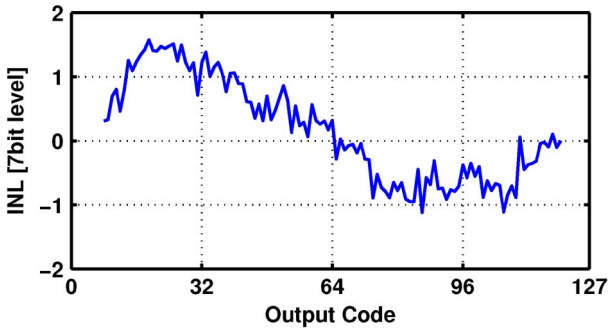

Fig. 11. Measured 7-bit level INL.

TABLE I
PERFORMANCE SUMMARY

Process Technology	0.18μm CMOS	
Resolution	7 b	
Supply Voltage	1.3 V	
Full-scale Input Range	560 mVpp differential	
Sampling Rate	50 MS/s	
Input Frequency	1.0 MHz	24.0 MHz
SNDR	35.6 dB	34.2 dB
ENOB	5.62 b	5.41 b
SFDR	44.0 dB	44.0 dB
Total Power	312 μW	433 μW
Figure-of-merit (FOM)	127 fJ/step	204 fJ/step
Total Active Area	0.094 mm^2	

near-Nyquist inputs, the thermometer-to-binary decoder may completely change its output from cycle to cycle.

IV. Conclusion

A domino-logic-based ADC was presented. The use of digital dynamic delay cells leads this design to be a good candidate for a highly scalable and synthesizable ADC. Adding this type of domino cell to a digital library would allow fully automated synthesis of this type of ADC. While this ADC cannot compete with the performance obtained by state-of-the-art successive-approximation ADCs directly, this ADC has an advantage by maintaining a very low design cost even in deep-submicrometer processes. The target application would be one where there is a design that is predominantly a digital circuit, but an ADC is required that must be compact and low power. A test chip was fabricated in 0.18-μm CMOS. The test chip achieves over 5.4-bit effective number of bits up to the Nyquist-rate of 50 MS/s with a 1.3-V supply. With a sampling frequency of 50 MS/s and a 24-MHz input, a 34.2-dB SNDR is achieved while consuming 433 μW and occupying only 0.094 mm^2 (see Table I).

Acknowledgment

The authors would like to thank National Semiconductor for providing fabrication of the prototype integrated circuit.

References

[1] B. Spencer, L. Wilson, and R. Doering, "The semiconductor technology roadmap," *Future Fab Int.*, vol. 18, Jan. 12, 2005.
[2] H. Iwai, "CMOS scaling towards its limits," in *Proc. 5th Int. Conf. Solid-State Integr. Circuit Technol.*, Oct. 1998, pp. 31–34.
[3] A.-J. Annema, "Analog circuits in ultra-deep-submicron CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 132–143, Jan. 2005.
[4] S. Weaver, B. Hershberg, D. Knierim, and U.-K. Moon, "A 6b stochastic Flash analog-to-digital converter without calibration or reference ladder," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2008, pp. 373–376.
[5] C. Donovan and M. P. Flynn, "A 'digital' 6-bit ADC in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 432–437, Mar. 2002.
[6] D. C. Daly and A. P. Chandrakasan, "A 6b 0.2-to-0.9 V highly digital Flash ADC with comparator redundancy," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2008, pp. 554–555, 635.
[7] T. Watanabe, T. Mizuno, and Y. Makino, "An all-digital analog-to-digital converter with 12-μV/LSB using moving-average filtering," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 120–125, Mar. 2003.
[8] H. Farkhani, M. M. Nejad, and M. Sachdev, "A fully digital ADC using a new delay element with enhanced linearity," in *Proc. IEEE Int. Symp. Circuits and Syst.*, May 2008, pp. 2406–2409.
[9] M. Dessouky and A. Kaiser, "A 1 V 1 mW digital-audio $\Delta\Sigma$ modulator with 88 dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, pp. 349–355, Mar. 2001.
[10] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 1, pp. 62–70, Feb. 1989.
[11] E. Sail and M. Vesterbacka, "A multiplexer based decoder for Flash analog-to-digital converters," in *Proc. IEEE TENCON*, Nov. 2004, vol. 4, pp. 250–253.