Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells

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Abstract

An ADC is synthesized entirely from Verilog code in 90nm digital CMOS using a standard digital cell library. An analog comparator is generated by cross-coupling two 3-input NAND gates. The random comparator offsets are used as the ADC references and are Gaussian. An implicitly aligned three-section piecewise-linear inverse Gaussian CDF function on chip linearizes the output. SNDR of 35.9dB is achieved at 210MSPS.

Introduction

An ADC is inherently a mixed signal system that contains both analog and digital components. Classically, it is the digital part that is synthesizable and can be generated from Verilog code, whereas the analog portion is designed on the transistor level with a fully customized layout. The comparator can be thought of as the block that defines the boundary between the analog and the digital circuitry. By moving the comparator as close to the input as possible, an ADC becomes as digital as possible. This essentially describes the flash ADC. Without pre-amplification, the only remaining analog components in a flash ADC are the comparators and their analog references. To make a comparator that is compatible with digital synthesis, it must be similar in size to that of standard digital cells. An implication of this is that the input-referred offset due to device mismatch will be significant. Using the inherent comparator offsets as the comparator references eliminates the need for analog references to be provided at all [1-3]. If the last remaining analog block, the comparator, can also be made out of standard digital cells, the entire design can be synthesized from Verilog code (Fig. 1).

Implementation Details

An analog equivalent comparator can be constructed from two standard CMOS NAND3 digital gates, as seen in Fig. 2. Cross-coupling the two NAND3 outputs and A inputs creates a positive-feedback latch similar to the back-to-back inverter latch of conventional clocked comparators. The clock is fed to the C inputs, which resets both outputs to high when the clock is low. When the clock goes high, the output capacitance is discharged through the three series NMOS devices. Connecting the B inputs to a differential analog input causes the discharging rate to be influenced by the input. Once one of the outputs drops below a PMOS threshold, the positive-feedback latch captures the outputs. The voltage of the inputs should be high enough that the PMOS devices (grayed out) that are connected to the input are effectively off. Otherwise, the comparators may stay reset and never evaluate.

Using a comparator made up of standard digital cells, the entire ADC is implemented from Verilog code. A flash ADC that uses random comparator offsets as the comparator voltage references, without calibration, requires 4^b comparators for b effective bits [4]. In this design, 2047 comparators are implemented for a target of 5.5bits (35dB SNDR). The comparator outputs are encoded into a binary value through a Wallace adder, which is pipelined to reduce the logic delay. The raw binary output of the ADC from a ramp input signal will be the cumulative distribution function (CDF) of the comparator offset. Since the CDF can be expected to be Gaussian, the raw output is passed through the inverse function of a Gaussian CDF to linearize the output data.

If the mean or standard deviation of the comparator offset distribution should change due to PVT or any other reason, the CDF transfer function would be shifted and scaled with respect to input voltage; however, the shape of the CDF remains the same with respect to output code. The digital output only represents the shape of the CDF, e.g. code 0 (signed) always represents the mean of the distribution, and code +699 always represents one standard deviation above the mean. Therefore, no calibration or tuning is required; the inverse Gaussian CDF is hard coded into the chip. The inverse function could be implemented as a lookup table, but this is unattractive due to the significant hardware requirement. Instead, the inverse function is approximated mathematically as a piecewise linear function, the result of which can be seen in Fig. 3. For hardware simplicity, the piecewise regions are chosen to use the slopes 1, 1.5, and 2.5 and extend the linear range to ±1.6 standard deviations (σ) of the comparator offset distribution. Multiply by 1.5 (1+1/2) and 2.5 (2+1/2) can be implemented in hardware as simple bit-shifting and addition, which requires minimal hardware. By extending the input range to $\pm 1.6\sigma$, 90% of the total comparators are used.

A standard digital synthesis procedure was followed to synthesize the circuit and generate the layout. In order to preserve the analog input path and ensure that the comparator module is not altered during synthesis, "don't touch net" and "don't touch" directives were given to the synthesis tool.

Measurement Results

The ADC is fabricated in a 90nm digital CMOS process and occupies 0.18mm^2 (Fig. 6). The input is connected directly to the comparators without a S/H. The total parasitic input capacitance due to routing and 2047 comparator inputs is 2.5pF. The measured standard deviation for an input common-mode of 800mV and a 1.2V supply is 45mV. As demonstrated in Fig. 4, a change to the input common-mode has a strong impact on the standard deviation of the comparator offset distribution. At a higher input common-mode the proportional difference in the NMOS overdrive voltages is reduced causing the distribution to spread out. Over 35dB SNDR is achieved with a 1MHz input up to a sampling rate of 210MSPS. This sampling rate is within the specification of the clock period given to the synthesizer and is limited by logic delays chosen by the synthesis tool. Power consumption is 34.8mW at 210MSPS from the 1.2V supply.

With a supply of 700mV, the ADC achieves 34.6dB SNDR for a 1MHz input at 21MSPS, and consumes 1.11mW.

An interesting property of this ADC can be seen in Fig. 5. Because nonlinearity is dominated by the shape of a Gaussian CDF and the piecewise-linear function (Fig. 3), SNDR is relatively independent of input signal amplitude. Also in Fig. 5 is a plot of SNDR as a function of input frequency. The degradation in SNDR is due to the parasitic filtering of the input through the automatically synthesized input nets. The roll-off at about 60MHz was predicted from extracted simulation.

Conclusion

By creating a comparator out of standard digital CMOS cells, a stochastic flash ADC can be implemented and synthesized entirely from Verilog code. The result is a truly all digital ADC with the only analog input being the input signal.

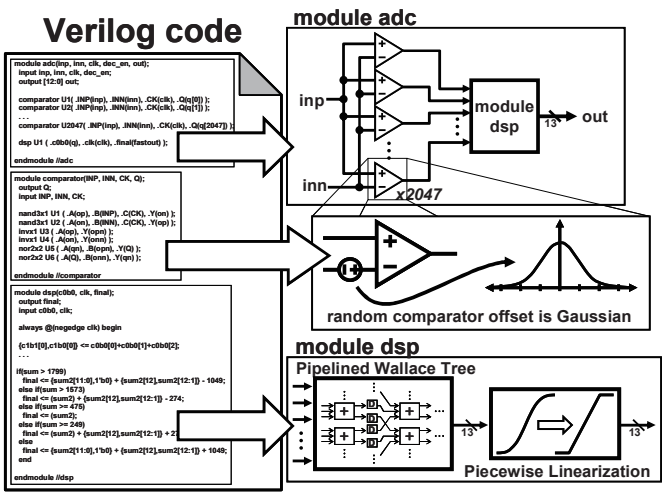

Fig. 1. Block diagram of Verilog code based stochastic flash ADC.

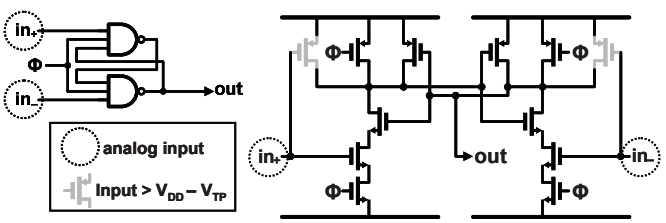

Fig. 2. Analog comparator made from standard digital cells using two standard digital NAND3 cells.

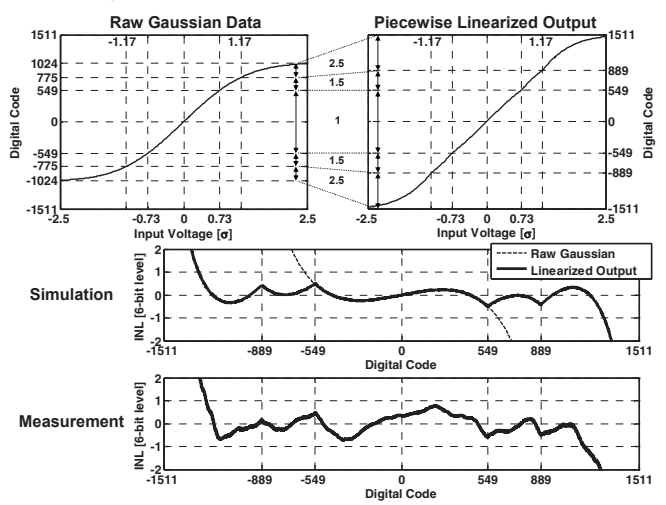

Fig. 3. Code-domain linearization is independent of PVT and is a low hardware cost compared to a lookup table.

Acknowledgements

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References

[1] T. Sundström and A. Alvandpour, "Utilizing Process Variations for Reference Generation in a Flash ADC," *IEEE Trans. Circuits and Systems II*, vol. 56, pp. 364–368, May 2009.

[2] D. C. Daly and A. P. Chandrakasan, "A 6b 0.2–0.9 V Highly Digital Flash ADC with Comparator Redundancy," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 554–555.

[3] C. Donovan and M. P Flynn, "A 'digital' 6-bit ADC in 0.25-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 432–437, Mar. 2002.

[4] S. Weaver, B. Hershberg, P. Kurahashi, D. Knierim, and U. Moon, "Stochastic Flash Analog-to-Digital Conversion," *IEEE Trans. Circuits and Systems I*, vol. 57, no. 11, pp. 2825-2833, Nov. 2010.

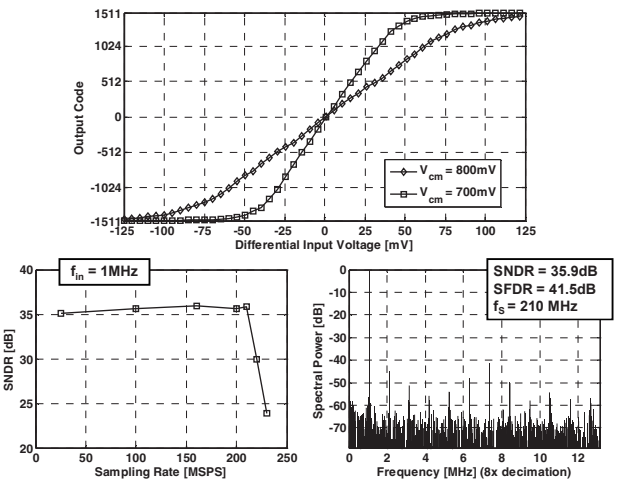

Fig. 4. Measured transfer function and dynamic performance.

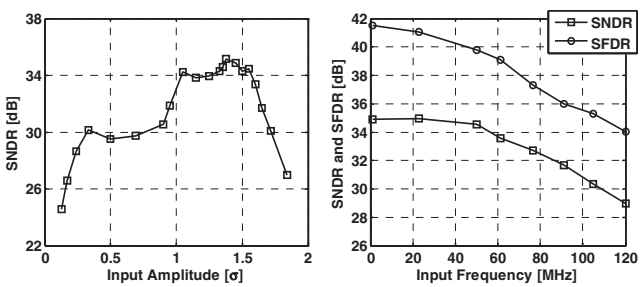

Fig. 5. SNDR measured vs. signal amplitude (f_S=210MHz). SNDR, SFDR vs. input frequency also measured (f_S=100MHz).

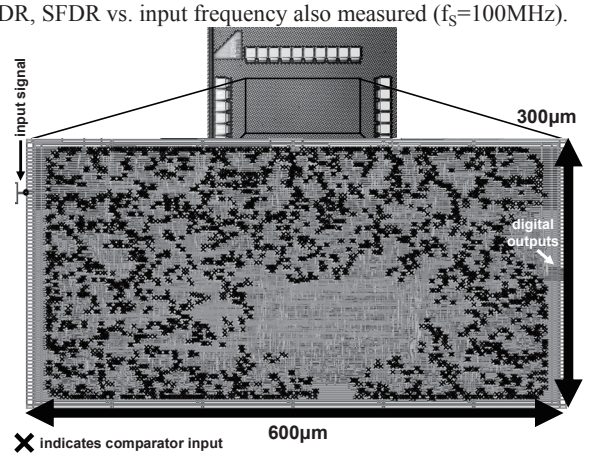

Fig. 6. Micrograph and screen-capture of entire synthesized layout.