The Effect of Correlated Level Shifting on Noise Performance in Switched Capacitor Circuits

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***Abstract*—The relation between opamp noise and the size of the level shifting capacitor in correlated level-shifting (CLS) architectures is explored. Analysis is performed for a Split-CLS switched capacitor amplification circuit, and many of the conclusions in this paper are applicable to more general CLS architectures as well. A theoretical model for noise is developed and shown to be in good agreement with simulation. It is found that for practical design values, the size of the level-shifting capacitor only weakly influences noise performance.**

I. Introduction

A fundamental limitation of accuracy in switched capacitor amplification circuits is that of finite opamp gain error. As silicon semiconductor processes march ever deeper into the realm of nanometer feature sizes, device characteristics have changed and achieving the requisite opamp gain for high accuracy amplification has grown increasingly difficult. A wide variety of solutions for mitigating finite opamp gain error have been proposed, ranging from digital calibration schemes to analog techniques such as gain-boosting [1] and correlated double sampling (CDS) [2].

A particularly attractive gain enhancement technique is correlated level shifting (CLS) [3]. CLS reduces finite opamp gain error by sampling the signal at the output of the opamp during an estimation phase, and then canceling this signal from the feedback path during a second level shifting phase, leaving only the error to be processed by the opamp. The performance of CLS can be optimized by using different amplification devices for the estimation and level shifting phases. This generalization of CLS is known as Split-CLS [4] [5].

Fig. 1 shows the structure of a generalized Split-CLS architecture. The input signal is sampled during ϕ_s and amplified during ϕ_a. Within the amplification phase, the output signal is approximated during ϕ_{EST} by AMP1, and this approximation is sampled onto the level shifting capacitor, C_{CLS}. During ϕ_{CLS}, C_{CLS} is placed into the feedback path, which removes the signal from the output of AMP2, and thus from the input as well (greatly reducing finite opamp gain error). Performance is optimized by designing AMP1 and AMP2 for their differing operation requirements [5]. AMP1 needs high slew and swing but can have low accuracy and high noise, and should be able to power down at the end of ϕ_{EST}. AMP2 has much smaller slew and swing requirements, but should be high accuracy and low noise. The Split-CLS pipelined ADC presented in [6] demonstrates a successful implementation according to these optimization requirements, and achieves the best power efficiency reported to-date for any pipelined ADC. It uses ring amplification (introduced in [6]) for AMP1 and a telescopic opamp for AMP2.

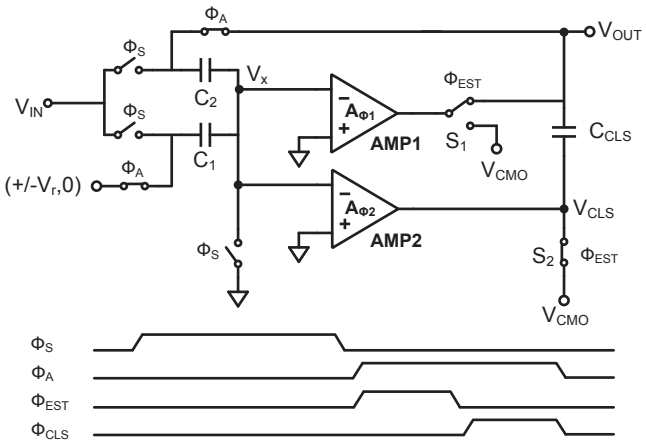

Fig. 1. The basic Split-CLS structure. An estimate of the signal is generated during ϕ_{EST} and sampled onto C_{CLS}, which is then placed in the feedback path in order to cancel finite opamp gain error during ϕ_{CLS}. The effective gain at the end of ϕ_{CLS} is proportional to $A_{\phi 1} \cdot A_{\phi 2}$.

The size of C_{CLS} affects many overall aspects of performance, sometimes in complex ways, since it influences both the feedback factor and total charging (load) capacitance of the structure. For example, decreasing C_{CLS} increases the loop bandwidth of AMP2 and reduces the total capacitance which AMP1 must charge, but also decreases the loop gain (and thus the overall accuracy) and increases the output swing requirement of AMP2. Beyond the effect of C_{CLS} on efficiency and accuracy, an important question to answer is the effect of C_{CLS} on noise requirements. The noise from AMP1 during ϕ_{EST} is suppressed by the gain of AMP2 [3], which means that AMP2 is by far the more dominant source of noise at the end of ϕ_a when the final output voltage is sampled. In this paper, we will examine the effect of C_{CLS} on the noise due to AMP2 in order to gain a better understanding of the key noise considerations unique to the design of CLS amplification.

II. Split-CLS Noise Analysis

The CLS configuration during ϕ_{CLS} is shown in Fig. 2. An equivalent signal flow diagram of Fig. 2 is given in Fig. 3. The capacitor C_P represents the lumped internal capacitances of the opamp as seen from its output. C_{LOAD} is the capacitor

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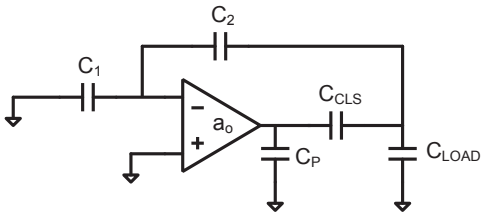


Fig. 2. CLS configuration during ϕ_{CLS} used for this analysis. Unless stated otherwise, all numerical results in this paper are found for C_1=C_2=400fF, C_P=45fF, C_{LOAD}=640fF, and a_o=58.4dB. The values for C_P and a_o are extracted from the transistor level implementation of the opamp of Fig. 4.

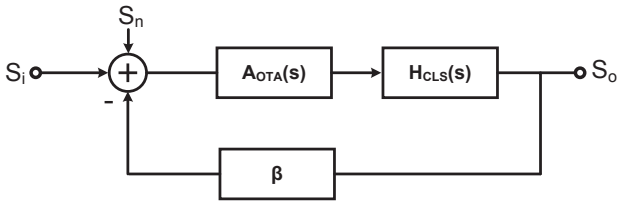


Fig. 3. Equivalent signal flow diagram for the structure given in Fig. 2

which samples the final output voltage. In this analysis we will consider a pipelined ADC, where C_{LOAD} is the sampling capacitance of the next stage MDAC and typically given by

$$C_{LOAD} = \alpha(C_1 + C_2) \tag{1}$$

where α is a stage-scaling factor. In this analysis, α is chosen to be 0.8. As with a standard MDAC, the feedback factor, β, is:

$$\beta = \frac{C_2}{C_1 + C_2}. \tag{2}$$

Furthermore, the transfer function of the CLS network is found to be

$$H_{CLS}(s) = \frac{C_{CLS}}{C_{CLS} + C_{LD}} \tag{3}$$

where C_{LD} is the total capacitance at the output of $H_{CLS}(s)$:

$$C_{LD} = C_{LOAD} + \frac{C_1 \cdot C_2}{C_1 + C_2}. \tag{4}$$

The behavior of $A_{OTA}(s)$ depends on the type of opamp used. A cascoded telescopic opamp is an ideal architecture to use for AMP2 in Split-CLS [5], and the one shown in Fig. 4 is used for this analysis. This opamp has a single dominant pole defined by its output impedance, R_O, and its total output capacitance, C_{OTA}:

$$C_{OTA} = C_P + \frac{C_{CLS} \cdot C_{LD}}{C_{CLS} + C_{LD}} \tag{5}$$

$$A_{OTA}(s) = \frac{a_o}{1 + \frac{s}{p_1}} \Bigg|_{p_1 = \frac{1}{R_O C_{OTA}}} \tag{6}$$

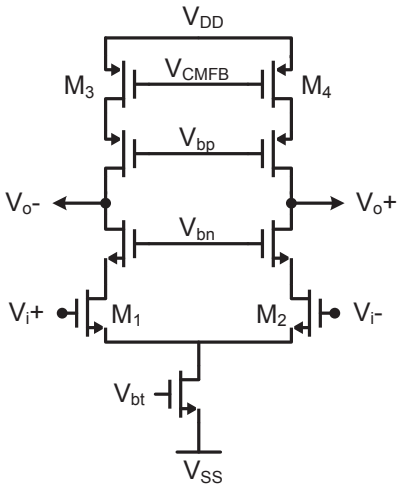


Fig. 4. Cascoded telescopic opamp used for analysis and transistor level simulation. The dominant noise sources are transistors M1-M4, which can be modeled as a single noise source at the opamp input that is filtered to the output by (6).

where a_o is the dc open-loop gain of the opamp and R_O is the opamp output impedance. The gain of the forward path for this system is

$$A_{fp}(s) = A_{OTA}(s) \cdot H_{CLS}(s) \tag{7}$$

and the noise transfer function (which is also the overall closed-loop gain of the system) is

$$H_n(s) = \frac{A_{OTA}(s) \cdot H_{CLS}(s)}{1 + \beta \cdot A_{OTA}(s) \cdot H_{CLS}(s)}. \tag{8}$$

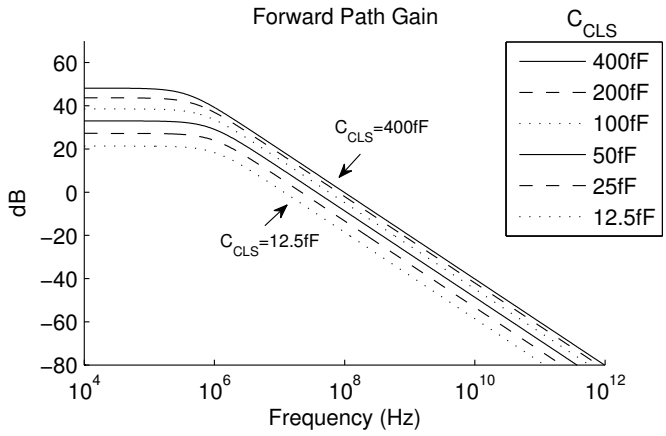
The forward path and overall gains for several values of C_{CLS} are shown in Fig. 5. In a typical feedback system, the gain-bandwidth product is a constant [1]. As Fig. 5(a) shows, this is not the case when C_{CLS} is varied. If C_P were equal to zero, the gain-bandwidth product would be constant for all values of C_{CLS} because the factor

$$\frac{C_{CLS}}{C_{CLS} + C_{LD}} \tag{9}$$

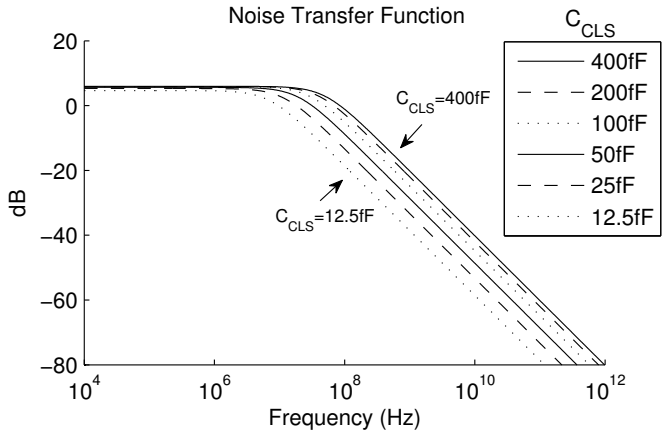
is found in both (3) (which affects the forward path gain) and (5) (which affects the pole frequency) and will cancel each other out in the gain-bandwidth product. However, because C_P only affects (5) and (6) and not (3), the gain-bandwidth product varies with respect to C_{CLS}. The effect that this dependency on C_{CLS} has on the overall noise transfer function is seen in Fig. 5(b).

In the process of designing a CLS structure, it is ultimately the degree to which C_{CLS} affects the noise sampled onto C_{LOAD} that we are interested in knowing. This integrated noise power at the output is found by passing the spectrum of the noise source through the noise transfer function and integrating the noise power:

$$\tilde{v}_{no}^2 = \int_0^\infty S_n(f) \cdot |H_n(2\pi f)|^2 \; df. \tag{10}$$



(a)



(b)

Fig. 5. Magnitude response curves for C_{CLS} ranging from 12.5fF to 400fF for C_P=145fF for a) the forward path gain described by (7) and b) the noise transfer function $H_n(s)$ described by (8). As illustrated by the bandwidth spreading seen in these figures, the gain-bandwidth product is not constant with respect to C_{CLS}.

where $S_n(f)$ is the power spectrum of the noise source.

The shape of $S_n(f)$ is not white for an opamp, including the one of Fig. 4. Furthermore, there are many noise contributors within the opamp, with each one generating noise. Different noise sources take different paths to the output of the opamp, and so the filtering of each noise source as it appears at the output must be examined on a case-by-case basis. Conveniently, for the opamp of Fig. 4, transistors M1-M4 are by far the dominant noise sources, and our analysis can be simplified to the noise contribution of only these transistors. M1-M4 are all filtered on their way to the output by (6) (or something very similar in the case of M3 and M4). For this reason, the total opamp noise can be idealized as a single noise generator at the input of the opamp, such as indicated in Fig. 3.

For most designs, the spectrum of the noise consists of two main components - white noise effects (i.e. thermal and shot noise) and low-frequency $1/f$ noise (i.e. flicker noise). For practical values used in a typical pipelined ADC, such as the values chosen in this paper, the -3dB frequency of the noise transfer function is much larger than the frequency where the

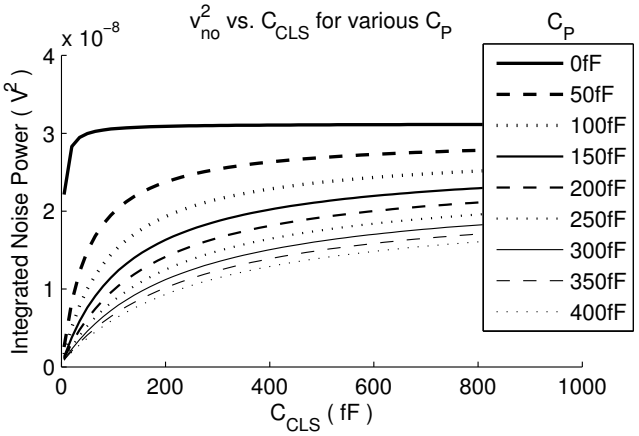


Fig. 6. The relation between opamp noise at the output and C_{CLS} is shown for many values of C_P. For most designs the condition in (13) will be true and noise will not be strongly affected by C_{CLS}.

$1/f$ noise effects cease to be a significant contributor to noise power. In this case, the shape of the low-frequency noise is unaltered by $H_n(s)$ since the magnitude response of $H_n(s)$ is flat in this frequency range; the non-white noise components manifest themselves in the final integrated output noise as a constant offset. By making these reasonable assumptions, the white and $1/f$ noise components can be separated as such:

$$\tilde{v}_{no}^2 = v_{n(1/f)}^2 + \int_0^\infty S_{n(white)} \cdot |H_n(2\pi f)|^2 \; df \qquad (11)$$

where $v_{n(1/f)}^2$ is the total integrated noise power of the low-frequency $1/f$ noise component and $S_{n(white)}$ is the noise power per hertz of the white noise component. This equation for integrated output noise is particularly convenient to use because the input noise source is expressed as two frequency-independent constants. For designs where the shape of low-frequency noise is altered by $H_n(s)$, the complete noise spectrum calculation of (10) should be used instead.

III. Numerical Results

The total integrated noise sampled by C_{LOAD} described by (11) is plotted in Fig. 6 for many values of C_{CLS} and C_P. When the condition

$$C_P >> \frac{C_{CLS} \cdot C_{LD}}{C_{CLS} + C_{LD}} \qquad (12)$$

is true, the forward path gain pole frequency is mostly defined by the fixed capacitance C_P, so the total integrated noise and C_{CLS} become correlated due to the effects considered in Section II. Likewise, when

$$C_P << \frac{C_{CLS} \cdot C_{LD}}{C_{CLS} + C_{LD}} \qquad (13)$$

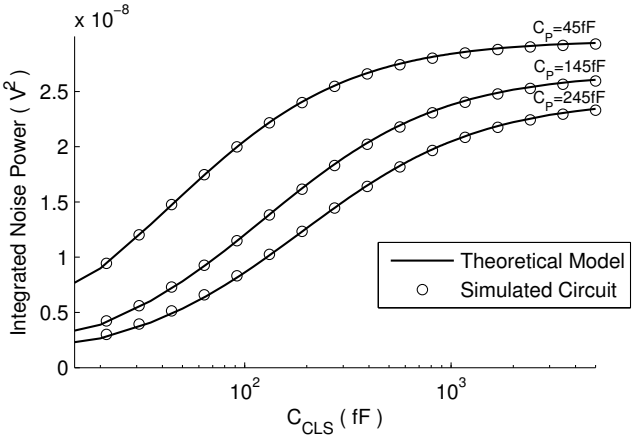
the pole frequency is most influenced by the factor in (9) and leads to little variation in the gain bandwidth product and noise. To ensure a low-swing requirement for AMP2 in Split-CLS and achieve a high level of gain-enhancement,

the value of C_{CLS} should usually be on the same order of magnitude as the values of C_1 and C_2 or larger (i.e. 400fF). Moreover, because opamp efficiency and speed is maximized by minimizing it's capacitive load, for optimum performance C_P should be minimized and consist only of the unavoidable parasitic capacitances of the opamp itself. Therefore, the region described by (13) is the most commonly encountered scenario in actual designs. The resulting implication is that for most practical designs, there will not be a strong correlation between C_{CLS} and noise sampled at the output, which simplifies the considerations a designer must make when building a CLS system.

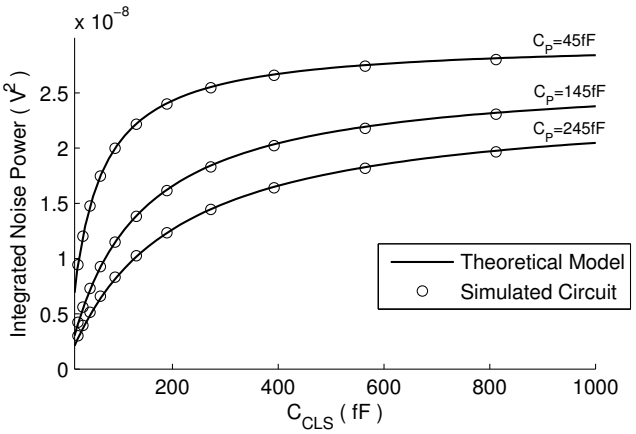
Although the derivation of this paper was made for a Split-CLS architecture, the theoretical model will not be drastically altered for most other forms of CLS, and the same key conclusions found here are also applicable in a more general sense.

IV. Comparison with Simulated Results

To verify the theoretical model derived in this paper, a transistor level simulation of the circuit in Fig. 2 was compared with theory. Shown in Fig. 7, simulated and theoretical curves are superimposed together and found to match up very closely. The three curves correspond to three values of C_P (45fF, 145fF, and 245fF), with the minimum value C_P=45fF being defined by the extracted parasitic output capacitance of the transistor level opamp in the simulation environment. The extracted transistor-level opamp DC gain of 58.4dB was used for a_o, C_1=C_2=400fF, and C_{LOAD}=640fF in both setups. For the theoretical model, the input-referred noise values $v^2_{n(1/f)} = 6.31 \times 10^{-10}\ V^2$ and $S_{n(white)} = 6.17 \times 10^{-17}\ \frac{V^2}{Hz}$ were used for all three curves. These flicker and white noise values were extracted from the transistor level opamp measured in open-loop. The noise contribution of all opamp transistors were accounted for and all other noise sources such as switches and resistors were excluded (in both theoretical and simulated results).



(a)



(b)

Fig. 7. Comparison of the theoretical model derived in this paper with transistor level simulation in a 0.18μm CMOS process using the opamp of Fig. 4 for C_P={45fF, 145fF, 245fF}. The two are compared on (a) a log scale for C_{CLS} ranging from 5fF to 5000fF, and (b) a linear scale for C_{CLS} from 5fF to 1000fF.

V. Conclusion

In this paper, an analytical model for the dominant sources of opamp noise in a CLS system has been derived. It is found that for most practical designs, there is only a weak correlation between total integrated output noise and the size of C_{CLS}. This conclusion simplifies the interaction between design variables, and allows the size of C_{CLS} to be chosen based on design parameters other than opamp noise. The theoretical model has been compared with transistor level noise simulations and found to be in excellent agreement.

Acknowledgment

The authors would like to thank Asahi-Kasei Microdevices for supporting this research.

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