# Parallel Gain Enhancement Technique for Switched-Capacitor Circuits

Hariprasath Venkatram, Benjamin Hershberg, Taehwan Oh, Manideep Gande, Kazuki Sobue[1], Koichi Hamashita[1], Un-Ku Moon

Oregon State University, Corvallis, OR, U.S.A; Asahi Kasei Microdevices, Atsugi, Japan
venkatha@eecs.oregonstate.edu

***Abstract*—This paper presents a unified classification model for gain enhancement techniques used in the design of high performance amplifiers. A parallel gain enhancement technique is proposed for switched capacitor circuits which combine the best features of the existing gain enhancement techniques found in continuous-time and discrete-time amplifiers. This technique utilizes two dependent closed loop amplifiers to enhance the open loop DC gain of the main amplifier. This replicated parallel gain enhancement (RPGE) technique enables a very high DC gain amplifier with an improved harmonic distortion performance. A proof of concept pipeline ADC in a 0.18 um CMOS process using RPGE technique achieves 75 dB SNDR, 91 dB SFDR, -87 dB THD at 20 MS/s. The measured 13 bit DNL and INL is +0.75/-0.36 and +0.88/-0.92 LSB respectively. The ADC operates from a supply voltage of 1.3 V, consumes 5.9 mW, occupies 3.06 mm$^2$ and achieves a figure of merit of 65 fJ/CS.**

## I. Introduction

Gain enhancement, distortion reduction and cancellation techniques are widely used in building high performance amplifiers. A unified gain enhancement classification chart is shown in Fig. 1. The gain enhancement techniques can be classified into *continuous*-time and *discrete*-time gain enhancement techniques. The continuous-time gain enhancement technique can be broadly classified into *parallel* [1] and *replica* amplifier [2, 3] based techniques. The discrete-time gain enhancement techniques can be classified as *sequential* and *parallel* gain enhancement techniques based on their operation and implementation. Using this classification method, we identify the advantages and disadvantages of the existing gain enhancement techniques and propose a parallel gain enhancement technique, for switched-capacitor circuits, combining the best features of the existing gain enhancement techniques.

In discrete-time switched-capacitor circuits, the gain enhancement technique is classified as a sequential technique when the measurement of gain error and its correction are performed in two different clock phases. This sequential discrete-time gain enhancement technique can be further classified into *input* and *output* based techniques based on the location of the gain error measurement (input or output) and the correction of the measured gain error (input or output). Under this classification, correlated double sampling (CDS) technique [4] will fall under sequential input based gain enhancement technique. The correlated level shifting (CLS)

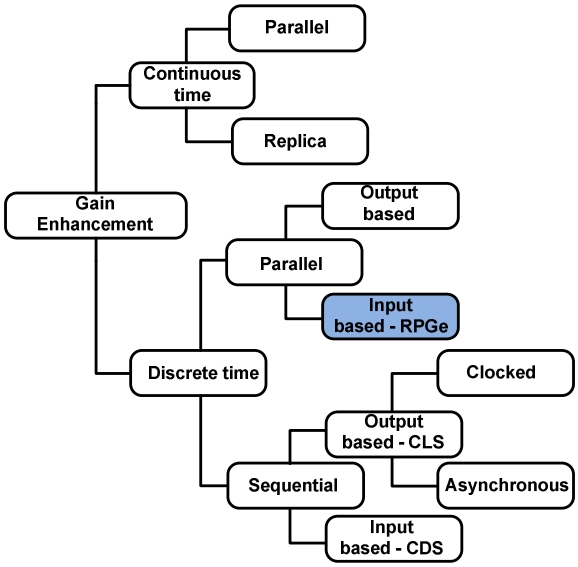


Fig. 1. Gain enhancement technique in amplifiers

and Split-CLS techniques can be classified as sequential output based gain enhancement technique [5]. The *asynchronous* sequential output based CLS technique was proposed in [6] and the parallel output based Class A+ amplifier technique was proposed in [7].

In this paper, the proposed RPGE technique is a discrete-time parallel input based gain enhancement technique for switched-capacitor circuits. Section II describes the RPGE amplifier in detail. Section III describes the high resolution pipelined ADC enabled by RPGE amplifier and Section IV concludes the paper with measurement results.

## II. Parallel Gain Enhancement Technique

The replica amplifier based gain enhancement technique [1] and the switched capacitor based CLS gain enhancement technique [5] are discussed briefly to identify their strengths and weakness.

### *A. Replica Amplifier and CLS Amplifier*

The main amplifier and the replica amplifier from [1] are shown in Fig. 2a. The replica amplifier is a scaled version of the main amplifier. The coupling transconductance supplies the majority of the output current while the main amplifier supplies only the mismatch current between the coupling transconductance current and the load current.

978-1-4673-6146-0/13/$31.00 ©2013 IEEE

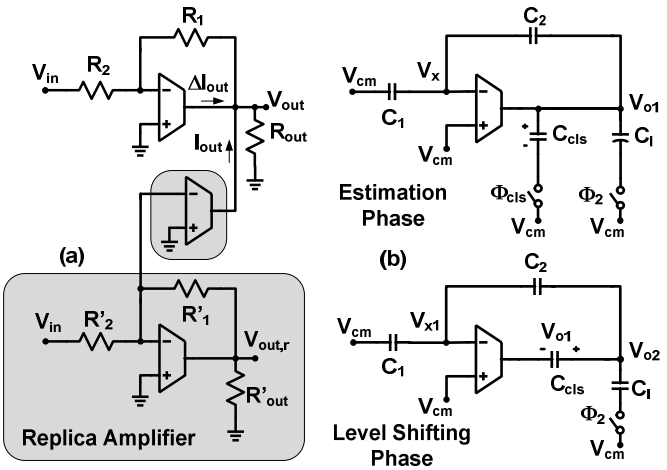


Fig. 2. (a) Replica amplifier (b) CLS estimation & level shift phase

As described above, in addition to requiring an additional amplifier, the replica amplifier technique in [1] suffers from mismatch errors between the main amplifier and replica amplifier output impedance.

The sequential output based switched capacitor technique [5], CLS, is shown in Fig. 2b. The estimation phase and the level shifting phase are shown in Fig. 2b. The equivalent loop gain at the end of the level shifting phase is approximately the product of the loop gain in the estimation phase and the level shift phase. The opamp output is closer to virtual ground at the end of level shift phase. However, this technique requires one additional phase to complete the accurate charge transfer. The $C_{cls}$ capacitor is an additional load capacitor at the output and its size in comparison to the load capacitor is an important design trade-off.

### *B. Replicated Parallel Gain Enhanced Amplifier*

The parallel nature of operation, present in the replica amplifier, transferred to a switched capacitor amplifier would enable the use of an existing two-phase non-overlapping clock, with reduced bandwidth and relaxed settling time requirement for the opamp. Also, the replicated parallel load at the input can be made very small. This important feature allows us to decouple DC-gain and output swing requirements to build an amplifier optimized for gain without the burden of swing requirement. The replicated parallel gain enhanced (RPGE) amplifier, shown in Fig. 3, combines the above mentioned benefits of reduced bandwidth, settling time requirement, conventional two phase operation, smaller replicated parallel path capacitors, decoupled DC gain and swing requirements to produce an optimized input based parallel gain enhancement amplifier. Fig. 3 shows the main loop amplifier as well as the parallel loop amplifier section in the shaded region. The gain of the main loop is set by $C_1/C_2$ and that of the parallel loop is set by $C_1'/C_2'$. When the gain of the parallel path, $C_1'/C_2'$, is made higher than $C_1/C_2$, the first stage output ($V_y$) is forced to move closer to "zero" as the parallel loop virtual node ($V_{x2}$) swing increases. This trend is illustrated for the internal node voltages, $V_y$ and $V_{x2}$, in Fig.4a.

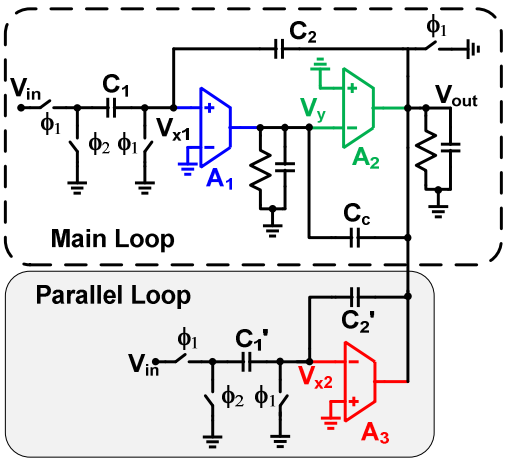


Fig. 3. Replicated Parallel Gain Enhanced Amplifier

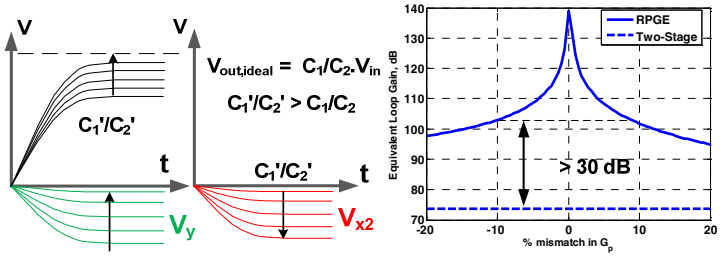


Fig. 4. (a) RPGE Trend & (b) Effective loop gain enhancement with mismatch

The improved loop gain is obtained from the gain correction/enhancement of second stage by reducing swing at node $V_y$. The equivalent open loop gain of RPGE amplifier can be made very high in theory (infinite) by selecting the appropriate parallel path gain and is limited only by the capacitor ratio precision ($C_1'/C_2'$) in a given process. In reality, with non-linear transconductance and limited precision for capacitor ratio, the gain enhancement is at least the product of main loop and the parallel loop ($A_1 \cdot A_2 \cdot A_3$). The equivalent loop gain enhancement is shown in Fig. 4b. Even with +/- 10% mismatch in the parallel path gain, set by the capacitor ratio $C_1'/C_2'$, the loop gain enhancement is at least 30 dB. This is well within the matching accuracy of the on-chip capacitor.

## III. Pipeline ADC Using RPGE Amplifier

### *A. RPGE amplifier design for a pipeline ADC*

The RPGE amplifier is an ideal candidate for the high gain, wide bandwidth and high swing amplifier required in a high resolution pipeline ADC. Fig. 5 shows a fully differential switched capacitor RPGE amplifier and a transistor level implementation using a miller compensated two-stage amplifier with RPGE amplifier embedded in the second stage. This implementation in an attractive one, among others, as it requires only switches and capacitors to implement the RPGE loop shown in the shaded region. It is instructive to note that the use of this parallel path decouples the swing at the output of the first stage of the amplifier ($V_y$) and it is less than 5 mV for the entire output voltage range of the amplifier. This allows us to design the first stage for DC-gain and bandwidth

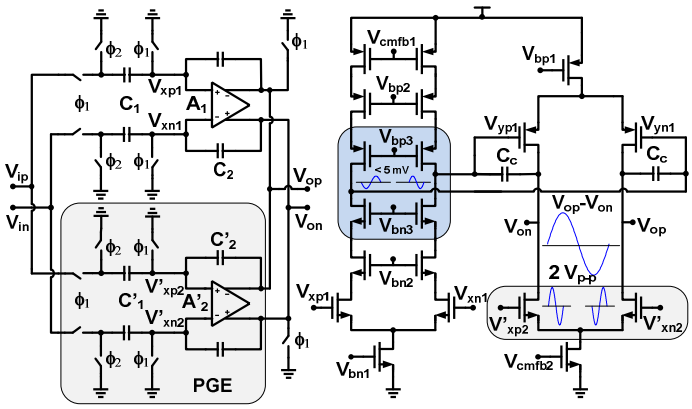


Fig.5. Switched capacitor implementation of RPGE amplifier and schematic

without considering swing requirement. Without this benefit, it would not be possible (very difficult) to double cascode the first stage for the given supply voltage. The RPGE enabled additional cascode stage is highlighted in Fig. 5.

Fig. 6 shows the effective loop gain enhancement obtained with the transistor level design in Fig. 5. The amplifier in Fig. 5 was designed for a 2.5 bit MDAC stage in a pipeline ADC with the main path closed loop gain set to $G_M = 4$ and the parallel path closed loop gain set to $G_p = 5$. Apart from the gain enhancement obtained from the parallel path, the RPGE amplifier can provide a higher output voltage swing as compared to a conventional two-stage amplifier. This is due to the push-pull nature of RPGE output stage as shown in Fig. 6. This RPGE output stage enables a class-AB like operation of second stage, which allows 50 % reduction in the output stage power consumption and area as compared to a conventional two-stage amplifier. Table I summarizes the comparison of performance parameters of a two-stage amplifier, a feed-forward push-pull two-stage amplifier, a two stage amplifier with gain boosted (GB) first stage and the RPGE amplifier. The RPGE amplifier provides the largest DC gain, swing and low distortion without additional power consumption.

### *B. 13 bit Pipeline ADC using RPGE amplifier*

To verify the above mentioned advantages, a 13-bit pipeline ADC was built in a 0.18 µm CMOS process. The pipelined ADC consists of six 2.5 bit MDAC stages followed by a 9-level flash ADC as shown in Fig. 7. The strong-arm dynamic comparator was used in the flash ADC. The main path (1st stage) sampling capacitor was 2 pF, $G_M = 4$ and the parallel path sampling capacitor was 500 fF (limited by the smallest unit capacitor in MDAC), $G_p = 5$. All six of the MDAC stages were gain enhanced by RPGE technique as shown in Fig. 7.

Table I Comparison of performance parameters

| Amplifier | DC Gain | Swing | Power | Distortion |
|---|---|---|---|---|
| Two-Stage | $A_1 \cdot A_2$ | Moderate | High | Moderate |
| Feedforward Two-Stage | $A_1 \cdot (A_2 + A_3)$ | High | Moderate | Moderate |
| GB Two-Stage | $A_1 \cdot A_2 \cdot A_{gb}$ | Moderate | High | Low |
| RPGE | $\geq A_1 \cdot A_2 \cdot A_3$ | High | Moderate | Low |

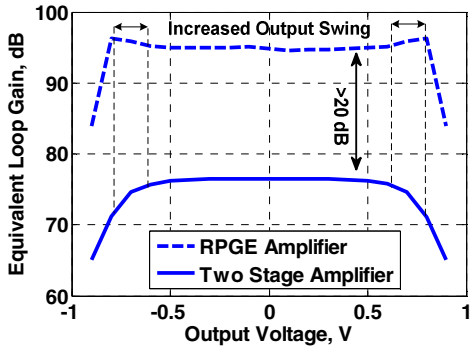


Fig. 6. Transistor level RPGE amplifier gain enhancement

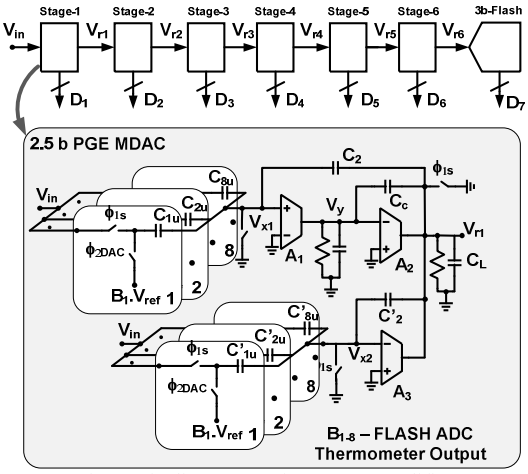


Fig. 7. Pipeline ADC using RPGE amplifier

Capacitor scaling was performed for the first four stages of the RPGE MDAC. The RPGE amplifier was also scaled down for the first four stages to maintain the same unity gain bandwidth.

## IV. MEASUREMENT RESULTS

The prototype pipeline ADC occupies 3.6 mm x 0.85 mm active area and operates at 1.3 V supply voltage at 20 MHz clock frequency. Fig. 8 shows the measured spectrum for a 1 MHz input with 20 MHz clock. As shown in Fig. 9, the measured 13-bit DNL and INL were +0.75/-0.36 and +0.88/-0.92 LSB respectively.

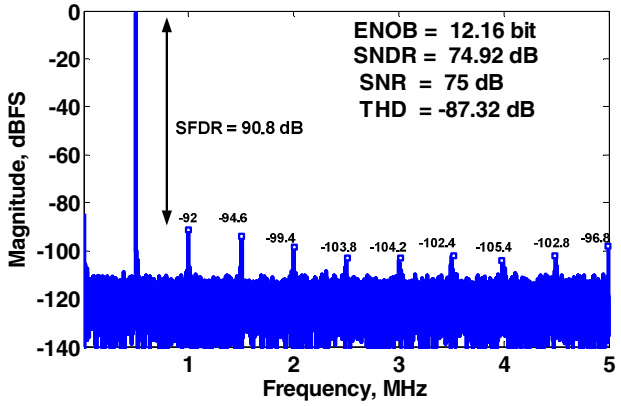


Fig. 8. Measured Spectrum at 1MHz input

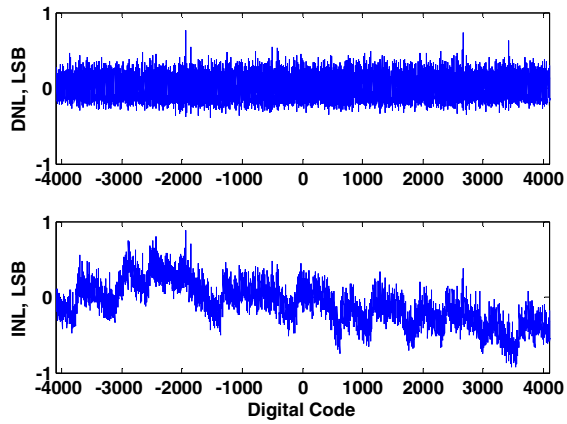


Fig.9. Measured DNL, INL at 13 bit LSB

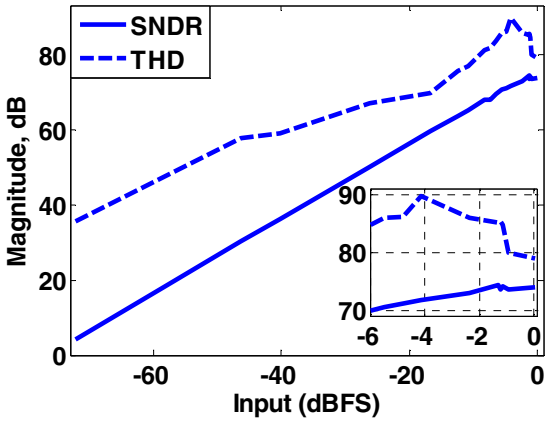


Fig.10. Input vs. SNDR and THD

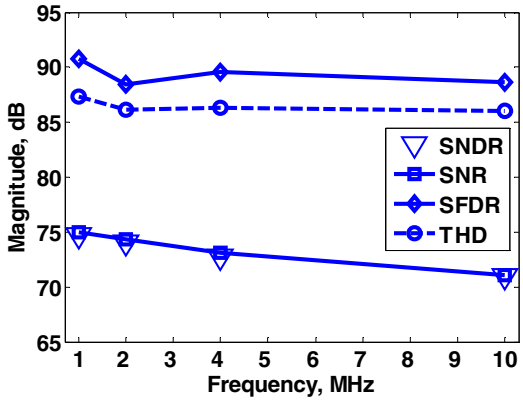


Fig. 11. Input Frequency vs. SN(D)R, SFDR and THD

The measured SNDR, SFDR and THD were 74.92 dB, 90.8 dB and -87dB respectively. The reported measurements results are without any form of calibration. The measured SNDR, SFDR and THD at 10 MHz input were 71.4 dB, 88 dB and -86 dB. The dynamic performance is shown in Fig. 10 and Fig. 11. The analog portion of power consumption was 4 mW out of the total power consumption at 5.9 mW. Fig. 12 and Fig. 13 show the die-micrograph, performance summary and comparison table respectively.

| Parameter | Value |
|---|---|
| Technology | 1P4M 0.18 μm |
| Supply Voltage | 1.3 V |
| Sampling Rate | 20 MS/s |
| Input Voltage Range | 2.4 $V_{p-p}$ |
| SNDR/SFDR | 74.9 / 90.8 dB |
| Power | 5.9 mW |
| Active Area | 3.6 x 0.85 $mm^2$ |
| FoM | 65 fJ/C-S |
| Resolution | 13b |

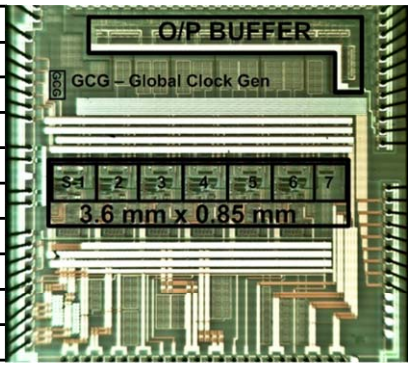


Fig.12. Performance Summary and Die Micrograph

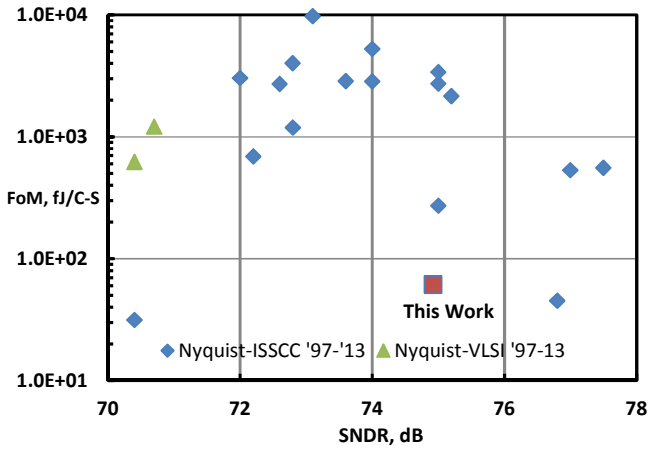


Fig. 13. Comparison to Nyquist ADC ('97-'13) > 70 dB SNDR, >5 MHz BW

## ACKNOWLEDGMENT

The authors would like to thank AKM for supporting this work and providing fabrication.

## REFERENCES

[1] P.C. Yu and H. S. Lee, "A high-swing 2-V CMOS operational amplifier with replica-amp gain enhancement," *IEEE Journal of Solid-State Circuits*, vol.28, no.12, pp.1265-1272, Dec. 1993.

[2] S. Pavan and P. Sankar, "Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique," *IEEE Journal of Solid-State Circuits*, vol.45, no.7, pp.1365-1379, Jul. 2010.

[3] J. Chen et al., "A 62mW Stereo Class-G Headphone Driver with 108dB Dynamic Range and 600μA/Channel Quiescent Current," *IEEE Int. Solid-State Circuits Conf*, pp. 182-182, Feb. 2013.

[4] C. C Enz, G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE* , vol.84, no.11, pp.1584,1614, Nov 1996.

[5] B. R. Gregoire and U. Moon, " An Over-60dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp with 30dB Loop Gain," *IEEE Int. Solid-State Circuits Conf*, pp.540-541, Feb. 2008.

[6] H. Venkatram, B. Hershberg, U. Moon, "Asynchronous CLS for Zero Crossing based circuits", *IEEE Int. Conf. Elec. Circuits Syst*., Dec. 2010.

[7] H. Venkatram, T. Oh, J. Guerber, and U. Moon, "Class-A+ amplifier with controlled positive feedback for discrete-time signal processing circuits", *IEEE Int. Symp. Circuits Syst.,* May 2012.