A 75.9dB-SNDR 2.96mW 29fJ/conv-step Ringamp-Only Pipelined ADC

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Abstract

A high resolution pipelined ADC that performs precision amplification using only ring amplifiers is presented. Several enabling techniques are introduced, namely parallelization via the use of Composite Ring Amplifier Blocks and a new ringamp topology designed for high-precision use. The 15b ADC achieves 75.9 dB SNDR and 91.4 dB SFDR at 1.2 V supply and 20 Msps conversion rate. Total power consumption is 2.96 mW, resulting in a Figure-of-Merit of 29 fJ/c-step.

Introduction

Ring amplification, recently introduced in [1], can be used to perform scalable switched-capacitor amplification with efficiencies far exceeding that of conventional opamp topologies. However, although the existing pseudo-differential ring amplifier structure of [2,3] is well suited for high-speed, medium-accuracy use, it is limited in its practical ability to provide high accuracy amplification. This accuracy limitation was overcome in [3] by incorporating a conventional telescopic opamp via Split-CLS. However, the unique power-scaling properties of ringamps imply that a high accuracy ringamp-only solution is capable of even higher efficiencies. With this in mind, we introduce several techniques used to extend the unaided use of ringamps into precision analog applications.

To briefly review, a ring amplifier (ringamp, RAMP) is constructed by splitting a ring oscillator into two signal paths and embedding a voltage offset of opposite polarity into each path (i.e. Fig. 1, top left). This creates a small input-referred dead-zone for which neither output transistor will conduct, and when operating in feedback, the ringamp rapidly charges-to, stabilizes, and then locks into this dead-zone region. Stability is created by internal finite-gain and slew-rate limiting effects that cause the peak overdrive voltage (V_{OV}) applied to M_{CN}/M_{CP} to decrease from the maximum value [1]. This V_{OV} damping effect also decreases both the output current and amplitude of oscillation, and thereby progressively feeds back to further reduce V_{OV} on subsequent cycles until the ring amplifier is stably locked.

As shown in the plot of Fig. 1, the range of input values for which stability is possible also include a small boundary 'weak-zone' region where the output still slightly conducts - under certain circumstances, the stability region can even consist exclusively of weak-zone. In such a scenario, ringamp accuracy will be limited by the structure's open-loop gain, behaving like a three stage opamp with a stabilizing output pole. Critically, the settled value of V_{OV} applied to M_{CN}/M_{CP} under these conditions is guaranteed to be very small, and the output transistors will operate in weak-inversion at steady-state. This maximizes both gain and output swing, thereby minimizing THD while simultaneously maximizing SNR. Finding a structure that fully exploits this enhancement effect is the key to unlocking efficient high-accuracy ringamp operation.

High Accuracy Ring Amplifier Structure

Shown in the bottom left of Fig. 1 is one such solution. Notably, the offset V_{DZ2} is embedded just prior to M_{CN}/M_{CP}, and allows the settled value of V_{OV} to be precisely set (and weak-zone operation to be guaranteed). However, the constraint that this places on the value of V_{DZ2} consequently limits its ability to tune stability. This is solved by observing that stability is actually determined by the input-referred value of V_{DZ2}, which can also be tuned by adjusting the gain of either the first or second stage inverter. Thus, a tunable gain-control resistor (R_{GC}) is used to set the size of the stability region. There is almost no linearity requirement for this tuned resistance, and it is implemented in this design as a simple 3-bit DAC composed of tiny MOSFET resistive elements.
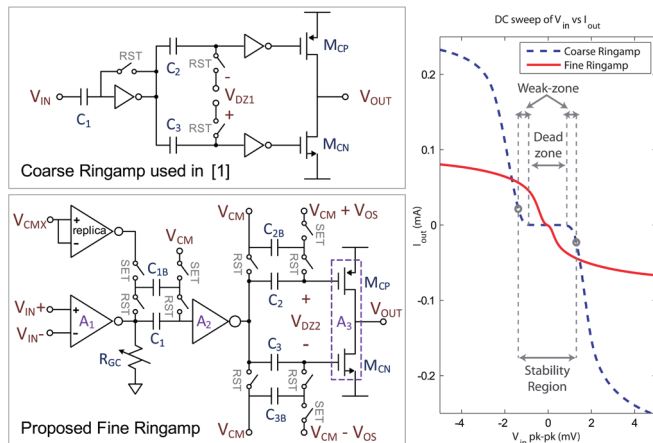

Fig 1: Simplified coarse and fine ringamp structures (left) and typical V_{IN} vs. I_{OUT} characteristic of each (right). A stability region consisting only of weak-zone ensures weak-inversion at steady-state.
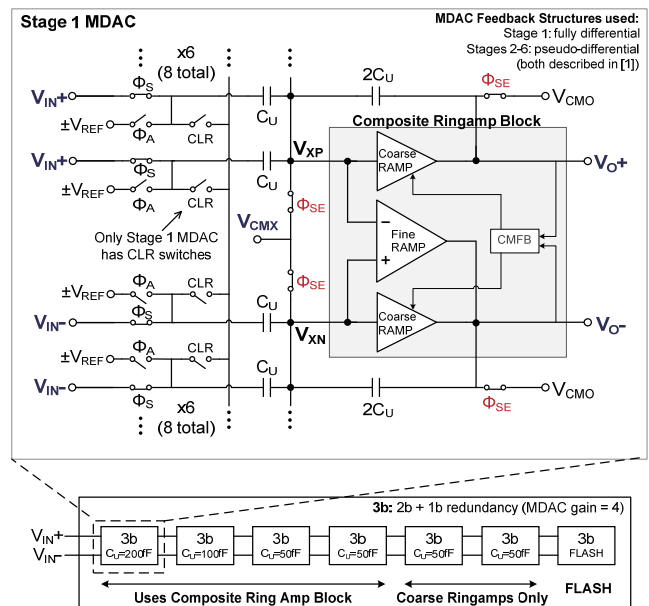

Fig. 2: Composite Ring Amplifier Block embedded within the stage 1 MDAC (top) and overall view of 15b Pipelined ADC (bottom).
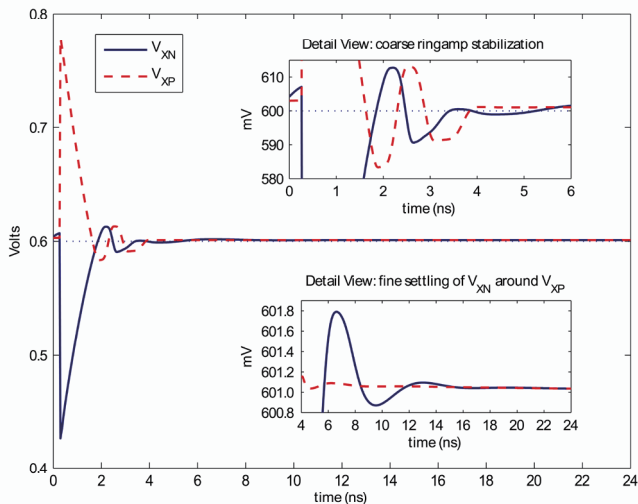
Fig. 3: Example charging characteristic of nodes V_{XN} and V_{XP} for the MDAC of Fig. 2.

Performance Summary

Resolution	15 bits		Input Range	2.4 V pk-pk diff.
Supply Voltage	1.2 V		SNDR	75.9 dB
Sampling rate	20 Msps		SNR	76.1 dB
ERBW	10 MHz		SFDR	91.4 dB
Technology	0.18μm 1P4M CMOS		ENOB	12.3 bits
Active Area	1.98mm² (3.05mm x 0.65mm)		Total Power	2.96 mW
			FoM	29.0 fJ/c-step

Fig. 4: Summary of performance and measured output spectrum.

Composite Ring Amplifier Block

The two key drawbacks of the proposed high-accuracy ringamp structure in Fig. 1 are reduced slew rate (compared to that of [2,3]) and a single-ended output. These two limitations can be removed entirely by incorporating it into a larger Composite Ring Amplifier Block. As illustrated in the switched-capacitor MDAC of Fig. 2, a coarse but fast ring amplifier is placed in parallel with the proposed high-accuracy ring amplifier. The coarse ringamp is composed of two pseudo-differentially configured single-ended ringamps (i.e. upper left of Fig. 1) coupled together via the simple capacitive common-mode feedback (CMFB) network described in [1,3].

Critically, when placed in this parallel configuration, the coarse ringamp will automatically and asynchronously cutoff and transfer control to the fine ringamp at the correct moment of operation. To understand how this is possible, consider the example charging waveform of Fig. 3. Initially, all ringamps are enabled, and contribute charge to the output. However, the coarse ringamps have a larger slewing capability and dominate the initial charging behavior, quickly settling both the differential and common-mode levels close to their final target values. As the coarse ringamps enter their dead-zone, they automatically disconnect from the output. The fine ringamp remains active, however, since its stability region (weak-zone) is necessarily quite small and thus completely enclosed by the larger stability region (dead-zone) of the coarse ringamps. With the common-mode level already settled to sufficient accuracy by the coarse ringamp's CMFB, and V_O+ floating, the fine ringamp simply settles V_O- differentially *around* a stationary V_O+. Thus, in addition to providing speed enhancement this scheme removes the need for common-mode feedback in the fine ringamp, permitting a single ended output to be used without loss of accuracy, thereby minimizing both complexity and power.

Implementation Details

The 15b pipelined ADC structure in Fig. 2 is implemented to demonstrate and characterize these techniques. The coarse ringamp and CMFB circuit is identical to that used in [3]. The fine ringamp is based on the simplified circuit in Fig. 1 (bottom left). Its input stage is a simple differential pair with R_{GC}
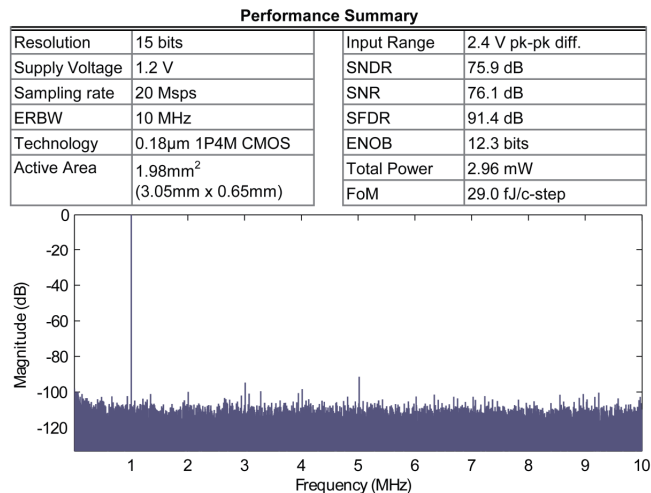
connected across its outputs. The voltage offsets stored across capacitors C_1, C_2, and C_3 must be periodically refreshed. This is accomplished with switched-capacitor charge transfer, which allows an accurate offset voltage to be programmed even when the first and second stage outputs are not completely settled. Compared to the voltage-domain approach used in [2,3], this enables much faster, more accurate offset programming. C_1 is used to remove the systematic offset caused by the difference between the common-mode output level of the first stage and the inverter threshold voltage of the second stage. This ensures that the fine ringamp's stability region will lie entirely within that of the coarse ringamp's. To save power, the fine ringamp is only enabled during Φ_A, and the coarse ringamp is only enabled at the beginning of Φ_A. An exception is during a refresh period (controlled by an on-chip counter), when both ringamps are enabled during Φ_S as well.

Measured Results

The ADC is fabricated in a 0.18μm CMOS technology. With a 1.2V supply and the MDAC references set to 0V and 1.2V, a 2.4V pk-pk sinusoidal signal is applied to the input. The resulting digital output spectrum is shown in Fig. 4, and achieves 75.9 dB SNDR (12.3 ENOB), 76.1 dB SNR, and 91.4 dB SFDR at 20 Msps conversion rate. Overall performance is fundamentally limited by kT/C noise, as predicted. Total power consumption is 2.96 mW, with 755 uW consumed by the four fine ringamps, 627 uW consumed by the six coarse ringamps, and the remaining 1.58 mW consumed by digital, switch, and quantizer blocks. The ERBW is greater than 10 MHz, yielding a Figure-of-Merit ($P_{TOTAL}/2^{ENOB} \cdot f_s$) of 29 fJ/conversion-step. A conversion speed of 20 Msps was selected for the sake of design re-use, and is by no means a fundamental limitation.

Acknowledgements

References

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