A 9.1-12.7 GHz VCO in 28nm CMOS with a Bottom-Pinning Bias Technique for Digital Varactor Stress Reduction

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***Abstract*— A wide tuning range class-B VCO in 28nm CMOS targeted for software defined radio applications demonstrates a technique for minimizing device stress while simultaneously optimizing off-state Q in digitally switched tank capacitor cells. The proposed digital varactor structure can be implemented using only capacitors and NMOS transistors, resulting in a very compact layout. The VCO operates between 9.1 - 12.7 GHz, achieving a tuning range of 32% and phase noise of -163.2 dBc/Hz at 20 MHz offset referred to a 915 MHz carrier while consuming 9.5 mW for a FoM of -187 dBc/Hz.**

I. Introduction

A core feature of CMOS technology scaling is the progressive reduction in the on-resistance of a minimum length transistor when operated as a digital switch. In the design of a wide tuning range VCO, where the parasitic capacitance of large switches limits the fundamental tradeoff between a tank capacitor's Q and tuning range, this represents an opportunity to leverage the latest CMOS technologies. However, until now it has not been possible to take full advantage of this scaling trend with existing techniques. For the conventional switched capacitor cell of Figure 1, whose core functionality is found almost universally in wide tuning range VCOs [1]–[3], a number of stress rules will be violated when native thin-oxide devices are used, especially in the off-state. In this paper, we examine an alternate digital varactor cell approach that does not suffer from these limitations (Figure 2).

The crux of the problem is illustrated by the transient waveform and amplitude growth plots of Figure 3. When EN = 0, the peak voltage at V_A and V_B will *always* exceed V_{DD} in the conventional structure of Figure 1. Although some amount of peaking above the native V_{DD} of the given technology does not significantly reduce device lifetime (since the channel of M_{SW} conducts no current in the off-state), oxide stress and impact ionization at the source/drain overlap regions still impose a fundamental upper limit on the allowable voltage swing. Although this practical constraint is not always properly addressed in experimental VCO designs (and the associated penalties avoided), for industrial designs thick-oxide transistors typically must be used [2]. Unfortunately, the use of such thick oxide devices results in greater parasitic capacitance and negates much of the potential performance advantage of scaling down into nanoscale CMOS mentioned earlier. In this paper, a simple and broadly applicable solution

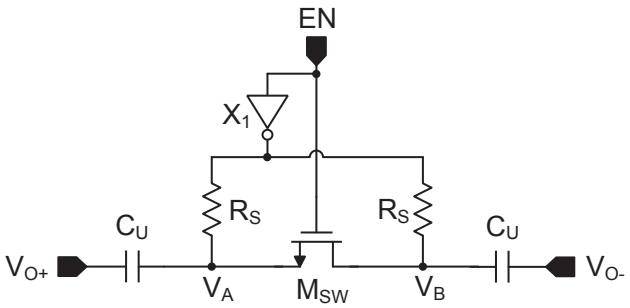

Fig. 1: The conventional digital varactor unit cell structure used in many wide tuning-range VCOs [1].

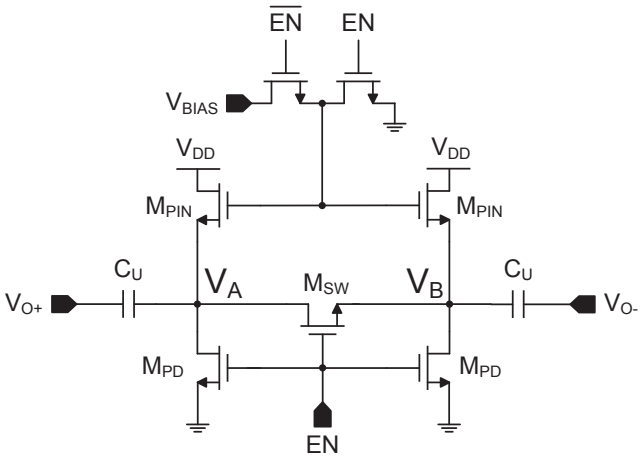

Fig. 2: Proposed digital varactor unit cell.

to this problem is proposed. We present a class-B VCO utilizing a compact NMOS-only capacitor cell that reduces device stress to an absolute minimum while simultaneously optimizing the off-state Q.

II. Capacitor Cell with Bottom-Pinning Bias

The proposed tank capacitor cell is shown in Figure 2. When EN = 1, the operation is identical to the conventional structure of Figure 1. The switch M_{SW} differentially shorts nodes V_A and V_B together and the linear capacitors C_U add to the overall tank capacitance of the VCO. The DC voltage

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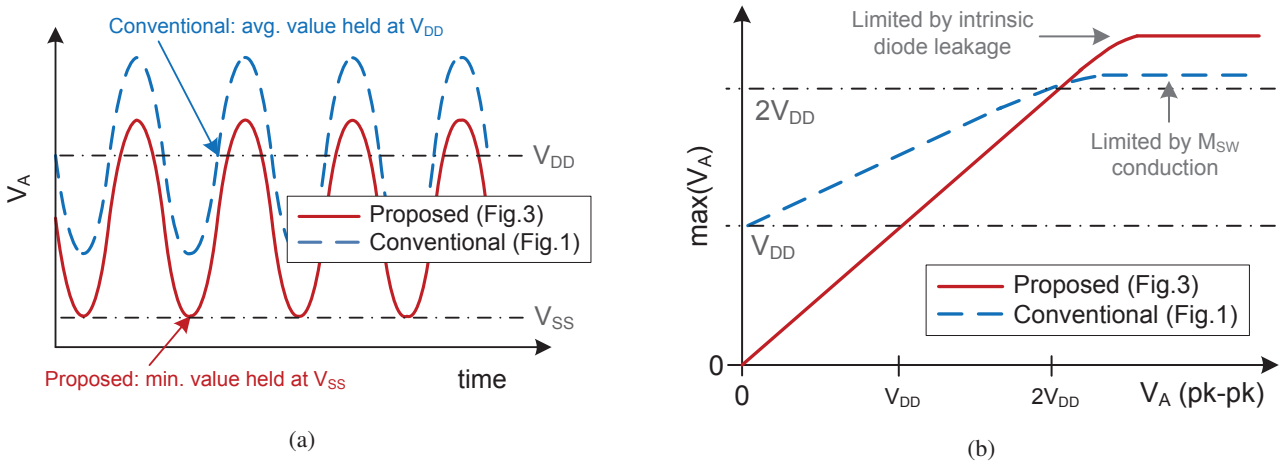

Fig. 3: Comparison of node V_A's behavior for the conventional and proposed structures: (a) transient waveform and (b) peak voltage growth characteristic. Node V_B also behaves in this way.

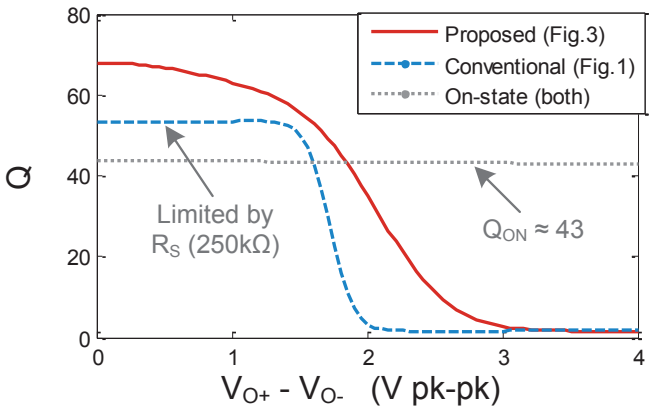

Fig. 4: Simulated off-state and on-state Qs for the structures of Figures 1 and 2.

at V_A and V_B is forced to V_{SS} by M_{PD}, and ensures the maximum conductance of M_{SW}.

When EN = 0, switch M_{SW} is open and V_A and V_B appear as high impedance floating nodes at the frequency of oscillation. In this off-state the capacitors C_U do not contribute to the overall VCO tank capacitance, except for parasitics. A slightly attenuated replica of the VCO's output waveform will thus be present at V_A and V_B. The instantaneous voltage of this floating waveform must never dip far below V_{SS}, otherwise the channel of M_{SW} would begin to conduct and degrade the Q of the cell. A conventional cell such as Figure 1 avoids this problem by using a high-ohmic connection (R_S) to set the DC level, typically to V_{DD}.

However, when we consider this minimum-voltage constraint alongside device stress constraints, it is clear that device stress will be minimized when the minimum voltage of the floating waveforms at V_A and V_B are held at V_{SS}, regardless of the amplitude. The transistors M_{PIN} of Figure 2 provide this bottom-pinning functionality. They act as floating source-followers and force the minimum voltage of the waveform (V_{MIN}) to a fixed value equal to V_{BIAS} - V_{TN}. The theory of operation can be understood by considering two possible initial conditions. In one case, when $V_{MIN} < V_{BIAS} - V_{TN}$, M_{PIN} will conduct at the bottom of the waveform and inject some charge from V_{DD} into the floating node. This will progressively raise the DC level of the floating node by some amount each period until $V_{MIN} = V_{BIAS} - V_{TN}$. In the other scenario, where initially $V_{MIN} > V_{BIAS} - V_{TN}$, parasitic conduction paths at the floating node will naturally discharge the DC level until it halts at $V_{MIN} = V_{BIAS} - V_{TN}$ as M_{PIN} begins to conduct.

Figure 3b provides a comparison of the off-state peak-voltage growth versus oscillation amplitude of the proposed and conventional cells. The proposed cell provides a large region of operation in which V_{DD} is never exceeded for small to moderate oscillation amplitudes, and then optimally minimizes stress as the amplitude grows larger. By contrast, the conventional cell exceeds the native V_{DD} for any signal amplitude, and generates comparatively more stress for all practical amplitudes.

Up to this point, we have considered a transistor with a sharp cutoff at $V_{GS} = V_{TN}$. In reality, the value of V_{MIN} will be the voltage for which the DC current entering and exiting the floating node is equal. Specifically, the current flowing from V_{DD} into the floating node through M_{PIN} must equal the sum of all parasitic leakage currents flowing out of the node. It is thus unavoidable that M_{PIN} conduct slightly. This highlights another key advantage: at steady-state, the average conductance of M_{PIN} is the exact value required to counterbalance all leakage. The result is that this structure naturally produces the highest off-state Q possible. By contrast, the series resistance R_S of Figure 1 must be chosen to ensure stable operation under worst-case leakage conditions (high-swing), which will result in a sub-optimal Q for normal leakage conditions (moderate-swing). Layout area tradeoffs further constrain the design of R_S. In nanoscale

CMOS this leakage issue is particularly relevant; the reverse-bias breakdown voltage of the intrinsic source-bulk and drain-bulk junction diodes can be as little as 1.8 V for some transistor options in 28nm CMOS, and leakage current can be on the order of several micro-amps even at 1.5 V.

A comparison of capacitor cell Q using practical design values is plotted in Figure 4 for the unit capacitor cell illustrated in Figure 5. An off-state Q $\geq$ 50 is targeted for this design. This is achieved in the conventional Figure 1 structure by choosing R_S to be 250 kΩ, which results in a peak off-state Q of 53 for the unit cell. In addition to the area penalty required to implement such large resistors, it also places a tight constraint on the amount of leakage current that can be tolerated. For example, just 2 μA of leakage current would shift the common-mode voltage down by 500 mV, causing any VCO amplitude greater than 400 mV to allow M_{SW} to accidentally conduct and significantly degrade the tank Q (assuming V_{DD} = 900 mV).

By contrast, the bottom-pinning transistors of Figure 2 adaptively control the channel resistance in order to counter-balance leakage; even if leakage degrades Q, the greater threat of M_{SW} conducting will still be avoided. It is for this reason that the slopes of the Q curves in Figure 4 under high swing conditions differ. The conventional cell has a steep Q roll-off beginning at about 1.5 V due to leakage induced common-mode droop that leads to M_{SW} to conduction. The proposed cell has a more gradual Q roll-off due to the unavoidable but increasingly large leakage currents under high-swing conditions. The pinning transistors cancel out this leakage and prevent M_{SW} from conducting.

For on-state operation, the size of M_{SW} in Figure 2 was chosen to provide a total VCO tuning range of at least 30%. The simulated on-state Q is 43 for both cells (shown in Figure 4), and reduces to 36 in post-layout extraction, with an extracted C_{ON}/C_{OFF} ratio of 3.1.

III. Class-B VCO Implementation

The well-known class-B VCO architecture of Fig. 3 is implemented in a 28nm CMOS technology. Although class-C and class-D VCOs provide higher theoretical efficiencies, the simplicity and robustness of class-B provides a good test bench for characterizing the proposed cell [3], [4]. A digital varactor utilizing ultra-low V_T thin oxide transistors provides 6-bit digital coarse frequency tuning, and an analog varactor provides fine tuning. The cross-coupled $-g_m$ transistors, M_C, see the full VCO swing and are implemented as thick oxide devices, with only a minor penalty in tuning range. A digitally tunable tail resistor can be used to trade power consumption for phase noise performance based on the requirements of the software-defined radio that this VCO is used in.

A further advantage of the cell of Figure 2 is its compact, NMOS-only implementation. As seen in the capacitor cell floor plan of Figure 5 used for this VCO design, it can be realized as a single composite NMOS block placed between the two unit capacitors. By comparison, the conventional cell uses both PMOS and NMOS transistors and a polysilicon resistor,

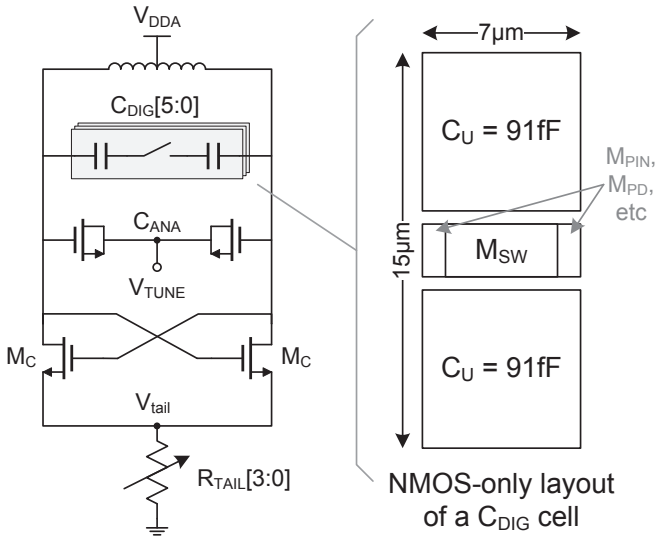

Fig. 5: Class-B VCO (left) and layout floor plan of the NMOS-only digital varactor unit cell (right).

Technology	28nm CMOS	
Active Area	0.125 mm² (500 µm x 250 µm)	
Digital Supply (V_{DD})	0.9 V	
	Efficiency Configuration:	*Phase Noise Configuration:*
Analog Supply (V_{DDA})	0.9 V	1.2 V
Power (max/min)	9.5 / 8.3 mW	20.8 / 18.4 mW
Frequency Range	9.1 – 12.7 GHz (32%)	9.0 – 12.4 GHz (32%)
f_{min} PN @ 20MHz	-163.2 dBc/Hz (w.r.t. 915MHz)	-165.2 dBc/Hz (w.r.t. 915MHz)
f_{max} PN @ 20MHz	-161.1 dBc/Hz (w.r.t. 915MHz)	-161.8 dBc/Hz (w.r.t. 915MHz)
FoM (max/min)	187.0 / 184.4 dBc/Hz	185.4 / 182.8 dBc/Hz

Fig. 6: Measured performance for high efficiency and low phase noise modes of operation.

which cannot be abutted. This layout, in conjunction with the inherent density scaling of a nanoscale CMOS process, yields a layout area of only 117 μm x 15 μm for the 15 element thermometer plus 2 element binary C_{DIG} array of Figure 5.

IV. Measured Performance

The prototype VCO, fabricated in a 28nm 9M digital CMOS process, occupies 500 μm x 250 μm. For testing purposes V_{BIAS} of Fig 2 is provided by an off-chip reference. In future implementations, on-chip biasing can easily be implemented, since V_{BIAS} requires neither high-accuracy nor very low-noise and has an optimal value that depends only on V_{TN}. For example, a simple diode-tied NMOS current mirror with a small bias current would provide a near-optimal bias voltage for the bottom-pinning transistors.

A summary of measured performance is tabulated in Figure 6 for both a high efficiency and a low phase noise mode of operation. In the high efficiency configuration, the measured phase noise at 20 MHz offset is -163.2 dBc/Hz

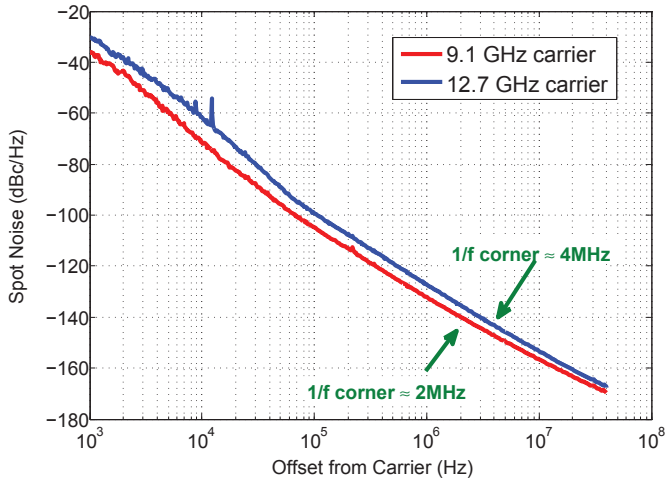

Fig. 7: Phase noise at min and max operating frequencies for the high-efficiency operating mode tabulated in Fig. 6.

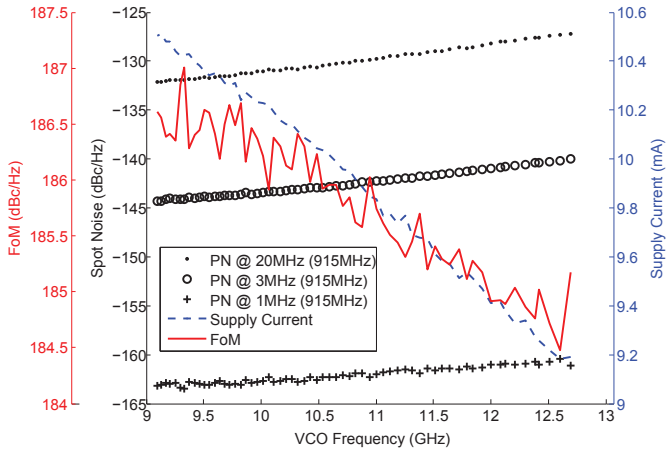

Fig. 8: Performance versus frequency for the high-efficiency operating mode tabulated in Fig. 6.

(at 9.1 GHz carrier referred to 915 MHz) with a FoM of −187.0 dBc/Hz while consuming 9.5 mW. The VCO operates between 9.1 GHz and 12.7 GHz with a tuning range of 32%. Analog tuning is available via an accumulation-mode varactor with a minimum tuning range of 100 MHz at 9.1 GHz. The phase noise spectrum at the maximum and minimum oscillation frequency is given in Figure 7. A higher than expected $1/f$ noise corner degrades spot noise at 20 MHz offset-from-carrier by approximately 2 dB. It was determined that this high 1/f noise corner is due to a limitation of the transistor noise modeling, and the core transistors (M_C of Figure 5) need to be made larger in future implementations to account for this uncertainty.

For the low noise configuration tabulated in Figure 6, the phase noise at 20 MHz offset is −165.2 dBc/Hz (at 9.0 GHz carrier referred to 915 MHz) with a FoM of −185.4 dBc/Hz while consuming 20.8 mW. Performance is sufficient for SAW-less operation across all major wireless standards.

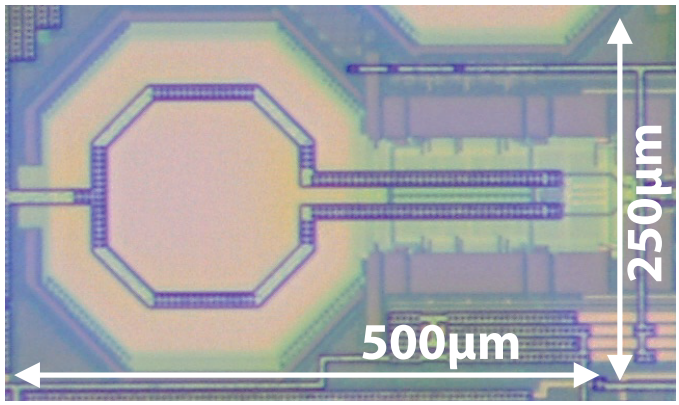

Fig. 9: Die micrograph.

	Area (mm^2)	Frequency (GHz)	PN @ 20MHz from 915MHz (dBc/Hz)	P_{DC} (mW)	FoM (dBc/Hz)
Fanori, ISSCC 2012	0.39 (55nm)	6.7-9.2 (32%)	-169	27	188/189
Liscidini, ISSCC 2012	0.49 (55nm)	6.5-9.0 (33%)	-168	36	185
Visweswaran, ISSCC 2012	0.19 (65nm)	7.3-8.0 (10%)	-170	25.8	190
Dal, JSSC 2010	0.06 (65nm)	13-15 (15%)	-162	8.4	185
This work	0.13 (28nm)	9.1 – 12.7 (32%)	-163	9.5	187

Fig. 10: Comparison to other state of the art cellular TX VCOs with $f_{min} \geq 6$ GHz.

In Figure 10 the VCO is compared to other state-of-the-art VCOs operating with similar center frequencies and tuning ranges. This VCO compares favorably in all key metrics of area, tuning range, and power efficiency, especially when considering the Class-B topology and the flicker-noise problems discussed here that can be improved in future implementations.

V. Conclusion

The digital varactor cell presented in this paper provides the best possible operating conditions for thin-oxide switches, and can be broadly applied to improve the performance and reliability of many VCO architectures, both in nanoscale CMOS and otherwise. It is implemented in a compact NMOS-only layout and can be biased with a simple current mirror.

Acknowledgment

The authors would like to thank L. Pauwels, the imec BODI team, and Integrand Software.

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