A 9.2–12.7 GHz Wideband Fractional-N Subsampling PLL in 28 nm CMOS with 280 fs RMS jitter

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***Abstract* — This paper describes a fractional-N subsampling PLL in 28 nm CMOS. Fractional lock is achieved by using a 10bit digital-to-time converter (DTC) that generates a delayed sampling clock with minimal impact on PLL performance. Background calibration guarantees appropriate DTC gain, reducing spurs. The system achieves −38 dBc of integrated phase noise (280 fs RMS jitter) at 10 GHz when a worst-case fractional spur of −43 dBc is present. In-band phase noise is at the level of −104 dBc/Hz. The class-B VCO used can be tuned from 9.2 GHz to 12.7 GHz (32%). The total power consumption of the synthesizer, including the VCO, is 13 mW from 0.9 V and 1.8 V supplies.**

***Index Terms* — Phase locked loops, phase noise, sampling, fractional-N, frequency synthesis, jitter.**

I. Introduction

Frequency synthesizers receive increasing attention from both the RF community, where they serve as LO sources for up/downconversion and the digital community, where low-jitter clocks are critical. In particular, digital PLLs have been pushing performance boundaries from one year to another. However, the analog subsampling PLL that appeared in [1] has until now been unbeaten in terms of integrated phase noise (or RMS jitter) amongst all CMOS frequency synthesizers. The comparatively large phase detection gain of this architecture improves in-band phase noise and, thanks to that, allows for wide bandwidths. At the same time, power consumption can be reduced thanks to divider-less operation. However, an architecture-inherent integer-N operation prevents the adoption of this approach in practical wireless transceivers. Within the fractional-N PLLs, the all-digital systems (for example [2], [3]) show potential of achieving performance similar to the subsampling PLL, although often at the cost of large power consumption of the time-to-digital converter (TDC).

In this paper we present a method which allows the subsampling PLL topology to be used for fractional-N operation. By adapting the sampling timings to match the zero-crossings of the VCO output, the subsampling operation is maintained for any fractional multiplication and the phase noise improvement thanks to subsampling architecture is retained.

The architecture of the fractional-N PLL is shown in Fig.1. Similarly to the original subsampling PLL [1], the system features two loops, where one provides frequency acquisition and the second one maintains phase-lock. Phase detection is done in essence by a switch and a capacitor and the charge pump/transconductor can be very simple. Thanks to the high detection gain, the noise of any of these circuits does not impact the overall system performance.

II. Fractional-N operation of a subsampling PLL

The integer-N subsampling PLL of [1] operates by sampling the (differential) VCO sinusoid with a repetition rate set by the reference frequency. In a phase-locked state the sampling happens precisely at the zero crossings of the differential sinewave. Any deviation from the timing of the zero crossing results in a non-zero voltage being sampled, which in turn is converted to a correction current fed to the loop filter. Since the VCO zero crossings are aligned to the reference, the VCO produces a frequency which is an exact integer-N multiplication of the reference.

There is no divider in the subsampling loop and, therefore, the classical method of applying a $\Delta\Sigma$ stream to modulate the division ratio and enable fractional-N operation is not possible. Another technique known from digital PLLs, where a TDC is used to measure the phase delay between the reference and the VCO is not applicable either, because the subsampled phase correction information lies in the amplitude of the sampled voltage and not in its phase.

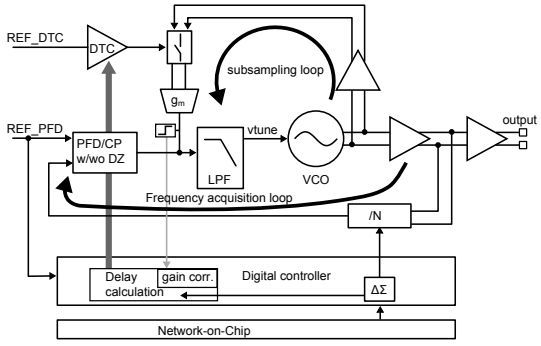

Fig. 1. Architecture of the fractional-N subsampling PLL.

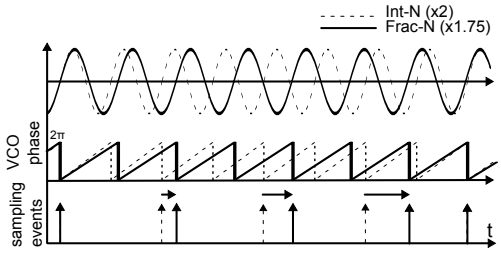

Fig. 2. Implementation of fractional-N subsampling operation by delaying the sampling reference. The last sampling event is a start of a next cycle and has no extra delay.

A possible solution to this problem is illustrated in Fig.2. If we compare an integer-N VCO waveform with a (simple) fractional-N one, we see that the zero-crossings in time move away from the original sampling events. If we can delay the sampling event to match the required positions of zero crossings of the VCO, we will achieve fractional-N phase lock.

For example, let us take a fractional-N frequency that is different from integer-N by 0.25, as in Fig.2. Let us assume that in the first cycle we will sample at the same time as in the integer-N mode. Then, in the second cycle we sample 0.25*Tvco later, in the third cycle 0.5*Tvco later, then 0.75*Tvco later. Finally, in the fifth cycle, we should sample 1*Tvco later, however, we recognize that simply skipping a VCO cycle is going to yield the same effect, thus we sample at the integer-N time. Critically, since we know the required PLL frequency and the reference frequency, we can calculate the position of any following zero crossings with absolute precision. This means that if we could implement an ideal delay generator, the PLL would be completely spur-less, unlike the traditional analog $\Delta\Sigma$ PLL. Additionally, the tuning range of the delay generator only needs to cover one VCO period, since the calculations "wrap around" as in the aforementioned example.

III. System architecture and circuit design

The proposed PLL consists of two phase-locked loops: a traditional $\Delta\Sigma$ loop based on a phase-frequency detector (PFD) and a subsampling loop. The PFD-based loop is used to track frequency as the subsampling loop can only track phase and can lock to any multiplication of the reference. After the frequency acquisition is complete, the PFD loop is automatically deactivated thanks to a half-period deadzone introduced on purpose in the PFD [1]. In fact, once the subsampling loop is phase locked, the PFD-based loop can be disabled, saving power.

The PFD-based loop is a classical implementation with CMOS VCO buffers driving a first CML divide-by-2/3 stage, that is followed by a programmable CMOS divider. The divider is followed by a deadzone-enhanced PFD and a simple charge-pump. Thanks to the fact that this loop is not critical in terms of phase noise or spurs, the components can be low-power and as small and simple as possible.

The subsampling loop uses a capacitive attenuator and a source-follower-based VCO buffer in order to reduce kickback effects and adjust voltage levels, at the same time preserving the sinusoidal shape of the VCO waveforms. The buffer is followed by twin NMOS-based samplers, each operating at a different phase of the reference clock [4]. The total sampling capacitance is around 20 fF. Finally, a transconductor stage converts the differential sampled voltage to current that is fed into the 3rd-order passive lead-lag LPF (with a total capacitance of 106 pF). The output current of the transconductor is pulsed in order to reduce the loop gain [1]. The transconductor and the charge pump of the PFD-based loop operate from a 1.8 V supply to match the tuning curve of the analog varactor that was available in the design kit. Depending on the supply and settings of the VCO, the optimal tuning point of the VCO can move from around 0.7 V to 1.5 V.

The digital-to-time converter (DTC, see Fig.3) operates on the reference signal of the complete PLL and, therefore, its phase noise performance is critical. For acceptable overall performance the DTC must add minimal amounts of jitter to the delayed clock. We implemented a single-ended reference path based on inverters, however, to increase immunity to supply-induced spurs, the parts of the DTC that operate asynchronously to the reference clock use a simple regulated supply. This regulated supply is based on a programmable current source and diode-connected transistors charging a large (4 pF) capacitance that further conditions the supply of the DTC. The DTC delay is generated by a tunable RC network, where the capacitance can be programmed to 10b resolution with an LSB step of 3 fF. Although the discharging curves of an RC network are exponential, the delay at a fixed threshold due to tuning of capacitance is linear. However, the slopes of the discharge are rather slow, so large inverters serve as comparators to regenerate the actual DTC output.

The VCO is a thick-oxide NMOS cross-coupled core with current limiting realized using a tunable resistor. The VCO has been designed to meet the stringent GSM900 specification for out-of-band phase noise. Digital tuning is realized using a bank of NMOS-only switched capacitor cells. The simulated Q of the tank reaches 18. The VCO is designed to operate with an LDO (not present on chip) with a supply between 0.9 V and 1.5 V, depending on the required phase noise performance and available power.

The complete system is driven by a digital controller which computes the sequence of DTC codes representing the correct delays required to match the wanted PLL frequency. These calculations are done based on a $\Delta\Sigma$

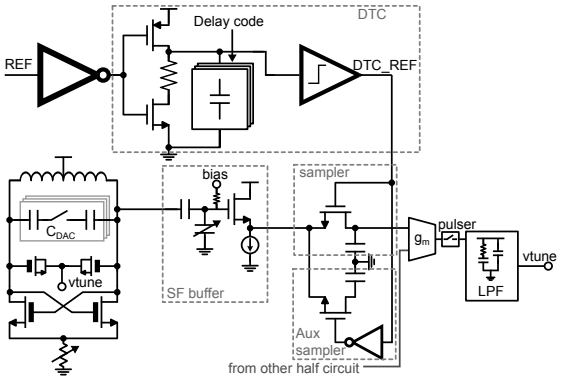

Fig. 3. Simplified schematic of the subsampling loop.

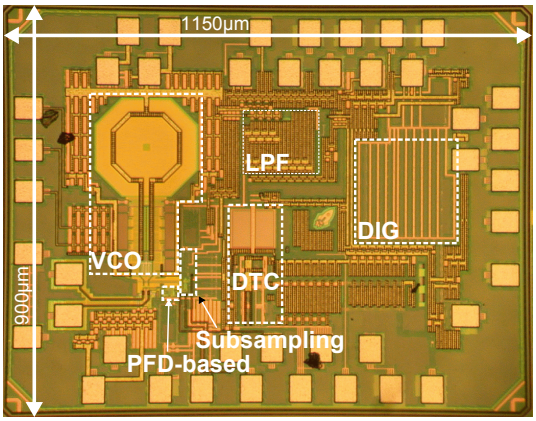

Fig. 4. Chip microphotograph.

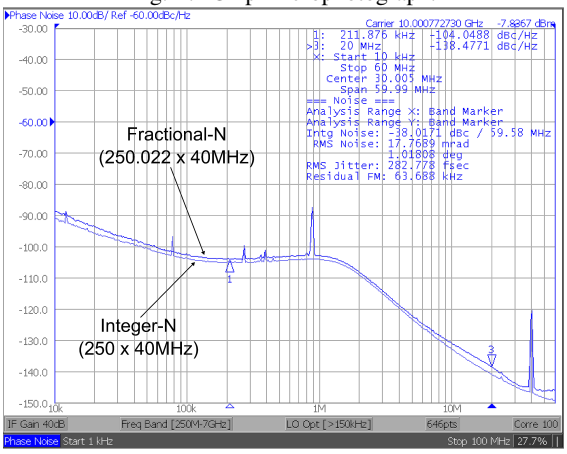

Fig. 5. Measured phase noise for a worst-case fractional-N scenario. For reference, the integer-N phase noise trace is shown as well.

modulator which also directly drives the frequency divider of the PFD-based loop. This modulator can work in either 1st-order mode or in MASH 1-1 and MASH 1-1-1 modes. To obtain DTC codes the error of the $\Delta\Sigma$ stream is accumulated and scaled by a constant $T_{ref}/(LSB_{DTC} \cdot N_{frac})$. In the higher order $\Delta\Sigma$ modes the DTC generates delays larger than a single VCO period and the neighboring VCO zero crossings are sampled. This helps to de-color the output spectrum in a way similar to how the classical $\Delta\Sigma$ PLLs work. As the DTC delay is based on RC delays, it is susceptible to PVT variations: any gain (LSB_delay/code) variations generate additional fractional spurs and $\Delta\Sigma$ leakage will increase in-band phase noise. Therefore, a background digital calibration is present in the controller that correlates the change of the DTC code and the sign of the current flowing to the LPF (which, apart from offset, is equivalent to the sign of the sampled voltage). After accumulation, this data scales the DTC codes as an online gain adjustment that reduces spurious content.

IV. Experimental Results

The PLL was manufactured in 1P9M 28 nm bulk digital CMOS technology and occupies an area of 1 mm^2 (Fig.4). It is powered by 0.9 V and 1.8 V supplies. The 1.8 V supply is used for the IO interface, the charge-pump and the transconductor stage. Power consumption (excluding the 50 Ω output drivers and powering down the PFD-based loop) is 13 mW, where the DTC and transconductor consume 0.5 mW and 0.6 mW, respectively, the VCO and the source-follower VCO buffer 9 mW and the digital controller 2.5 mW. The digital controller was not optimized for power and includes additional testing circuitry that cannot be clock-gated.

The VCO frequency tuning spans from 9.2 GHz to 12.7 GHz with sensitivity to analog voltage that reaches 200 MHz/V around 10 GHz.

Oscilloscope measurements of the DTC show INL and DNL of less than 1.8 LSB and 0.8 LSB, respectively. The nominal time resolution is 550 fs.

Phase noise was measured using an Agilent E5052B signal analyzer with an external downconverter. A sample phase noise result around a carrier frequency of 10 GHz showing the fractional-N spectrum with the worst-case spur (880kHz) is shown in Fig.5. For comparison, the integer-N phase noise is visible as a memory trace, showing little degradation in the fractional-N mode. The in-band (200 kHz) phase noise reaches −104 dBc/Hz in fractional-N mode. The integrated phase noise in fractional-N mode spans between −40 dBc and −38 dBc depending on the fractional number. In integer-N mode it reaches −41 dBc. Phase noise integration was done from 10 kHz to 60 MHz and includes all spurs. No compensation or correction was applied to the system, apart from the online DTC gain correction. The PLL is working in a MASH 1-1-1 mode. Due to underestimated loop gain, the bandwidth cannot be made smaller than 1.8 MHz what worsens the integrated phase noise and jitter. However, this design is a starting point to a modulating TX PLL, where the large bandwidth is an advantage. Settling time (20 MHz step) is below 2 µs.

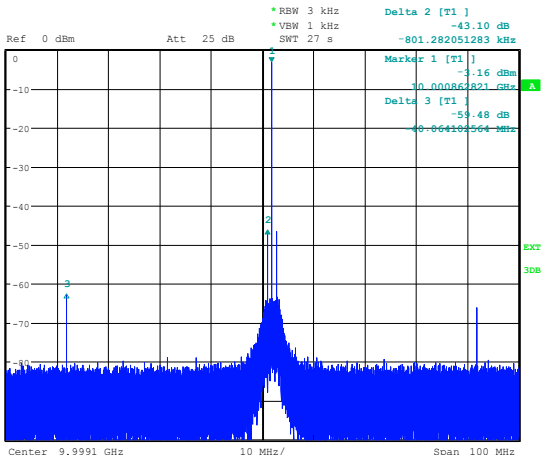

Fig. 6. Output spectrum of the PLL showing worst-case fractional spur and reference spur.

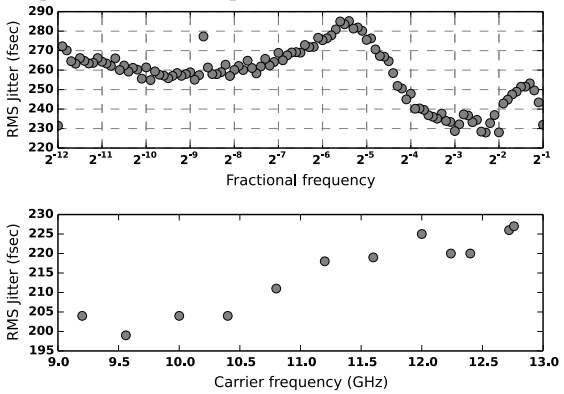

Fig. 7. RMS jitter over a fractional code and integer-N jitter over VCO tuning range.

Spurious response was measured using a Rohde&Schwartz FSQ26 spectrum analyzer and is shown in Fig.6. The worst case in-band fractional spur is −43 dBc. The spur is believed to be caused by the non-regulated supply of the VCO. In high power mode, with much smaller supply sensitivity, the fractional spur drops by approximately 10 dB. The reference spur is −60 dBc.

Jitter was extracted from the integrated phase noise and is shown versus fractional codes in Fig.7. With out-of-band fractional multiplication, the RMS jitter reaches 230 fs. When working in integer-N mode, the synthesizer achieves RMS jitter of only 204 fs.

V. Conclusions

We propose a fractional-N subsampling PLL reaching 280 fs of RMS jitter in worst-case fractional spur scenario and 204 fs in integer-N mode while consuming 13 mW. An inverter-based DTC is used to modulate the sampling clock of the PLL to enable fractional-N operation with almost no penalty on phase noise. Compared to state-of-the-art synthesizers (see Table I) and to our knowledge, this is the lowest phase noise analog fractional-N synthesizer to date. The inband phase noise level of −104 dBc/Hz challenges state of art of all fractional-N synthesizers.

TABLE I
Performance summary and comparison with other low-jitter fractional-N CMOS PLLs.

	This work	[5]	[6]	[2]	[3]
Type	**Analog**	Analog	Analog	Digital	Digital
Technology	**28nm**	180nm	180nm	65nm	55nm
Freq (GHz)	**9.2 - 12.7**	2.2 - 2.4	2.5 - 3.2	2.9 - 4.0	5.9 - 8.0
Ref. freq (MHz)	**40**	48	33	40	40
BW (MHz)	**1.8**	0.5	0.2	0.3	0.5
In-band PN[2] (dBc/Hz)	**-104**	-99.2	-89	92.5	-103
PN@20MHz[3] (dBc/Hz)	**-138**	-128	-139	-128	-144
RMS jitter (fs)[3]	**230 – 280**	266 – 400	455	560	190
IPN (dBc)[2,3]	**-39.8 – -38.1**	-38.5 – -35.0	-34.8	-32	-41.5
Worst frac spur	**-43**	-53	-74	-42	-70
Reference spur	**-60**	-55	-78	-72	-94
Power (mW)	**13**	17.3	48	4.5	36
FoM[4]	**-241.5 – -240**	-239.1	-230	-238.5	-239

[1] Scaled to 10 GHz by $20\log(\frac{f_c}{10\,\mathrm{GHz}})$
[2] Scaled to 10 GHz and extrapolated from existing data to 20 MHz offset
[3] Including spurs
[4] $FoM = 10\log((\frac{\sigma_t}{1\,\mathrm{s}})^2 \cdot \frac{Power}{1\,\mathrm{mW}})$

Acknowledgments

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