An Electrical-Balance Duplexer for In-Band Full-Duplex with <-85dBm In-Band Distortion at +10dBm TX-power

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***Abstract* — When using electrical-balance duplexers (EBDs) to provide RF self-interference cancellation for in-band full-duplex, in-band distortion produced by nonlinear CMOS switches in the duplexer cause distortion that limits the headroom for additional self-interference cancellation in subsequent cancellation schemes in the transceiver. A prototype EBD is fabricated in 0.18µm SOI CMOS to investigate the dynamic range limitations of a transceiver architecture for next-generation wireless systems that supports in-band full-duplex and legacy FDD. Measurements show -85dBm in-band distortion at +10dBm TX input power, enough for short-range links at 10MHz BW.**

***Index Terms* — In-band full-duplex, electrical-balance duplexer, multi-tone test, self-interference, cancellation.**

I. Introduction

In-band full-duplex (FD) operation not only offers the potential to double the available channel capacity [1], but also has many benefits on the MAC level, such as collision avoidance and energy efficiency [2]. Backwards compatibility with FDD is imperative for mass-market reception.

Electrical-balance duplexers (EBDs) are recently investigated as a way to provide an integrated frequency-agile alternative for surface acoustic-wave (SAW) duplexers in frequency division duplexing (FDD) applications [3]. The concept of the EBD is to *balance* the antenna impedance with a balance network impedance (Z_{BAL}), as seen at the ports of a hybrid junction. In contrast to filters based on frequency selectivity, an EBD can pass signals between transmitter (TX) and antenna, and receiver (RX) and antenna, while concurrently providing cancellation of self-interference (SI) originating from the local TX, all *at the same frequency* (Fig. 1). Therefore, EBDs are also attractive to provide self-interference cancellation (SIC) for *in-band* FD, directly at the RF antenna interface [4].

In fact, EBDs offer the opportunity for a single transceiver (TRX) to switch between FD and FDD, provided enough subsequent SIC can be achieved for FD. E.g., additional SIC could be implemented in the analog/digital baseband (ABB/DBB) or in an additional loop directly at RF. A unified, frequency-flexible, single hardware could support both FD and FDD.

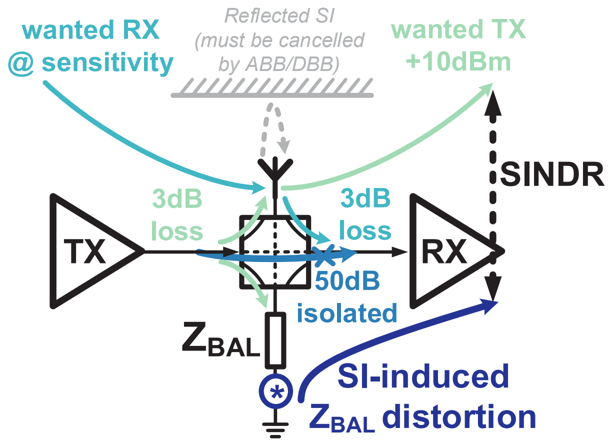

Fig. 1. An (ideal) electrical-balance duplexer enables RF SIC for in-band FD through TX-RX isolation and TX/RX signal transfer to/from the antenna, all at the same *time* and *frequency*.

This paper investigates an FD/FDD architecture that combines an EBD for RF SIC with a vector modulator (VM) canceller [5] as a second cancellation stage in the RX analog baseband and a third cancellation stage is implemented in the digital baseband [1].

To allow post-EBD SIC, including cancellation of delayed SI-components resulting from environmental reflections, the EBD must have high in-band linearity *and* SIC. In other words, low SI-induced distortion at the RX output *relative* to the SI power at the antenna is critical. That is, the EBD must achieve a high self-interference to noise-and-distortion ratio (SINDR) [5], while noise is less significant for the RX output signal to noise-and-distortion ratio (SNDR).

At moderate TX power, in-band distortion produced by the CMOS switches in the balance network of the duplexer (Z_{BAL}) can limit SINDR. Because Z_{BAL} distortion is not present in the reference copies used for subsequent SIC loops, it cannot be cancelled further down the RX chain. So, a very linear EBD is required for FD operation.

This paper uses the electrical-balance duplexer of [3] to demonstrate the limits of in-band FD. In-band distortion measurements show that ≤100dB of total SINDR is feasible for a transmit power up to +10dBm, enough for FD links up to ~100m at 10MHz bandwidth (BW).

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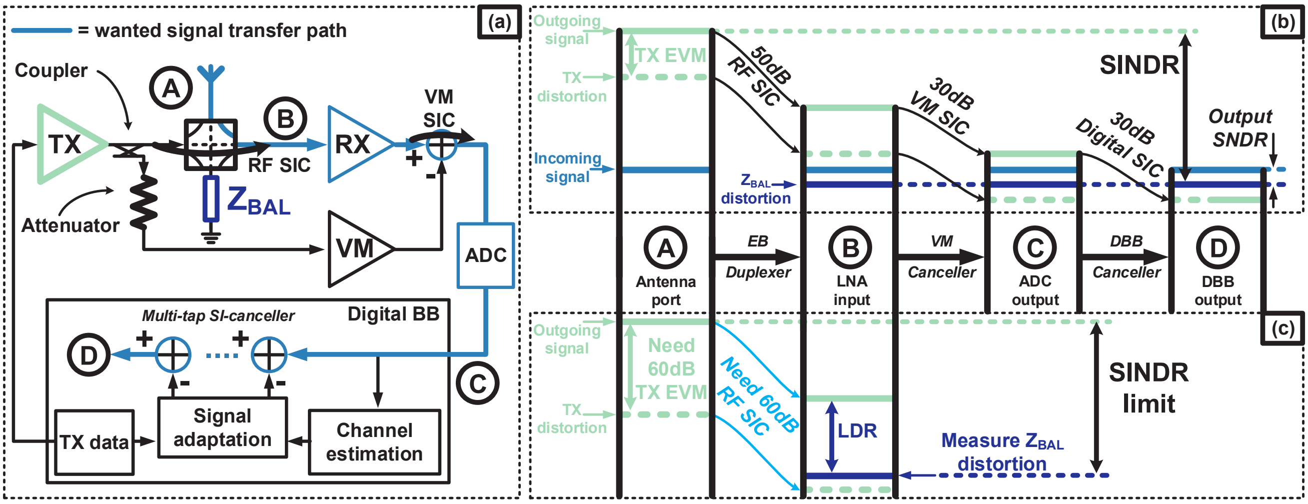

Fig. 2. Proposed architecture including digital BB (a), level diagram for the proposed architecture (b) and level diagram for distortion measurements presented in this paper (c).

II. Proposed Architecture and Level-Diagram

Fig. 2(a) shows the proposed three-stage SIC architecture with an example DBB implementation. It includes an electrical-balance duplexer for RF SIC, a VM canceller for ABB SIC and a multi-tap SIC solution in the DBB. Fig. 2(b) shows the level diagram at the nodes A, B, C and D of the architecture, as indicated in Fig. 2(a):

A. The antenna, with the TX noise and distortion assumed to be 30dB below the TX signal (TX EVM). The wanted signal level is far lower than the SI and distortion.

B. The EBD RX output, where the SI (TX) has been reduced by 50dB RF SIC, and distortion generated by the balance network Z_{BAL} is added.

C. The RX ADC output, after the analog SIC using a VM canceller [5], which can ideally lower both the TX leakage and TX distortion by an addition e.g. 30dB. However, the VM canceller cannot reduce the Z_{BAL} distortion and the wanted signal is still lower than the remaining SI.

D. The DBB output, where a final cancellation stage is implemented in the DBB to achieve e.g. 30dB SIC. It reduces the (known) TX leakage to similar levels at the TX distortion, for example by channel estimation [1], but cannot cancel distortion due to its inherent linear nature. Assuming that Z_{BAL} distortion is low enough to provide an acceptable output SNDR as in Fig. 2(b), the wanted signal can now be detected.

Fig. 2(c) shows the level diagram for the measurements done later in this paper. Without a VM in the measurements, it was found that the Z_{BAL} distortion may still be lower than the remaining TX distortion of an actual modulated signal, such that 60dB RF SIC and 60dB TX EVM is required to observe Z_{BAL} distortion. In the EBD, we achieve 60dB RF SIC by reducing the signal BW.

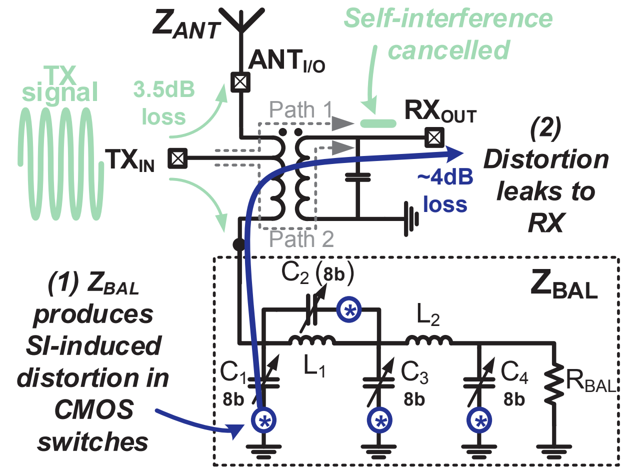

Fig. 3. Single-ended electrical-balance duplexer schematic [3], illustrating distortion generation in Z_{BAL}.

The TX power level is reduced to increase TX EVM. Then, as shown in Fig. 2(c), if the TX EVM is larger than the (linear) SI leakage-to-distortion ratio (LDR), Z_{BAL}-generated distortion is observed.

Critically, between 50 and 60dB of RF SIC, the Z_{BAL} distortion level at the EBD RX output *does not change*, since the TX-to-Z_{BAL} insertion loss and Z_{BAL}-to-RX insertion loss remains constant in both cases. Therefore, the measurement results give valuable information about normal operation, even when measured with a reduced bandwidth and at an increased RF SIC level.

The primary objective of this paper is to demonstrate that Z_{BAL} distortion exists and poses a limit to the achievable SINDR. To demonstrate this, the most linear (>+70dBm IIP3) EBD reported to date is used (Fig. 3) [3].

III. In-Band Distortion Measurements

The duplexer was fabricated in a 1P5M IBM 0.18μm SOI CMOS process, measuring 1.75mm^2, and bonded to a test-PCB [3]. Fig. 4 shows a chip photograph. A 50Ω termination is connected to the antenna port as a reference impedance. Since this dummy load impedance does not radiate (it only dissipates the TX signal), it is guaranteed that no SI resulting from environmental reflections is present and the observed in-band distortion could only originate from either the TX or the duplexer.

Fig. 5 shows the measured TX-to-RX transfer in the EBD versus frequency: 2MHz BW is achieved for 60dB attenuation, 10MHz for 50dB and 36MHz for 40dB. To observe the Z_{BAL}-generated in-band distortion, measurements are performed using a narrow BW on the order of several kHz to ensure at least 60dB SI suppression is achieved.

For these tests, a Keysight E8267D is used to generate a set of (N=4,8,16,32) tones with random phases at 1kHz tone spacing using a 1.875GHz carrier. A Minicircuits ZVE-8G+ power amplifier (+30dBm OP_{1dB}) emulates a typical PA, while a R&S FSW26 spectrum analyzer with pre-amp measures the spectrum of the TX and the duplexer (after reconnection). The TX input power is swept from -10 to +24dBm. The first tone to the right of the center frequency is *disabled* to allow observation of in-band distortion levels.

In order to emulate the distortion profiles that will arise in modulated signals as much as possible, a multi-tone instead of a simpler two-tone is used, such that many different orders of harmonics contribute at the missing tone frequency when a large amount of tones are used. A multi-tone ensures capturing sufficient orders of harmonics.

The in-band distortion relative to the in-band TX leakage power at the antenna port (TX EVM) and at the RX output (LDR) was measured, and the difference is used to illustrate the duplexer-added Z_{BAL} distortion.

Fig. 6 shows one of the measured spectra at the antenna and at the duplexer RX output at the same Y-scale to clearly show that Z_{BAL} distortion is added by the duplexer. This is confirmed by observing the TX EVM, which is 59dB, and the LDR, which is 45dB. Since the difference is positive (14dB), Z_{BAL}-induced distortion is demonstrated. TX EVM and LDR are estimated using the *average* power at three frequency points: in-band at the missing tone frequency, and at the two neighbors of the tone-sets. At these points, the number of tones causing intermodulation is assumed representative of the whole channel [6].

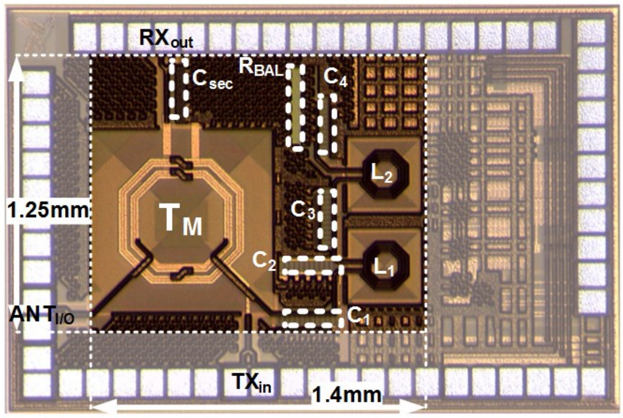

Fig. 4. 0.18μm SOI CMOS chip photograph.

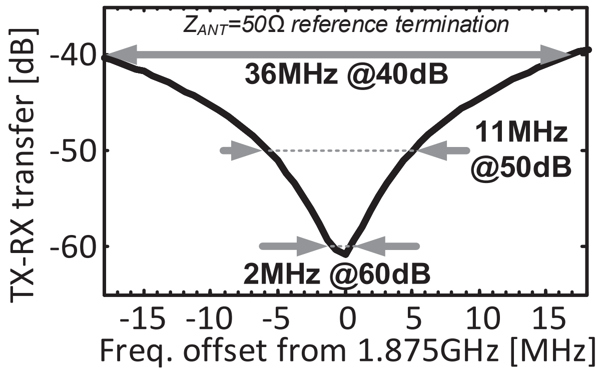

Fig. 5. Measured TX-RX transfer of the duplexer versus frequency offset from the 1.875GHz center.

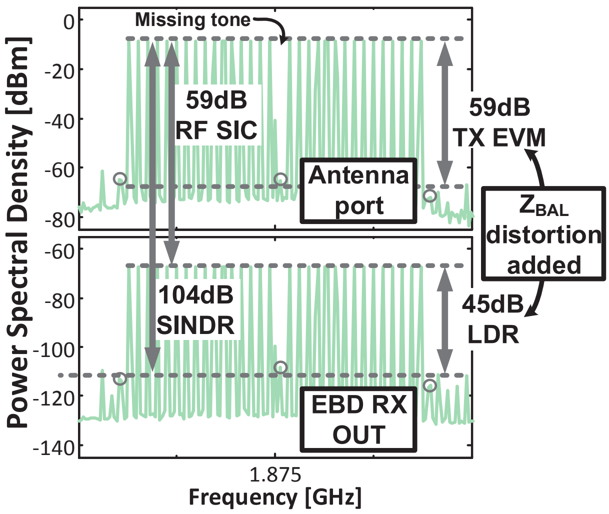

Fig. 6. Measured 32-multitone PSD for +10dBm TX input power: at the antenna port (top) and after RF SIC at the duplexer RX output (bottom). The tone spacing is 1kHz.

Fig. 7 illustrates how the EBD linearity performance varies with the SI input power for N=32. The spectrum analyzer noise floor limits SINDR at low SI power (<0dBm) before Z_{BAL} distortion comes in (<19dBm) and finally TX EVM dominates distortion (>20dBm), with SINDR = P_{SI} @ant. – In-band distortion @EBD RX out.

Fig. 8 shows TX EVM–LDR for N=4,8,16,32, where the EBD limits the dynamic range of the measurement setup since LDR<TX EVM. To measure Z_{BAL} distortion beyond >20dBm, a more linear TX would be needed.

Fig. 9 shows a peak SINDR of 112dB at 0dBm TX power and average 100dB SINDR up to +7dBm, for the same measurements as Fig. 8 (for all N).

These results imply the proposed architecture enables FD wireless links of around 100m with 10MHz BW, for ~15dB RX output SNDR at 0dBm to +7dBm TX power for <7dB total RX NF (incl. EBD loss) and assuming that the DBB can remove SI caused by environmental reflections. Finally, the TRX could switch to long-range FDD mode at full +27dBm TX power at the antenna.

IV. Conclusions

This paper uses an EBD to investigate the dynamic range limitations of a transceiver architecture for next generation wireless systems that supports in-band full-duplex and legacy FDD.

In-band distortion measurements of a fabricated EBD prototype show <-85Bm in-band distortion at +10dBm TX power, enough for short-range FD links at 10MHz BW.

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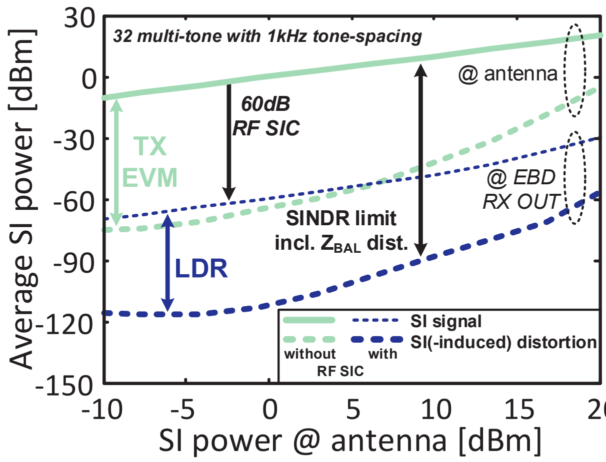

Fig. 7. Measured EBD linearity performance for FD (N=32).

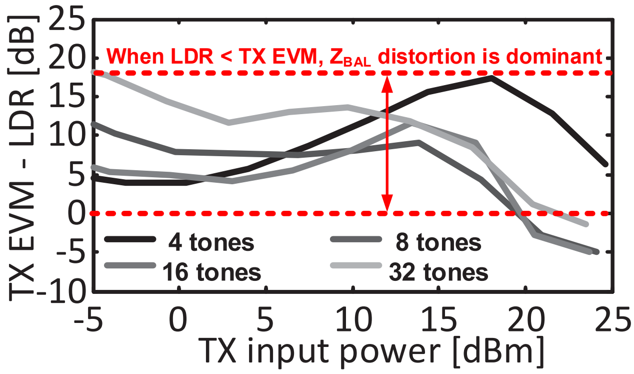

Fig. 8. Measured difference between TX EVM and the LDR at the duplexer RX output for N=4,8,16,32.

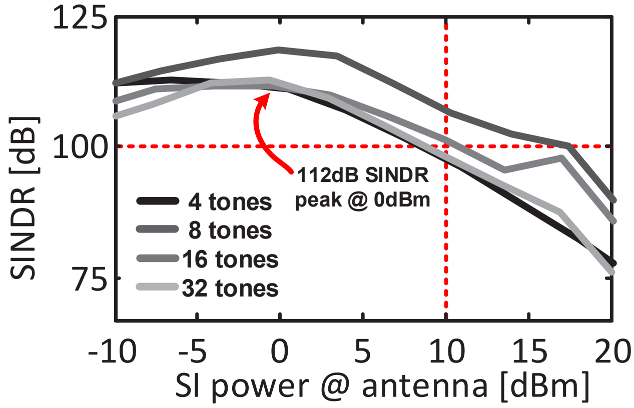

Fig. 9. Measured maximum SINDR that the system can achieve due to SI(-induced) distortion for N=4,8,16,32.

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