In-Band Full-Duplex Transceiver Technology for 5G Mobile Networks

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Abstract — **In-band full-duplex is a promising air interface technique to tackle several of the key challenges of next generation (5G) mobile networks. Simultaneous transmission and reception in the same frequency band increases the throughput and spectral efficiency, and reduces the air interface delay. Its implementation in 5G systems, however, restrains the full-duplex transceiver design requirements. Two analog integrated circuit solutions are presented and evaluated in the frame of 5G applications. The first design is a self-interference cancelling front-end implemented in 65nm CMOS, and the second design is an electrical-balance duplexer implemented in 0.18μm RF SOI CMOS. Both designs are attractive in the context of 5G; they allow dense integration, are configurable to support alternative and legacy standards, are compatible with conventional antenna(s), and they provide an attractive full-duplex performance for wireless communications.**

Index Terms — **In-band full-duplex, 5G, self-interference, analog/RF cancellation, integrated circuits, RF-IC.**

I. INTRODUCTION

NEXT generation (5G) mobile networks target to sustain the evolution of mobile communications in terms of connectivity, throughput and spectral efficiency while enhancing the user experience. To sustain this evolution, new technologies are being analyzed and developed. In-band full-duplex (IBFD) wireless communications is considered as a promising air interface technique for 5G as it tackles key issues such as throughput, spectral efficiency, latency and connectivity [1]. The IBFD concept involves that a wireless terminal is allowed to transmit and receive simultaneously in the same frequency band. The IBFD concept has been successfully validated for both the network and the physical layer [2][3], and puts additional requirements on the transceiver hardware. As 5G targets mass-market adoption, commercially attractive IBFD transceivers should be:

- compact and support dense system integration,
- implementable in low-cost mass-production technology,
- reconfigurable to support several communication schemes and backward compatibility (e.g. time division duplexing (TDD) or frequency division duplexing (FDD)),
- compatible with in-system and/or legacy components (e.g. commercial off-the-shelf components).

These additional requirements suggest compact integrated circuit solutions rather than e.g. using dedicated full-duplex antenna structures with specific dimensions, radiation patterns and polarizations [3][4]. These integrated circuits should operate with conventional antenna(s) used for legacy communications schemes.

This paper first introduces the main challenges for 5G systems and identifies the synergy in combination with IBFD wireless communications. Then, the main issue limiting the IBFD performance, self-interference (SI), is discussed for different transceiver architectures. Finally, two IBFD integrated analog circuit solutions are presented and evaluated. The first design is a SI- cancelling front-end implemented in 65nm CMOS [5][6], and the second is an electrical-balance duplexer implemented in 0.18μm RF SOI CMOS [7]. These solutions operate with a simple antenna structure providing a low initial isolation, and with a conventional single-port antenna respectively. Both solutions offer good levels of SI-cancellation, but should be completed with analog cancellation to achieve a total SI-cancellation requirement of 90-100dB for a typical indoor link budget [8] and to cancel multi-path reflections.

II. FULL-DUPLEX CONCEPT MEETS 5G CHALLENGES

The rapid growth of mobile communication and massive advances in technology are setting the ground for introducing 5G as the next step in the evolution of mobile communication systems. The 5G challenges in respect to radio system performance can be illustrated with the EU FP7 METIS project objectives to develop technical solutions towards a 5G system concept that supports (compared to 3G/4G mobile communication systems in 2012) [9]:

- 1000 times higher mobile data volume per area,
- 10 to 100 times higher number of connected devices,
- 10 to 100 times higher user data rate,
- 10 times longer battery life for low power massive machine communication, and finally,
- 5 times reduced end-to-end latency.

To achieve these extremely challenging targets, radical changes in the network architecture and significant developments in the air interface technologies are needed. Demand for very wide transmission bandwidths calls for seeking new spectrum in higher frequencies above 10 GHz. Support for higher bit rates and high number of connected devices in frequency bands below 6 GHz calls for novel

solutions to improve spectrum efficiency and flexible use of spectral resources.

IBFD operation sets high requirements on the transceiver implementation due to SI phenomena (i.e., the transmit signal leaking into its own receiver), but when successfully solved, it provides significant improvements to wireless systems operation [10]. Enabling wireless terminals to operate in full-duplex transmission mode offers the potential to double their *spectral efficiency*, i.e. the numbers of transmitted bits per second per Hz. IBFD operation can also provide more *flexibility in spectrum usage*. The same frequency resources can be used for one directional or bi-directional transmission. IBFD operation can complement legacy systems based on TDD or FDD. Beyond spectral efficiency and physical layer, full-duplex concepts can be advantageously utilized in higher layers, such as at the access layer. IBFD operation can *reduce air interface delay* due to simultaneous reception of feedback information (control channels, signaling related to error correction protocol, etc.) while transmitting data. IBFD capable terminals could *detect collisions* while transmitting data and also resolves the 'hidden node' problem, both typical issues for contention based networks. Thus, IBFD operation promises to enable various 5G mobile network targets [1].

III. IN-BAND FULL-DUPLEX TRANSCEIVER ARCHITECTURES

Figure 1 shows an IBFD link with a local and remote transceiver node. Each node has one antenna for the transmitter (TX) and one for the receiver (RX). In this link, three sources of SI limit the proper reception of the signal coming from the remote node by the local RX. First, leakage can occur on-chip or on-board (type A in Figure 1). Such direct cross-talk is likely to occur with dense integration. Second, line-of-sight leakage or spillover between the two antennas may occur (type B in Figure 1). This SI is generally reduced by implementing antenna structures with specific radiation patterns or polarizations. Finally, TX signals may be reflected on nearby objects back into the receive antenna (type C in Figure 1). Such multipath refection typically result in frequency-dependent SI.

The self-interference caused by the different paths can be cancelled by copying reference signal(s) in the TX chain and subtract the modified reference signal(s) in the RX chain. This modification involves attenuation and phase shifting to cancel the frequency-independent SI and additional signal delaying to cancel the frequency-dependent SI. As shown in bottom figure of Figure 1, the SI cancellation can be realized from various points in the transmitter chain to various points in the receiver chain. Therefore, different architectural options exist.

Using the TX signal close to the antenna as a reference is beneficial as it contains most information: the signal, any in-channel TX imperfections such as TX-generated noise and distortion, as well as any gain and phase imbalance across the channel that the signal has experienced through the TX chain. If, for example, the TX reference would be copied before the power amplifier (PA), the (dominant) PA-nonlinearities cannot
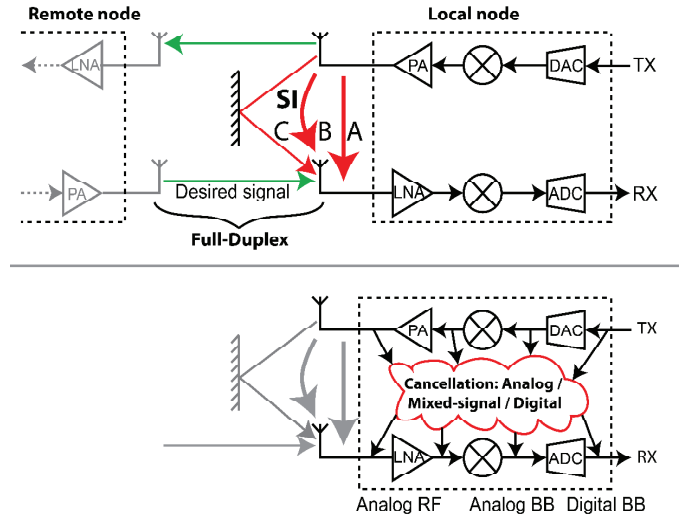

Figure 1: Top: full-duplex radio is subjected to different self-interference paths. . Bottom: self-interference cancellation can be realized from various points in the transmitter chain to various points in the receiver chain.

be cancelled using that particular reference copy. Similarly, cancelling the SI early in the RX chain is beneficial, because it relaxes the RX front-end linearity and large-signal handling requirements, as well as the required analog to digital converter (ADC) resolution. These architectures indicate the importance of implementing SI cancellation as close as possible to the antenna. But implementing additional SI cancellation at digital baseband remains essential, mainly to cancel the frequency-dependent SI. The physical dimensions of RF delay elements namely hamper dense integration, whereas this can be efficiently implemented in the digital domain.

The next section discusses two circuit implementations which address two architectural options: (1) a SI-cancelling front-end which copies the post-PA signal and subtracts it at baseband frequencies, and (2) an electrical-balance duplexer, which also copies the reference post-PA, but cancels directly at RF. Both circuits provide cancellation before the first RX amplifier stage, for type-A and type-B SI (Figure 1). These architectures should be completed with digital cancellation, but such techniques exceeds the scope of this paper.

IV. SELF-INTERFERENCE CANCELLING CIRCUITS

In this section, two transceiver designs are discussed which respectively build on a simple antenna structure and a conventional single antenna. These designs target dense integration in modern CMOS technology. The presented designs comply with the targeted analog SI requirement of 40-60dB for typical link bandwidths in indoor environments [3], while relying on digital cancellation to suppress reflections and realize a complete full duplex system. Both designs are highly reconfigurable and may support other communication schemes such as FDD and legacy TDD.

A. A self-interference cancelling front-end

The self-interference cancelling front-end architecture presented in [5] adds analog SI-cancellation to a simple

antenna structure with a low initial isolation (~20dB).

As shown in Figure 2, the SI-cancelling path takes a copy of the transmitted signal at RF through a fixed attenuator. The attenuator value sets the maximum strength of the cancellation path to correspond to the worst-case isolation expected from the antenna solution. Subsequently, a variable phase shift and attenuation is applied, the signal is downmixed and the resulting signal is subtracted in the analog baseband before any amplification. The main advantage of this architecture is that phase shift, attenuation and downmixing is efficiently combined in a single structure: a *vector modulator (VM) downmixer*. Figure 3 shows a simplified implementation of the RX with such a VM downmixer. Essentially, both the VM and the main RX mixer are 4-phase switched resistor mixers which maintain high linearity under large SI powers. The VM is a sliced version of the main RX mixer, incorporating multiplexers in each slice that steer the 4-phase output current to the appropriate baseband phases.

This front-end has been implemented in 65nm CMOS and covers an area of 2mm² only. A SI-cancellation of 27dB was measured over a bandwidth of 24MHz, however, since a real SI channel will not be frequency flat due to reflections from the environment, the bandwidth is limited in practice. Indoor experiments using a crossed dipole antenna pair at 2.5GHz showed that the 27dB cancellation can be maintained over ~16MHz bandwidth [5]. Based on its RX noise and distortion performance, the design allows for up to 42 dB of digital cancellation, for a total link budget of up to 42+27+20 = 89dB over 16MHz bandwidth. This is sufficient for short-range links at moderate transmit powers. The 27dB cancellation in the analog domain relaxes requirements on low noise amplifier (LNA) and ADC dynamic range and on TX fidelity to feasible levels [5][6].

All mixers in the prototype are clocked from the same clock, which contributes to the phase noise immunity in full-duplex mode [6]. If we want to use this front-end for FDD, the clocking needs reconfiguration. Conventional TDD operation is possible by simply disabling the SI-cancelling vector modulator, which eliminates the noise of the cancellation path, reducing the noise figure from about 10-12dB to 6dB.

The design has a very broad operational frequency range covering 0.15-3.5GHz, including the co-integrated TX [6]. The cancellation and noise performance remain intact over this wide RF range. Its versatility in operation frequency, universal two-port antenna interface and capability of working with only 20dB initial isolation brings IBFD closer to the realm of 5G hand-held devices.

B. An electrical-balance duplexer

In contrast to the architectures shown in Figure 1 and Figure 2, an alternative architecture uses a conventional single-port (e.g. miniature SMD) antenna in conjunction with a duplexing device to separate the transmit and receive signal. The electrical-balance duplexer [10][7] for simultaneous transmission and reception is depicted in Figure 4. Traditionally, surface-acoustic wave (SAW)-type duplexers
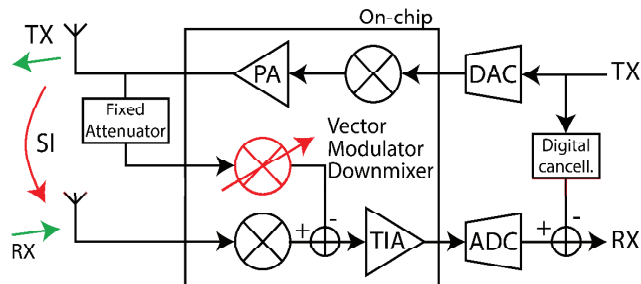

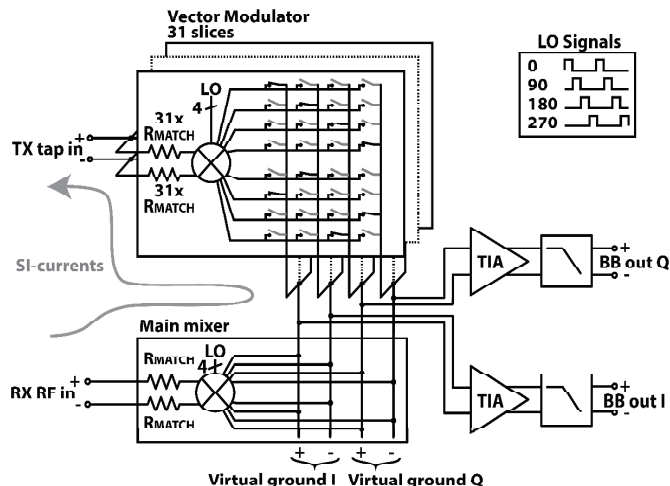Figure 2: Self-interference cancelling transceiver front-end.

Figure 3: Implementation details of the SI-cancelling receiver [5]. The vector modulator is sliced in 31 parallel slices and augmented by static multiplexer switches that can rotate the phase of each slice. This results in a discretely tunable phase and amplitude.

are commonly used in FDD systems to prevent the TX signal and TX-generated noise at the RX frequency from leaking into the RX. SAW-duplexers can, however, exploit the frequency difference between the two FDD-signals and use *filtering* to prevent leakage. Therefore, SAW duplexers are unable to support IBFD mode, when there is no frequency separation. Since electrical-balance duplexers rely on cancellation, they can prevent leakage both in FD and FDD modes.

The electrical-balance duplexer operation principle is illustrated in Figure 4; the RF circuit comprises a hybrid transformer and a balance network which is essentially a tunable dummy load impedance. By tuning the balance network impedance, the magnitude and phase of two TX-RX transfer paths are made equal, such that they destructively interfere at the single-ended RX port. A single-ended topology is preferred to avoid a common-mode SI and to enable high-power operation. This topology has been prototyped in 0.18µm RF SOI CMOS technology covering a small area of 1.75mm² [7].

For FDD compatibility, 50dB of isolation is required at both frequencies to prevent leakage of the TX signal itself at the TX frequency as well as the noise generated by the TX within the RX band, just like a traditional surface-acoustic wave (SAW)-type duplexer. This prototype integrates a balance network that enables (dependent) control of real and imaginary impedance
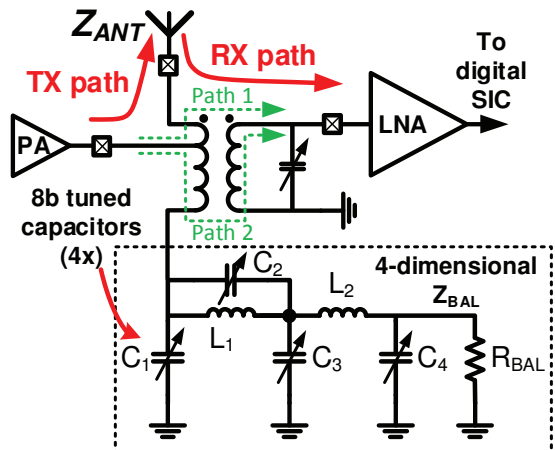
Figure 4: The antenna interface implemented using an electrical-balance duplexer.

Figure 5: Measured electrical-balance duplexer self-interference isolation performance with a capacitive 50Ω reference impedance.

at two frequencies with 4 tuning dimensions (Figure 4). Therefore, the electrical-balance condition can be tuned for two frequency points. Using a (slightly capacitive) 50Ω test fixture, measurements show a trade-off between the bandwidth and the average SI-isolation performance, as shown in Figure 5. This trade-off is used for IBFD operation, while this tunability also implies compatibility with FDD since high TX-RX isolation is provided at two frequencies. However, future work is still needed to address dual-frequency tuning with real antennas that have a substantial frequency- and environment-dependent impedance. Finally, the prototype has highly-linear tunable capacitors to ensure that external blockers do not cause intermodulation with the TX self-interference in FDD mode, which could lead to RX de-sensitization for blockers at two times the TX frequency minus the RX frequency [7].

The electrical-balance duplexer also allows conventional TDD operation to support legacy standards. This operation mode can be exploited for initial tuning of the balance network for preceding FDD or IBFD operation.

V. CONCLUSION

The in-band full duplex (IBFD) concept is a valid candidate for resolving several challenges of next generation (5G) mobile networks. The introduction of full-duplex in 5G however increases the design requirements on the full-duplex radio transceivers. For commercial relevance and implementation in hand-held devices, these transceivers should support dense (co-)integration in a low-cost process technology and be tunable to support alternative communication schemes and backward compatibility. Two potential transceiver designs are discussed and evaluated in the context of 5G application. The first design, a self-interference cancelling front-end implemented in 65nm CMOS, offers a full-duplex transceiver performances over a very broad operational frequency range (0.15-3.5GHz). This design is compatible with legacy TDD and the topology can be redesigned to support FDD. The second design, an electrical-
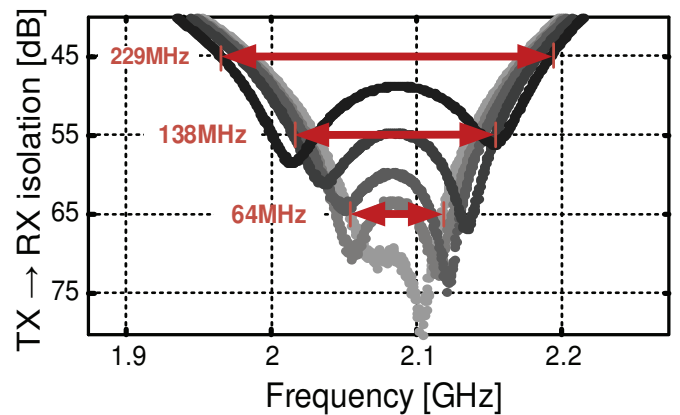
balance duplexer implemented in 0.18μm RF SOI CMOS, offers tunable self-interference cancellation directly at RF to relax the RX requirements. The prototype's high linearity means that low distortion is generated in FDD mode, critical when the TX and a jammer at a frequency offset cause intermodulation.

Further work is required to fully assess the proposed transceiver technology for 5G mobile networks, but the proposed in-band full-duplex designs are promising.

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