2.2 A +70dBm IIP3 Single-Ended Electrical-Balance Duplexer in 0.18µm SOI CMOS

Barend van Liempd[1], Benjamin Hershberg[1], Kuba Raczkowski[1], Saneaki Ariumi[2], Udo Karthaus[3], Karl-Frederik Bink[3], Jan Craninckx[1]

[1]imec, Leuven, Belgium, [2]Murata, Kyoto, Japan, [3]HiSilicon, Leuven, Belgium

The electrical-balance (EB) duplexer concept explored in [1-4] suggests a possible integrated multiband alternative to conventional fixed-frequency surface-acoustic-wave (SAW) duplexers. The basic principle of the EB duplexer is to balance the impedances seen at the ports of a hybrid transformer to suppress signal transfer from the TX to the RX through signal cancellation (Fig. 2.2.1). While the potential payoff is tantalizing, several challenges must still be solved before EB duplexers can become commercially viable. Specifically, the duplexer must provide high isolation and linearity in both the TX and RX bands across wide bandwidth (BW), with low insertion loss (IL), all in the presence of a real antenna whose impedance is constantly varying due to real-world user interaction. In this paper, we present a duplexer that significantly advances the state-of-the-art for two of these critical challenges: linearity and insertion loss.

The single-ended duplexer topology is shown in Fig. 2.2.1. Earlier implementations of EB duplexers use a differential LNA at the RX port [1-4]. Unfortunately, even when differential-mode isolation is high, the common-mode isolation will still be unacceptable [1,4], causing the LNA to compress when the PA operates at full power [2]. A solution was proposed in [2,3], at the cost of significantly more components and increased IL. We propose the simpler approach of moving to a single-ended topology, wherein only two transfer paths exist from TX to RX. To achieve isolation between the TX and RX, a balance network impedance (Z_{BAL}) must be chosen so that the signals through these two transfer paths destructively interfere at the RX port. The inherent asymmetry between these two paths, arising from the hybrid transformer capacitive coupling, means that the balance network and antenna impedances will not be the same when cancellation occurs. However, this asymmetry is easily accounted for during design of Z_{BAL}.

In order to minimize insertion loss, the hybrid transformer is designed using the back-end metal stack shown in Fig. 2.2.1. It includes 3 very thick RF metals with bar-vias between all RF metals. The primary winding is stacked on top of the secondary winding to improve coupling and to shield the primary winding from the substrate. Adequate substrate shielding is particularly critical in SOI CMOS, where signals present on RF metal layers can couple into nonlinear regions at the interface between the buried-oxide layer and handle wafer to generate distortion. Thus, an orthogonally patterned grounded shield is added. A 2:1 transformation ratio is used to convert the nominal 100Ω impedance connected to the primary winding (the antenna and balance network impedance combined) to 50Ω at the single-ended RX port. The transformer center-tap (TX input) is deliberately skewed to favor TX IL over RX IL [1,4].

A key challenge that motivates this proof-of-concept design is to demonstrate compliance with all linearity specifications of modern wireless standards. Most stringent among these is the 3GPP test scenario where a -15dBm out-of-band jammer present at the antenna port at $2f_{TX} - f_{RX}$, i.e. the "full-duplex" (FD) spacing, intermodulates with the +27dBm TX input signal. In this case, the duplexer must not generate IM_3 products >-112dBm (the 1.4MHz BW noise floor at the RX port). This translates to a demanding >+70dBm TX-to-antenna IIP3 requirement.

Figure 2.2.2 shows the tunable impedance network Z_{BAL} of Fig. 2.2.1 in greater detail. Each of the four tunable capacitors has a tuning range of 0.3 to 1.2pF and Q >19, with 8b tuning resolution. Each tunable capacitor is an array of the switched capacitor unit cells illustrated in Fig. 2.2.2. In order to satisfy the high linearity requirements and sustain the large voltage swing present in the balance network at full +27dBm TX power, switches are built by stacking four SOI CMOS transistors. The absence of the parasitic nonlinear substrate capacitance in SOI enables transistor stacking with much lower harmonic distortion. For the small LSB cells, parasitic capacitances still impede efficient voltage equalization across the transistors, so explicit drain-source coupling capacitances (C_C) increase coupling and the linearity of the LSB cells. Two metal-insulator-metal unit capacitors (C_U) are used in the tunable capacitor banks, which allow the capacitor banks to be connected in either differential (C_2) or single-ended (C_1,C_3,C_4) configurations, and controlled using standard non-negative supply voltages (0V and 2.5V). As a result, the total size and area dedicated to the C_U capacitors is quadrupled, but this does not impact linearity since the switch transistors still dominate as the primary source of harmonic distortion in Z_{BAL}. Even at poor isolation, C_{SEC} (Fig. 2.2.1) experiences an attenuated TX amplitude, which relaxes swing and linearity constraints. The 5b tunable capacitor is constructed with only two stacked transistors to achieve Q>58 and a tuning range of 0.5 to 1.8pF. The two inductors in Z_{BAL} are both 1.8nH with a peak Q of 20. The 50Ω polysilicon resistor is sized to withstand heating and power dissipation constraints. As described earlier, the asymmetry of the hybrid transformer requires compensation, which is done by adding extra static capacitances to C_1 and C_2.

This duplexer prototype was fabricated in the 1P5M IBM 0.18µm RF SOI CMOS process. The complete duplexer, including the transformer and Z_{BAL}, occupies 1.75mm^2 of chip area. Figure 2.2.7 shows a die micrograph.

Figure 2.2.3 shows the antenna-side impedance range for which >50dB isolation is found, using an external impedance tuner, at 1.9, 2.0, 2.1 and 2.2GHz across a coarse grid of $4^4 = 256$ balance network settings out of $(2^8)^4 \approx 4.3$M settings. This Z_{BAL} "cloud" implies operation with any <1.5:1 VSWR antenna impedance at any single frequency from 1.9 to 2.2GHz. By virtue of the orthogonal impedance shifts provided by the four capacitors in Z_{BAL}, the impedance coverage is maximized. Also shown in Fig. 2.2.3, for a close-to-50Ω Z_{ANT}, the prototype duplexer achieves >50dB isolation across >200MHz BW. Note that Z_{BAL} in this prototype, similar to [1-3], still cannot provide a large BW for a generic (real) antenna. The challenge of consistently balancing a real world antenna *across frequency* is left for future work.

Measured insertion and return loss is presented in Fig. 2.2.4, with <3.7dB TX-to-antenna insertion loss and <3.9dB antenna-to-RX insertion loss for any operating frequency from 1.8 to 2.2GHz. For these measurements, Z_{BAL} is tuned to provide at least 50dB isolation at the marked frequencies and the secondary side capacitor C_{SEC} is tuned to minimize RX-path IL. Return loss is <-15dB for all ports.

The measured results of three linearity tests are presented in Fig. 2.2.5. First, the top graph shows the TX-to-antenna IIP3, which varies from +70 to +83dBm across balance network settings. For the antenna-to-RX path (not shown), at least +72dBm IIP3 is also measured at all settings. Second, the middle graph shows the measured IM3 at the RX output for the FD-spaced jammer test, with a large TX signal at the TX port and a jammer at the FD frequency at the antenna port. With +24dBm TX signal power appearing at the antenna, the IM3 product at the RX output is measured to be -122dBm, 10dB below the 3GPP spec. Third, the bottom graph shows the results of a triple-beat (co-channel (CC) jammer) test [2,3]. When a two-tone TX signal delivers +24dBm to the antenna port and a -43dBm co-channel jammer is applied at the antenna port in the RX band, the cross-modulation product that appears at the RX port is at -145dBm, 33dB below the spec. The measurement setup IIP3 is +85dBm, and IIP3 is measured using 2 tones at 1.84GHz and 1.98GHz.

As seen in a comparison with the state-of-the-art in Fig. 2.2.6, this stand-alone EB duplexer demonstrates feasibility in two critical areas: it achieves >+70dBm IIP3 and achieves <3.7dB TX insertion loss and <3.9dB RX insertion loss. At the same time, it provides isolation, isolation bandwidth, and impedance-tuning abilities competitive with the state-of-the-art.

Acknowledgements:
This work was performed as part of imec's green radio research program and received funding through the European Union Seventh Framework Programme under grant agreement no. 316369 – project DUPLO. The authors thank Integrand Software for EMX, H. Suys and L. Pauwels (imec) for their support.

References:
[1] M. Mikhemar, H. Darabi and A.A. Abidi, "A Multiband RF Antenna Duplexer on CMOS: Design and Performance," *IEEE J. Solid-State Circuits*, vol.48, no.9, pp. 2067-2077, Sept. 2013.
[2] S.H. Abdelhalem, P.S. Gudem and L.E. Larson, "Hybrid Transformer-Based Tunable Differential Duplexer in a 90-nm CMOS Process," *IEEE Trans. Microwave Theory and Techniques,* vol. 61, no. 3, pp.1316-1326, March 2013.
[3] S.H. Abdelhalem, P.S. Gudem and L.E. Larson, "Tunable CMOS Integrated Duplexer With Antenna Impedance Tracking and High Isolation in the Transmit and Receive Bands," *IEEE Trans. Microwave Theory and Techniques*, vol. 62, no. 9, pp. 2092-2104, Sept. 2014.
[4] B. van Liempd, R. Singh, S. Malotaux, P. Reynaert, J. R. Long and J. Craninckx, "A Dual-Notch +27dBm TX-Power Electrical Balance Duplexer," *European Solid-State Circuits Conf.*, pp. 463-466, Sept. 2014.

 978-1-4799-6224-2/15/$31.00

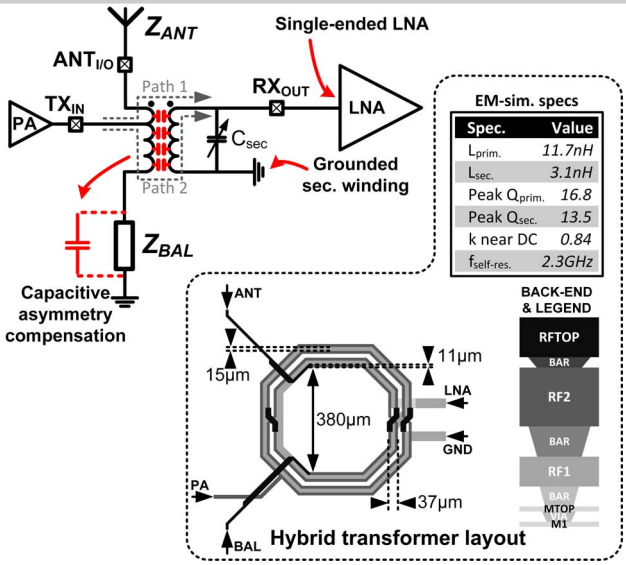

Figure 2.2.1: The single-ended duplexer topology and transformer.

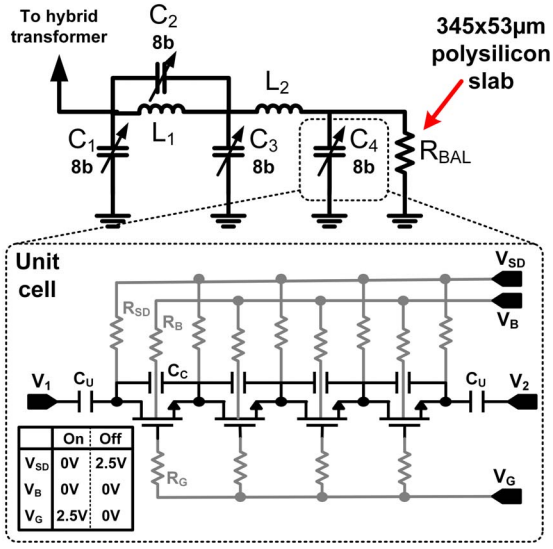

Figure 2.2.2: Balance network and switched-capacitor unit cell.

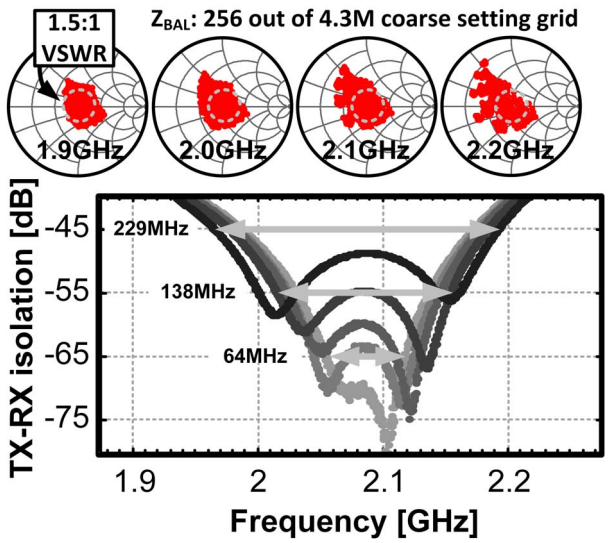

Figure 2.2.3: Measured impedance "cloud" and isolation performance.

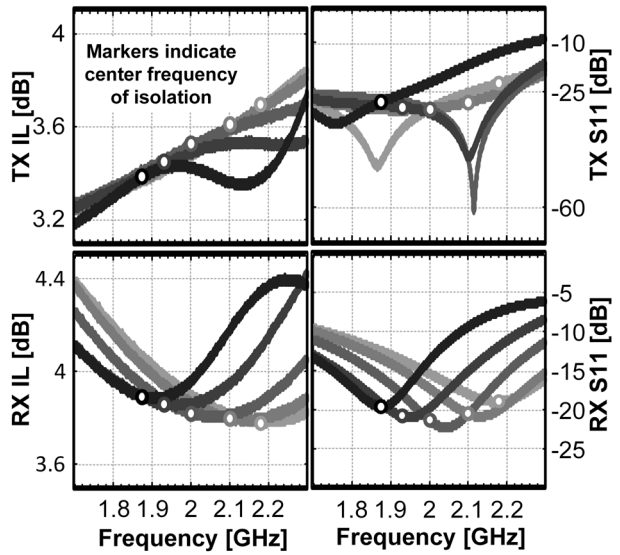

Figure 2.2.4: Measured insertion loss (IL) and return loss (S_{11}).

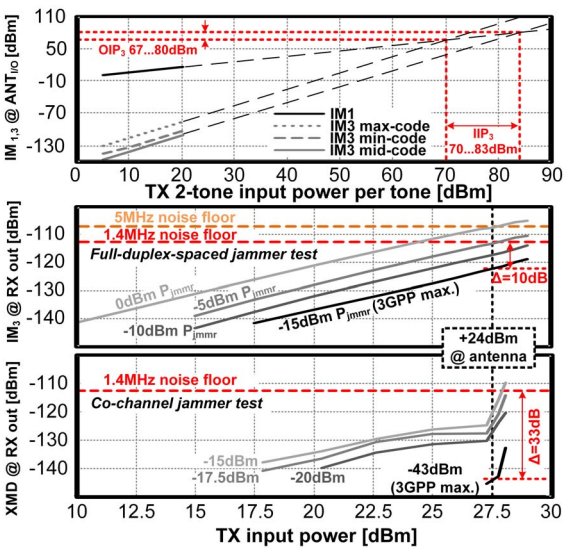

Figure 2.2.5: Measured linearity: IIP_3, IM_3, and XMD.

		JSSC'13 [1]	TMTT'13 [2]	TMTT'14 [3]	ESSCIRC'14 [4]	This work
Key specifications	Technology [CMOS]	65nm	90nm	90nm	0.18µm	**0.18µm SOI**
	Z_{ANT} reference impedance	50Ω	50Ω	2:1 VSWR	SkyCross ant.	**1.5:1 VSWR**
	Frequency range [GHz]	1.5-2.1	1.7-2.2	1.7-2.2	1.78-2	**1.9-2.2**
	Z_{BAL} tuning dimensions	2	2	4	4	**4**
	Area [mm²]	0.2 incl. LNA	0.6 incl. LNA	2.2 incl. RX	0.67	**1.75**
Small-signal operation	Common-mode isol. [dB]	(1 winding)	>60	>60	Poor	**Single-ended**
	TX-to-RX isolation [dB]	>50 (diff. LNA)	>60 (diff. LNA)	>50 (diff. LNA)	>50 (diff. LNA)	**>50**
	Aggregated isol. BW [MHz]	600(1)	500(1)	N/A	220	**300**
	RX insertion loss [dB]	With LNA	With LNA	With RX	11	**<3.9**
	RX casc. NF [dB]	5.0	6.7(2)	6.7(2)	No LNA	**No LNA**
	TX insertion loss [dB]	2.5	4.7(2)	4.5(2)	3.0	**<3.7**
Large-signal operation	Max. P_{TX} at Antenna [dB]	<+12	+27	+27	+27	**+27**
	TX-to-Antenna IIP_3 [dBm]	N/A	N/A		>+48	**>+70**
	Z_{BAL} IIP_3 (sim.) [dBm]	N/A	N/A	+54		**+65**
	Antenna-to-RX IIP_3 [dBm]	N/A	-5.6 incl. LNA	-4.6 incl. RX	>+32	**+72**
	IM_3 at EBD RX out [dBm]	N/A	N/A	N/A	Poor	**-124**
	FD-spaced jammer					(24dBm)(3)
	XMD at EBD RX out [dBm]	N/A	-105(4)	-115(4)	Poor	**-145**
	Co-channel jammer		(25.3dBm)(3)	(17.5dBm)(3)		(24dBm)(3)

(1) Only measured with an almost frequency-constant reference impedance. (2) Assumes a balun with 0.8dB loss.
(3) TX power observed at the antenna port. (4) Referred to the LNA input assuming: [2] 14dB G_{LNA}, [3] 43dB G_{RX}.

Figure 2.2.6: Comparison with state-of-the-art.

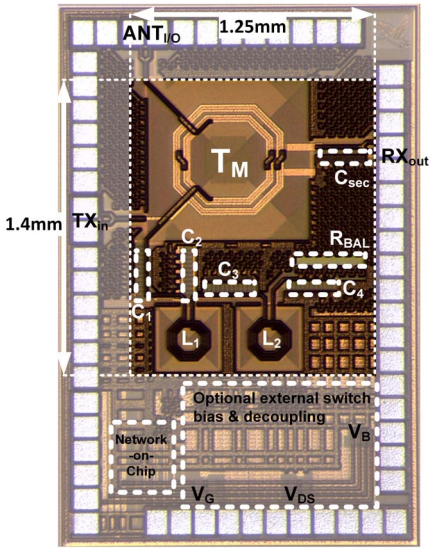

Figure 2.2.7: Micrograph of test chip in 0.18µm SOI CMOS.

978-1-4799-6224-2/15/$31.00