A DTC-Based Subsampling PLL Capable of Self-Calibrated Fractional Synthesis and Two-Point Modulation

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***Abstract*— We present an analog subsampling PLL based on a digital-to-time converter (DTC), which operates with almost no performance gap (176/198 fs RMS jitter) between the integer and the worst case fractional operation, achieving −246.6 dB FOM in the worst case fractional mode. The PLL is capable of two-point, 10 Mbit/s GMSK modulation with −40.5 dB EVM around a 10.24 GHz fractional carrier. The analog nonidealities—DTC gain, DTC nonlinearity, modulating VCO bank gain, and nonlinearity—are calibrated in the background while the system operates normally. This results in ∼15 dB fractional spur improvement (from −41 dBc to −56.5 dBc) during synthesis and ∼15 dB EVM improvement (from −25 dB to −40.5 dB) during modulation. The paper provides an overview of the mechanisms that contribute to performance degradation in DTC-based PLL/phase modulators and presents ways to mitigate them. We demonstrate state-of-the-art performance in nanoscale CMOS for fractional-N synthesis and phase modulation.**

***Index Terms*— Analog PLL, background calibration, digital-to-time converter (DTC), divider-less, fractional-N subsampling PLL (FNSSPLL), frequency synthesis, GMSK, linearization, low jitter, phase/frequency modulation, PLL, polar modulation, subsampling PLL (SSPLL), two-point modulation, wideband modulation.**

I. Introduction

STRONG demand for higher wireless data throughput, driven largely by the multibillion dollar smartphone market, will continue for the foreseeable future. At the same time, device battery life is a critical end-user performance bottleneck that is pushing the wireless RF community to explore new system architectures potentially improving the power efficiency. From the network-operator perspective, spectrum availability is a major bottleneck. It is therefore attractive to use higher order modulation schemes that maximize the spectral efficiency, achieving high bit/s/Hz values. This consequently places tough constraints on the linearity and noise requirements of transceivers.

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Digitally intensive, scaling friendly polar transmitter architectures [1]–[5] show potential for superior power-efficiency over their Cartesian counterparts. The main drawback, however, is that the polar representation of amplitude and phase signals have wider bandwidths than their I and Q counterparts [6]. Consequently, a polar transmitter requires a wideband phase modulator which is typically implemented by a bandwidth limited PLL. Moreover, the quality of the modulated signal, typically expressed in terms of error-vector magnitude (EVM) remains heavily limited by the PLL phase-noise, mismatch and nonlinearity in the digital-to-modulated phase conversion.

Gao's divider-less PLL [7], based on high-gain subsampling phase-error detection core shows unparalleled efficiency for low-jitter, integer-N, frequency synthesis. Extending this concept to fractional-N [8] synthesis and wideband modulation imposes an additional set of challenges. To maintain the same level of spectral purity, the system requires low fractional quantization-error residue, highly-linear phase-error detection and accurate injection of the modulating signal.

A. PLL Based Phase Modulation

A typical phase modulator for a polar TX is based on a fractional-N PLL with a bandwidth carefully selected for optimal filtering of phase-noise from the oscillator and reference, including in-loop and quantization noise. The basic concept of $\Delta\Sigma$ division factor dithering for fractional synthesis [9] can easily be extended to achieve phase modulation. Modulation through the single injection point is limited by the PLL low-pass filtering. For wideband modulation, the loop bandwidth can obviously be increased. This however comes at the price of suboptimal phase-noise filtering in the absence of accurately matched compensation [10], [11].

An alternative wideband modulation technique is two-point injection (Fig. 1), adopted by [12], [13] for analog PLLs. The basic principle is to inject the modulation signal simultaneously in front of the VCO (point-two) and in the reference path, through a programmable divider (point-one). The VCO frequency instantaneously changes with respect to the modulation signal. At the same time, the divider changes its division factor to compensate for the frequency shift, matching the divided output to the input phase/frequency. In case of an accurate match between the two injection points, there is an

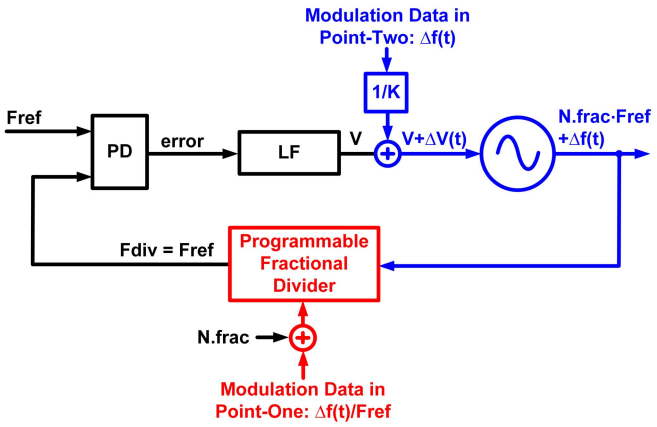


Fig. 1. Basic principle of two-point phase/frequency modulation.

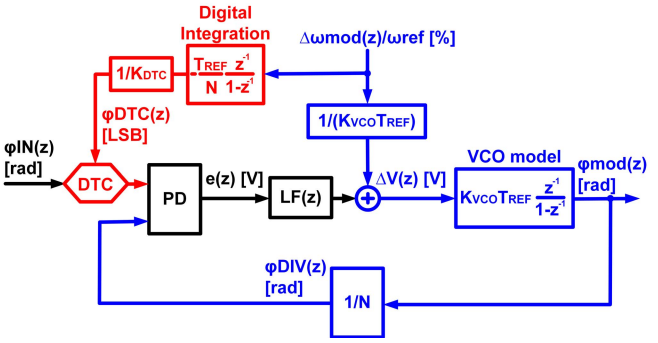


Fig. 2. Phase domain model of a DTC based PLL for phase modulation. With the DTC in the reference path, the divider can be optionally removed from the loop.

overall all-pass of the data to the PLL output. The phase-error detector, and therefore the loop, sense no disturbance due to the modulation.

Two-point injection can be analyzed in frequency domain. Injection point-two has a high-pass profile to the PLL output, while point-one implements a low-pass. There is an all-pass transmission of the modulation data to the PLL output if the bandwidths of the two profiles match.

B. Time-to-Digital vs. Digital-to-Time Conversion in PLLs for Phase-Modulation

Digital PLLs [14] that exploit time-to-digital conversion rather than voltage-domain phase-error processing during frequency synthesis opened up new opportunities in PLL based phase modulation [14]–[17]. A digital PLL offers good control over the mostly digital loop [18], hence it becomes easier to match the modulation injection paths [17]. However, the quantization error of the TDC used for phase-error detection in a digital, fractional-N PLL limits the spectral purity of the phase modulator [19]–[22]. The minimum time-quantization step of the TDC is typically related to the minimum gate delay defined by the physical technology used. Even in advanced 28 nm CMOS it is approximately 10 ps, which is enough to limit the PLL phase-noise performance.

A DTC, on the other hand, can easily operate with a resolution on the order of 100 fs [23], [24], which is fundamentally superior to a TDC in the same technology. The phase modulating capabilities of this block can be used in the feedback path of the PLL [17], [25], or in the reference path [26]–[28] (Fig. 2). In either case, the DTC is used to cancel the phase-error induced by both the fractional-N residue and the two-point modulation injection. It enforces a *near-to-zero* phase-error regime of the phase-error detector (PD), which relaxes the PD design in terms of its range. Recent designs that use a DTC-TDC combination for phase-error comparison exploit this DTC favoring trade-off [26], [29], [30]. An extreme case of this is the 1-bit, bang-bang TDC PLL [18], [25] or MDLL [28], [31] which can be also used for modulation [17].

C. A DTC-Based Fractional-N Subsampling PLL for Phase Modulation

For extremely low noise performance, a DTC-based fractional-N PLL can use a subsampling phase-error detection core [8], [27], [32], [33]. In its original integer-N form [7], without a DTC, the subsampling PLL achieves an unparalleled figure-of-merit (FoM) [34]. The divider-less loop (power savings) of the subsampling scheme has very high phase-error detection gain which suppresses all the in-loop phase-noise generators. Since wide PLL bandwidths can be used for VCO phase-noise filtering, the loop reaches an optimum [35] in which the output spectral purity is mainly limited by reference noise.

To minimize the gap between integer-N and fractional-N performance and to enable two-point modulation with a fractional-N subsampling PLL (FNSSPLL) [8], the problem of injection path matching must be addressed, as well as the challenge of nonlinearity neutralization, both in an analog environment [36].

In the following sections, we present a two-point phase modulator in 28 nm CMOS which uses an analog fractional-N, DTC-based subsampling PLL (FNSSPLL). In Section II we start by explaining the FNSSPLL and introduce digital DTC nonlinearity randomization and self-calibration enhancements. Section III presents the two-point phase modulation capabilities of the FNSSPLL, where the modulation inaccuracies are continuously calibrated in the background. Finally, Section IV reports system measurements, followed by conclusions in Section V.

II. A Self-Calibrated DTC-Based FNSSPLL

A. Basic Operation of the FNSSPLL

Fig. 3(a) depicts a simplified schematic of a FNSSPLL [8]. The high-frequency VCO output sinewave is directly subsampled at the reference rate in this loop, near the zero-crossing. The Gm produces a current linearly proportional to the sampled voltage which represents the phase difference between reference and VCO phases. That current is steered to the low pass filter during a fixed signal-independent pulse width time-window [7], and results in appropriate VCO control adjustment. A frequency acquisition loop [8] (not shown in the

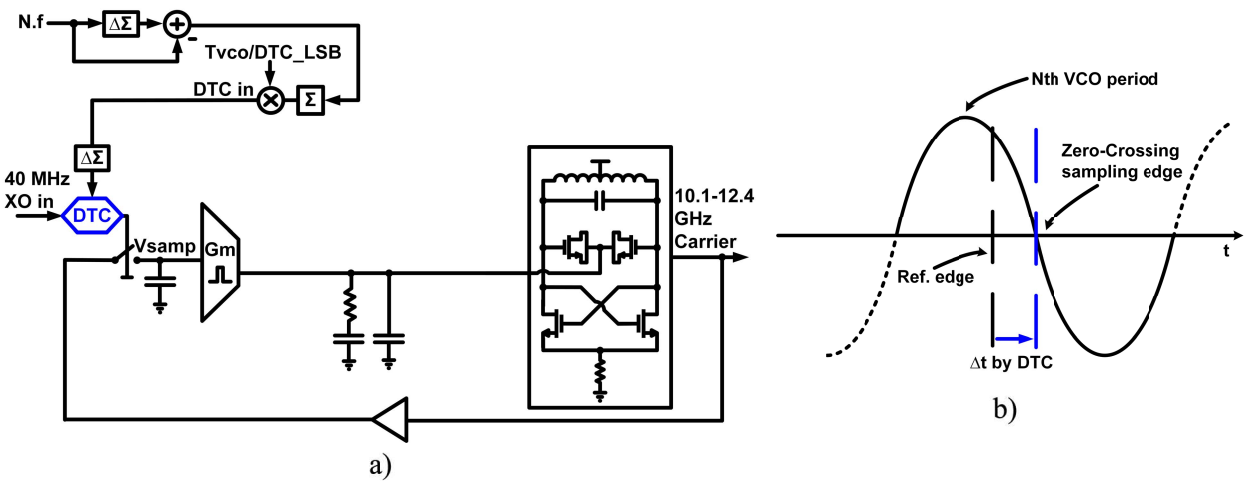


Fig. 3. (a) Simplified schematic of a DTC based fractional-N subsampling PLL (FNSSPLL). (b) Time domain operation of a DTC based FNSSPLL.

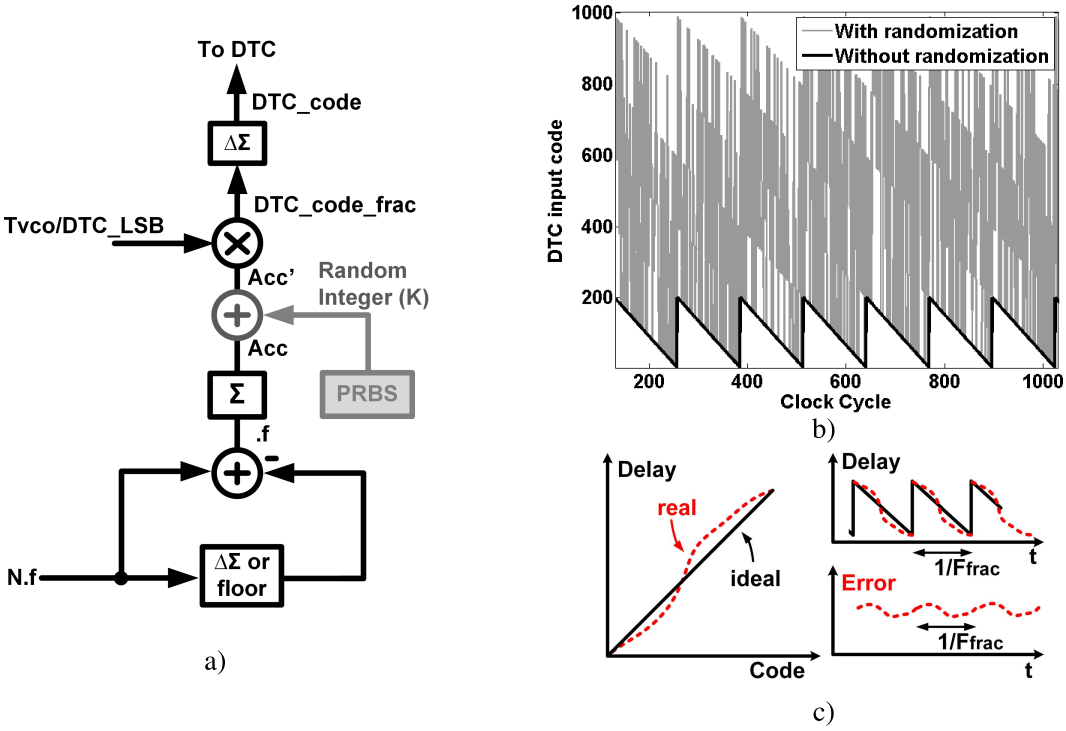


Fig. 4. (a) DTC input code calculation path in the Fractional-N subsampling PLL with pseudo random bit sequence (PRBS) generated random integer number (Random-Jump). (b) DTC input with and without Random-Jump calculation path in the time domain. (c) Generation of fractional spurs because of DTC INL.

figure) is implemented for initial frequency lock. The DTC with ps accuracy serves for fractional residue compensation during fractional-N synthesis. It forces *near-to-zero* voltage sampling by dynamically adjusting the delay, i.e., phase of the reference signal [27] [Fig. 3(b)], such that the PD gain remains determined by the linear part of the sinewave (near the zero-crossing). The DTC requires low phase and quantization noise since its noise is multiplied by N^2 in the transfer to the PLL output [24]. Moreover, any kind of nonlinearity in the phase comparison path (nonlinear DTC) induces noise folding and fractional spurs [37].

B. The Random-Jump for DTC Quantization Noise Randomization

The DTC input code calculation chain is depicted in Fig. 4(a). This digital compensation ensures that sub-sampling events still occur near a zero-crossing, even for a non-integer PLL multiplication number *N.f*. The fractional part of the multiplication number is accumulated and creates a periodic sawtooth signal *Acc*. After appropriate scaling, the required value *DTC_code_frac* is truncated to map on the available discrete codes of the DTC. This truncation is typically performed by a $\Delta\Sigma$ stage which shapes the

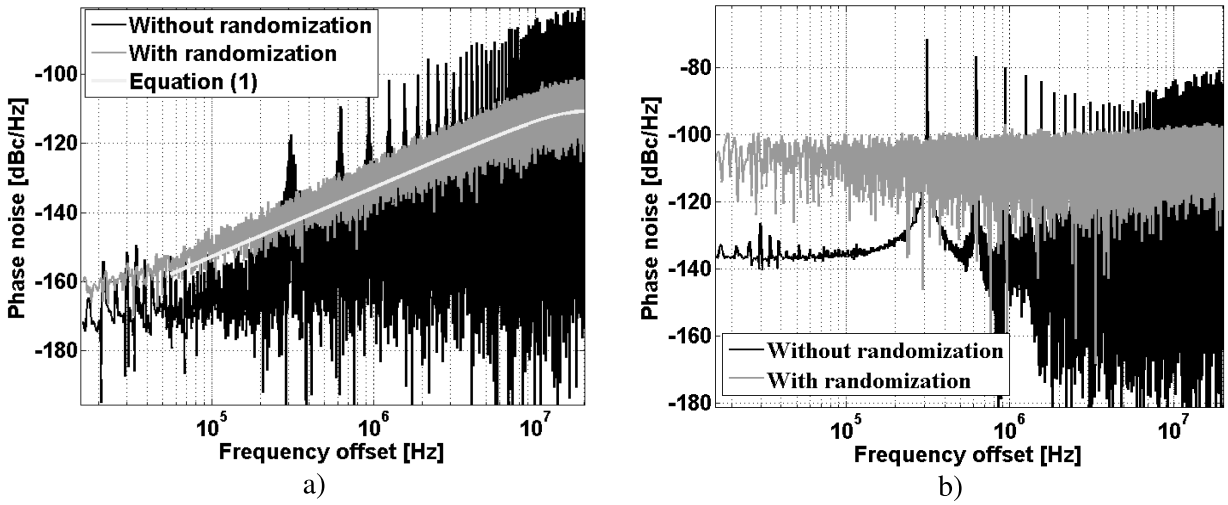


Fig. 5. A 10-bit 0.5 ps LSB DTC's quantization noise spectrum around a 10 GHz fractional carrier (40 MHz * $253+2^{-7}$) before the PLL filtering (in-band) without and with randomization. (a) Linear DTC. (b) Nonlinear DTC (2 LSB INL error). A randomized nonlinear DTC increases in-band noise floor masking the shaped ($\Delta\Sigma$) quantization noise.

quantization noise. The resulting DTC quantization noise power spectral density can be expressed as single sideband phase-noise by:

$$\mathcal{L}(f) = 10 \cdot \log_{10} \left\{ \left(\frac{2\pi}{\sqrt{12}} \cdot \frac{LSB}{T_{VCO}} \right)^2 \frac{1}{F_{REF}} \cdot [2 \sin(\pi f T_{REF})]^2 \right\} \left[\frac{\text{dBc}}{\text{Hz}} \right], \quad (1)$$

at in-band PLL output, where *LSB* represents the DTC LSB delay, T_{VCO} is the VCO period, $F_{REF}$and T_{REF} are the crystal reference frequency and period, respectively, and f is the frequency offset. The term $[2\sin(\pi f T_{REF})]^2$ comes from 1st order $\Delta\Sigma$ shaping [38] at reference rate. If the DTC quantization error is set to 0.5 ps, then the in-band (500 kHz offset) phase-noise at 3.6 GHz output (40 MHz reference) appears at -148 dBc/Hz. This value suggests that quantization noise can easily be kept under the thermal noise floor in a DTC-based subsampling PLL.

Equation 1 assumes an uniform Gaussian quantization noise distribution. This assumption does not strictly hold for a periodic sawtooth input quantized by a 1st-order $\Delta\Sigma$ and results in additional spurs. This is most pronounced for fractional residue offsets that are in-band near the loop cut-off, where the DTC sees a fast varying input without the benefit of PLL filtering. The quantization error of such a signal has a significant amount of energy stored within spurious tones, typically at harmonics of the fractional residue *.f*. Such tones, induced by "colored" i.e. repetitive DTC quantization errors, can appear as fundamental (fractional) spurs in the output spectrum [37].

We propose a DTC delay calculation method which removes the colored noise distribution from the DTC quantization error. A pseudo-random integer is added to the original *Acc* value [Fig. 4(a)] to enforce the DTC to sample random neighboring VCO zero-crossings. The sub-sampling operation is not altered since phase lock does not discriminate between adjacent integer-N periods [8], and the phase information captured by the sub-sampler is nearly identical in either case. However, by dithering the exact VCO period with which to sub-sample, different DTC input codes that induce different quantization errors can now be used for the same fractional residue. A direct consequence of this is a "decolored" quantization noise spectrum. This is shown in Fig. 5(a) for a random integer jump in the range [0:4] generated by the PRBS (pseudo random binary sequence). The method does not induce additional quantization noise in the system, since the quantization error remains within 0.5 ps, but the spurious content is masked. The method necessitates a DTC with a larger range that covers multiple VCO periods, unless a multiphase, e.g., a quadrature VCO is used.

C. The Random-Jump for DTC Nonlinearity Randomization

Any nonlinearities in the phase-error comparison path of a PLL will also induce fractional spurs and noise folding. In the context of analog PLLs, this problem typically originates from a nonlinear charge-pump [39], [40]. Similarly, in classical digital PLLs where an analog PFD is replaced by a TDC, the TDC causes similar issues [19], [20], [41].

In DTC-based PLLs, this problem arises due to the nonlinearity of the DTC, since the delay through the DTC affects the phase-error detection. Intuitively, if the DTC has a pronounced integral nonlinearity (INL), by application of a periodic signal at its input [Fig. 4(c)] during fractional synthesis, the DTC will create periodical errors. The periodicity is related to the fractional multiplication number and results in spurs at the fractional residue frequency and its harmonics [37]. Again, the Random-Jump mechanism described earlier helps with spurious tone reduction by removing periodicity from the DTC INL induced errors. For example, with [0:4] jump range, there are five different DTC codes and five different INL errors at five different zero-crossings which can be used for the same residual phase compensation. The cost of randomization is

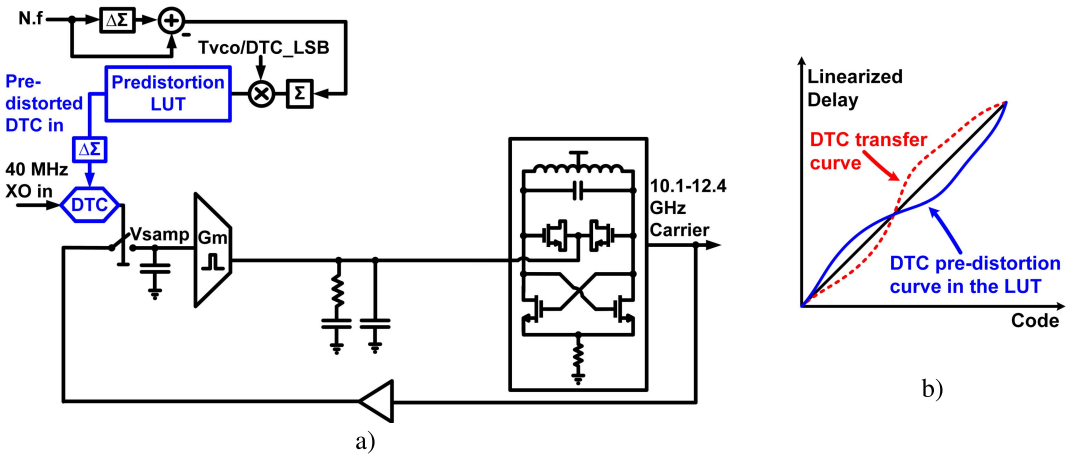


Fig. 6. (a) Concept of FNSSPLL DTC predistortion based on a look-up table (LUT). (b) Predistortion principle: LUT stores a curve which mimics inverse of the DTC nonlinearity.

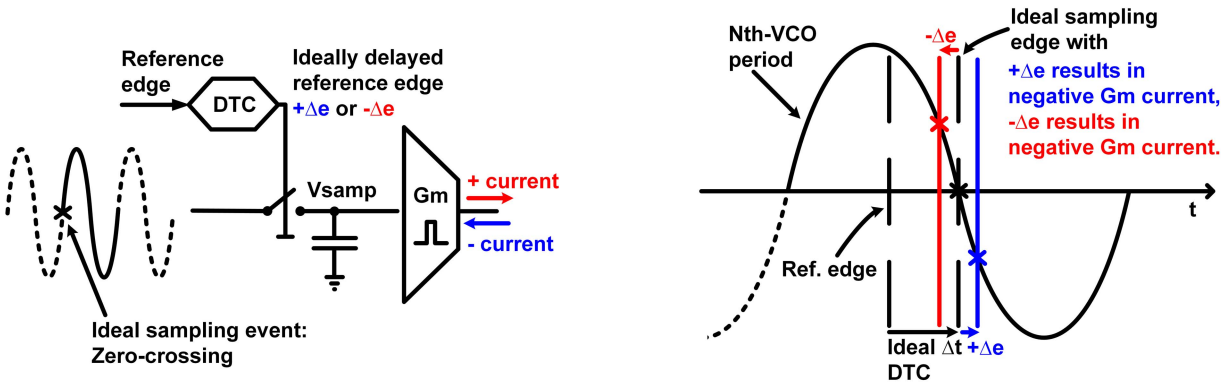


Fig. 7. The sign of the Gm output current is correlated to the error of the DTC code.

now, unfortunately, a higher noise floor, i.e., the spur energy is spread, not removed. Nevertheless, the reduction of spurs can be of greater importance than increased noise if the in-band noise is not a limitation, as is the case for many low-power medium-performance PLLs.

Fig. 5(b) shows the DTC error induced phase-noise in-band, without PLL filtering) for a fractional 10 GHz VCO output in a simulation with a nonlinear DTC (2 LSB INL), both with and without randomization. Clearly, to correct the spurs without raising the phase-noise floor, the spurs themselves must be reduced, meaning that better DTC linearity is required.

D. Self-Calibration of the DTC Nonlinearity

Instead of directing design effort into analog DTC linearization [23], [24], [42] for low spur content at the PLL output, we propose digital self-calibration. If the DTC INL is *known* (measured *a priori*), predistortion can be used to remove the predictable errors [Fig. 6(a)]. Since we use a 10-bit 0.42 ps LSB DTC [24], a 10-bit look-up-table (LUT) could be employed in front of the DTC. The LUT stores the INL value at every DTC code. At a given cycle, the appropriate INL error is simply subtracted from the original DTC input code. With this correction to the nonlinear DTC the sampler correctly samples near the VCO zero-crossing restoring spur-free PLL operation.

For accurate predistortion the DTC INL needs to be measured. This is not a trivial task, especially for small DTC time steps (on the order of 100 fs) [42]. Moreover, the DTC transfer curve is very sensitive to process and environmental variations, meaning that the correct predistortion values will drift over time. It is therefore mandatory to have a digital self-calibration which runs in the background while the PLL operates normally.

The central phenomena used for self-calibration is the correlation between the DTC input code and the instantaneously detected phase-error. Namely, if the DTC is nonlinear, the sampler will trigger at an offset from the VCO zero-crossing (Fig. 7). The non-zero sampled voltage that results is proportional to the timing error at that particular DTC code (plus noise from other sources). The transconductor then outputs a non-zero current into the loop filter. This error current contains information about the DTC (INL) timing error per particular code. The main idea of the proposed

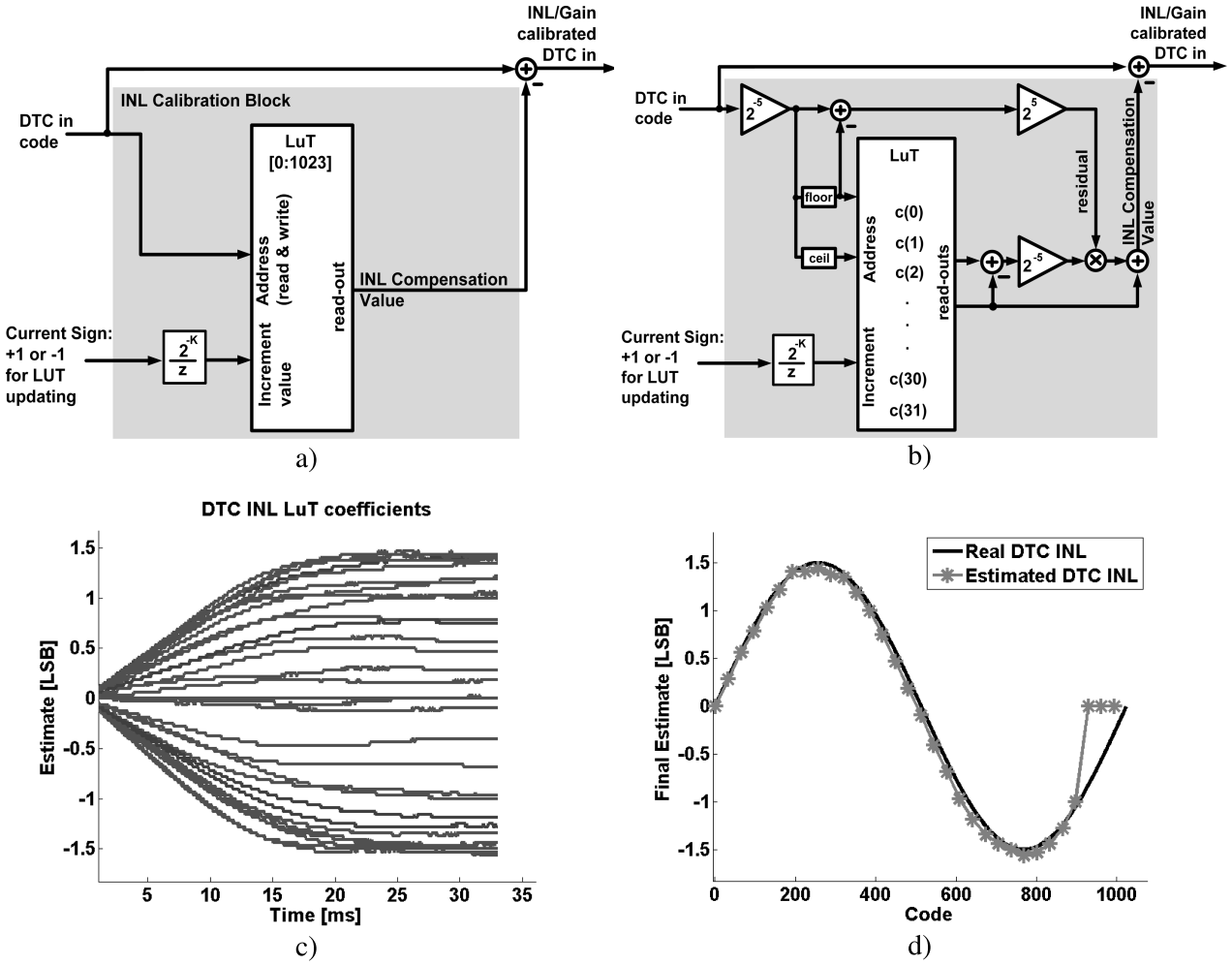


Fig. 8. (a) Digital self-calibration of the DTC with a 1024 entry LUT. (b) Digital self-calibration of the DTC with a 32 entry LUT and piece-wise linear approximation. (c) Time domain simulation of the FNSSPLL with 32 entry LUT based DTC calibration with a nonlinear DTC. (d) Final INL estimates.

calibration scheme is to track the average value of this current[1] for each DTC input code, and to use this information to construct an accurate pre-distortion function that linearizes the DTC.

Measuring the magnitude of the current produced by the transconductor is cumbersome. Instead, we extract only its sign. This is enough to determine if the sampling instance came before or after the VCO zero-crossing at the respective DTC code. These two situations are depicted in Fig. 7. The sign information is used to gradually update the INL LUT [Fig. 8(a)] using a sign least mean square (LMS) algorithm. The current error sign is in every cycle initially extracted by a comparator. The digital $(+/-1)$ value is then scaled by $2^{-K} \ll 1$ and finally integrated to the appropriate LUT address defined by the DTC input code. While the PLL operates, the LUT coefficients gradually change towards their optimal values at a convergence speed dependent on K. They settle to values that accurately represent the DTC INL, and only move if the INL changes (due to PVT), because the error sign becomes a zero-mean stream per particular code once converged.

To reduce complexity and area, we implement a 32 entry piece-wise-linearized equivalent of the 1024 entry LUT, as shown in Fig. 8(b). The 32 correction coefficients are spread across 1024 DTC INL values, with linear approximation in-between. The error cancellation is negligibly compromised if the INL curve changes monotonically between two neighboring correction coefficients. In every cycle, the coefficients are updated-based on the extracted error sign. The correction value is formed by linearly approximating between the floored and ceiled LUT address i.e. by approximating between the two instantaneous read-outs from the LUT. To visualize this approximation, a straight gray line is indicated between the '*' symbols (representing 32 LUT correction values) in Fig. 8(d). This approximation obviously only tracks the 'global' INL characteristic of the DTC transfer curve, and cannot compensate for localized DNL errors for every code. But since the DTC capacitive load array has been sized with intrinsic matching for 10-bit accuracy, such remaining errors are negligible.

[1]Alternatively, it is possible to track the sampled voltage. However, in presence of transconductor offset, the sampled voltage is no longer a valid representation of the phase-error. The type-2 subsampling loop settles in a zero-phase-offset condition which translates to a zero-current state and not in the zero-sampled-voltage state [44].

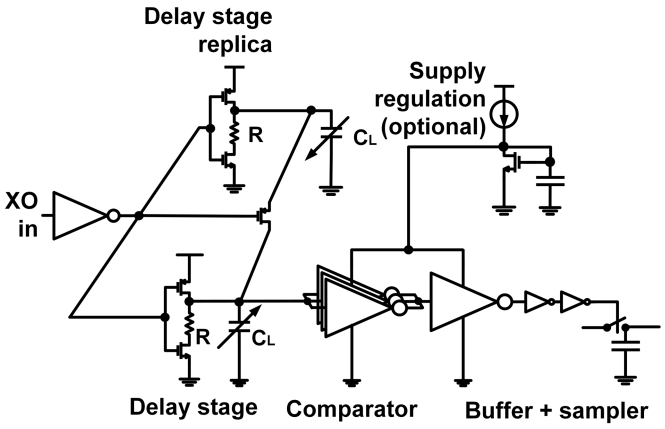


Fig. 9. A simplified schematic of the DTC [24] used in this design.

We reuse the DTC architecture from [24] (Fig. 9) in this design. The overall DTC nonlinearity is dominated by analog effects such as RC-input-slope-dependent (from the delay stage) comparator delay, which typically results in DTC INL curve similar to the exemplary Fig. 8(b) [24] that can indeed be calibrated in the proposed way.

Another concern is supply ripple in the DTC [24], or more specifically colored supply noise which could be coupled into the delay path that uses digital gates. This DTC uses a replica of the sensitive delay stage, in parallel to the main delay path, to ensure that there is no code dependent power consumption (colored supply noise). In other words, the amount of charge pulled from the supply remains consistent at every reference cycle. Moreover, the comparator in the DTC can optionally work on a regulated supply to avoid code dependent time switching instant and the related supply bounce. By taking these precautions, the DTC nonlinearity remains unaltered over time. Any other (non-colored) supply noise in the DTC can still exist and can create phase-noise, hence it is necessary to use enough DTC supply decoupling. Finally, the output DTC buffers generate steep slopes to minimize phase-noise at the sampler or any dependency of the DTC on VCO frequency/swing.

A simulation of the FNSSPLL during the background calibration process is shown in Fig. 8(c) for a DTC with 3 LSB INL error. The tap 2^{-K} gain is set to 2^{-13} for a calibration time of approximately 15 ms, with correction coefficients initialized to zero. Although not the focus of this work, obviously initializing the LUT to previously acquired values will reduce the convergence time, since the calibration must then only settle whatever small PVT related changes have occurred in the interim, i.e., the experienced ΔINL. Also gear-shifting techniques by initially operating with a larger tap gain will speed up the settling. Since the DTC nonlinearity is independent of the VCO operating frequency/swing, recalibration for different output frequencies is not needed, only background tracking for slow supply and temperature variations. Finally, in the absence of spurs (due to calibration) the dithering effect of the Random-Jump technique no longer increases the noise floor appreciably.

The linear gain error of the DTC is another effect that must be calibrated, which can be done using a separate background calibration algorithm [8]. Here, a separate algorithm is not necessary, since it is automatically accounted for in the LUT coefficient update procedure. Just as DTC INL error affects the sampling of the VCO zero-crossing, so does DTC gain error, and as a result, any gain error is removed by the pre-distortion function provided by the LUT. The gain correction algorithm from [8] is still implemented in this design for comparison purposes. It can be run for gain error cancellation but never in parallel with the presented gain/INL calibration algorithm.

E. Extraction of the Current's Sign and Comparator Offset Compensation

Fig. 10 depicts the main transconductor and the sub-circuit used to extract the sign of its current. The subsampled VCO voltage biases the input pair which then steers a proportional current into the loop filter during pulser opening windows [7]. After that pulse, the same current is steered into a sign extracting node within the given reference period. Since the capacitance at the sign extracting node *Vextract* is kept low (e.g. below 100 fF), a high voltage swing can be expected there. This is beneficial for the dynamic comparator [43] which senses the node potential in comparison with *Vfollow*. The output of the comparator is interpreted as +1 or 1. Importantly, the node *Vextract* is reset to *Vlpf* potential, through a unity gain buffer.

Any input-referred offset in the comparator is destructive for DTC INL calibration. Its presence will cause the error sign signal to have a non-zero mean, even when the PLL settles into its zero phase-offset condition (type-II loop). Consequently, the DTC INL calibration block receives a stream of plus-ones and minus-ones with a shift in their mean value that the LUT interprets as error and corrects. This results in a slow drift of the LUT correction coefficients at a speed proportional to the offset level. We solve this with digital background compensation [Fig. 11(a)] that cancels the comparator-induced offset before sending the error sign to the INL calibration block, thereby restoring the average error sign value to zero in the settled state. This is achieved by periodically overruling the Error Sign bit with a fixed high or low value to bring the average output back to zero. The overrule period should be proportional to the magnitude of the offset.

To determine this period, the raw Error Sign output is fed into an integrator, which gradually begins to accumulate in the direction related to the offset sign. Its output drives another integrator (after appropriate scaling by $\mu << 1$) which will eventually overflow at a rate depending on the magnitude of the comparator offset. The overflow flag is used to address a MUX, steering the appropriate artificial error sign value to the INL calibration algorithm. The original Error Sign signal stream is "cleaned" of offset by these periodic injections of override values, which stops the coefficient drift. The first integrator settles to a value which is proportional to the offset.

This algorithm runs in the background in parallel to the INL calibration. If override injections are triggered infrequently, they appear as low-level noise to the INL calibration and

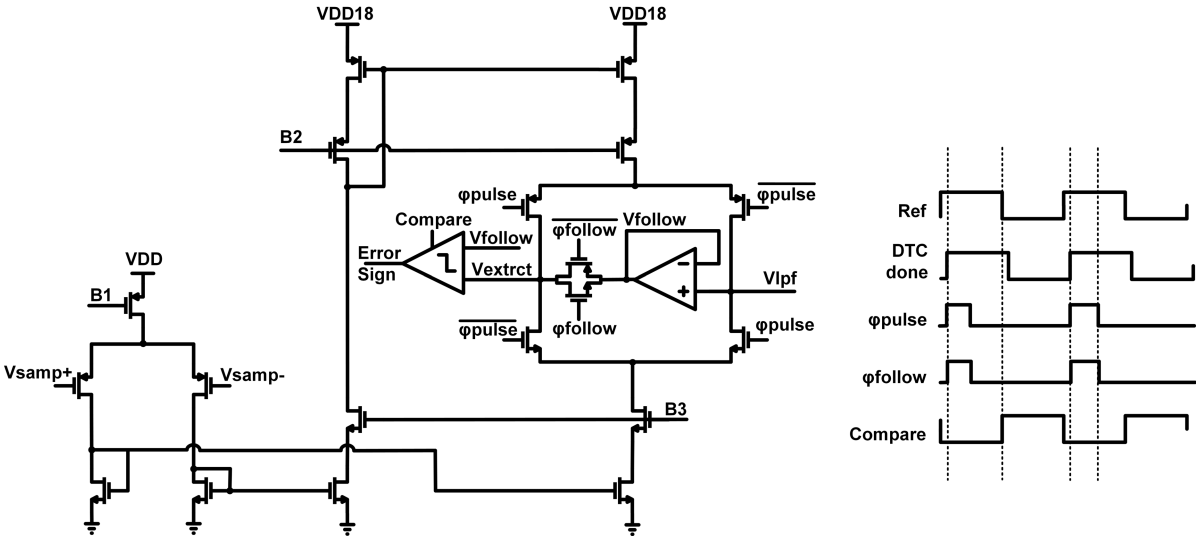


Fig. 10. Gm transconductor and current extraction mechanism schematic and operation time diagrams.

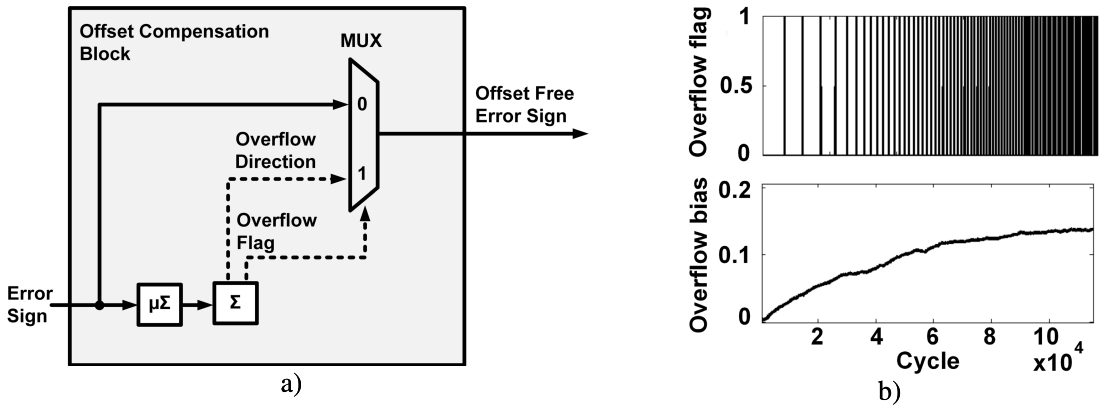


Fig. 11. (a) Digital background offset calibration implementation. (b) Background offset calibration simulation with 0.15σ comparator input swing offset. When the loop settles, the overflow flag is activated approximately every 10th cycle.

are averaged out. However, an excessive amount of offset results in the integrator overflowing frequently, which dilutes the useful information about INL error. For normal settling of the algorithm, the offset has to be kept below 1σ of the full input swing (assuming Gaussian distribution at the comparator input with standard deviation σ). This is easily achieved by good analog design and layout.

Another important detail is that the system indeed requires two integrators connected in series. An alternative implementation with only a single integrator would not be able to track offset in the background. A single integrator would overflow with frequency proportional to the offset but also dependent on the integration gain. To overflow at the exact frequency of interest, this gain would need accurate manual tuning, which is inappropriate for this application.

III. Two-Point Phase Modulator Based on the FNSSPLL

The synthesizer is enhanced for high-speed (10 Mb/s), high-performance (< -40 dB at 10.24 GHz) GMSK phase modulation. The objective is to exploit the subsampling architecture's excellent phase-noise performance for high fundamental EVM performance during modulation.

Similar to other fractional-N PLLs, phase modulation can be achieved by direct modulation of the DTC. The DTC can force controlled "phase errors" (modulation signal) into the loop by purposely moving away from the VCO zero-crossings. The modulation signal is then transferred to the PLL output, although due to the presence of the loop filter the achievable data rate is limited by the loop bandwidth. Higher data rates could be enabled by predistortion of the modulation signal [11] in front of the DTC. However, the predistortion transfer-function is not easily determined since it depends on inaccurate analog components. Furthermore, it can initiate clipping in the PD: the linear range of the subsampling PD is valid only for small phase-errors [44].

To achieve data rates above the loop bandwidth, we use two-point modulation [14]–[17]. To realize the second injection point (point-two), we add a separate 8-bit, 50 kHz/LSB frequency modulating bank in the VCO (Fig. 12) that enables 10 Mb/s GMSK modulation. Since the modulating bank is clocked at F_{REF} (40 MHz) the highest reasonable modulation

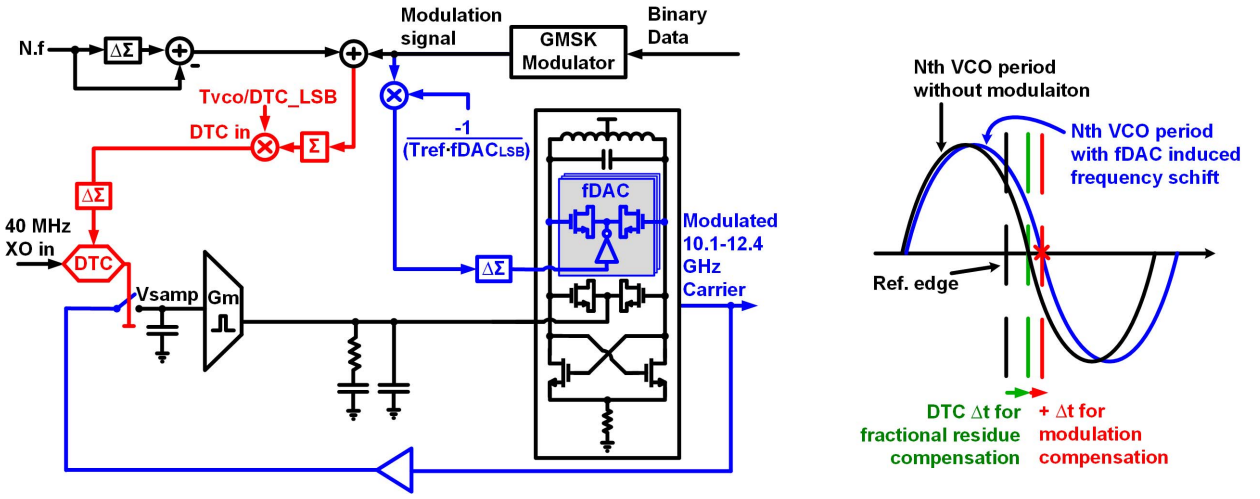


Fig. 12. Simplified two-point modulation schematic based on the FNSSPLL and time-domain modulation operation.

bandwidth is 20 MHz. We restrict the speed of GMSK to 10 Mb/s to avoid degradation by the spectral replicas. During modulation, the input data is sent through a GMSK modulator which generates a frequency modulating signal for the VCO's modulating fDAC, inducing appropriate instantaneous frequency shifts. In the time domain this means that the VCO instantaneously changes its period and the amount of accumulated phase over one reference period changes. This is why the DTC receives the same modulation signal (expressed in phase) on top of the regular fractional residue compensation signal. It must delay the sampling event by an amount that will keep the VCO zero-crossing sampling unperturbed. Importantly, there are no phase-errors in the PD induced by the modulation. The modulation signal transfers unfiltered to the output, i.e., the injection between the two points is cancelled within the PD (sampler) and the loop does not "sense" the modulation data.

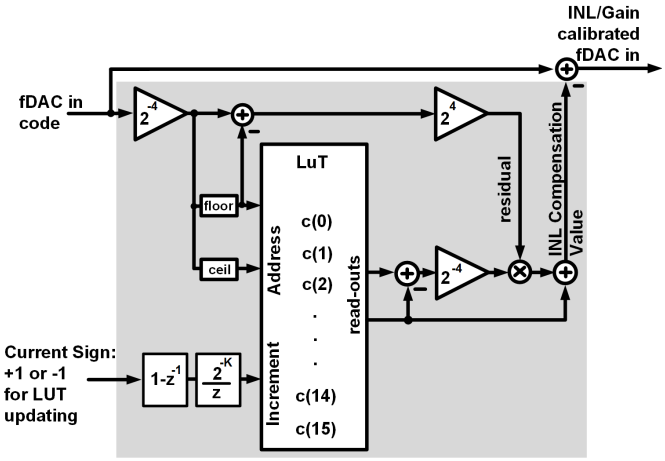


Fig. 13. fDAC calibration implementation details.

A. Modulating fDAC INL Calibration

The EVM of this modulation scheme can be strongly degraded in the presence of nonlinearities and gain errors in the digital-to-modulated phase conversion that occurs in both the DTC and the modulating fDAC. The DTC INL calibration as explained in Section II-D is readily re-used here. Indeed, during two-point FNSSPLL modulation the zero-crossing subsampling condition still holds, and the PD works within its linear range. The DTC input code and phase-error remain correlated in the presence of INL in the same way as in the synthesizer mode. The modulator's injection point-one (DTC) can, therefore, already be randomized and background calibrated (as explained in section II.D). We show next that a similar algorithm can be implemented for calibration of the modulating fDAC at injection point-two.

Nonliterary of the modulating fDAC arises due to capacitor mismatch and nonlinear capacitance-to-frequency conversion in the LC tank. We use an INL background calibration technique to linearize its behavior (Fig. 13). In the presence of nonlinearity (or gain error), the instantaneous frequency shift induced by the fDAC will be wrong, i.e., the modulated PLL output period will be larger or smaller than expected. This leads to the DTC sampling away from the ideal zero-crossing (late or early) and, consequently, to the transconductor injecting an error current into the loop filter. This current and its extracted sign is strongly correlated with the fDAC input code, and can be exploited for fDAC self-calibration (Fig. 13). To linearize the fDAC we use a predistorting 16 value LUT that linearly approximates between 256 unique fDAC inputs. To correctly correlate the PD error with the fDAC input code it is necessary to track the derivative of the PD error since the VCO integrates the phase and the modulation signal appears in the frequency domain. The correction coefficients are again gradually increased/decreased (depending on the PD sign) at appropriate addresses, until they converge to positions that cancel out the fDAC nonlinearity, i.e., where the PD output becomes a zero mean stream per particular fDAC input code. Since DTC and fDAC INL calibration loops cancel uncorrelated static errors independently of each other, they can run simultaneously in the background.

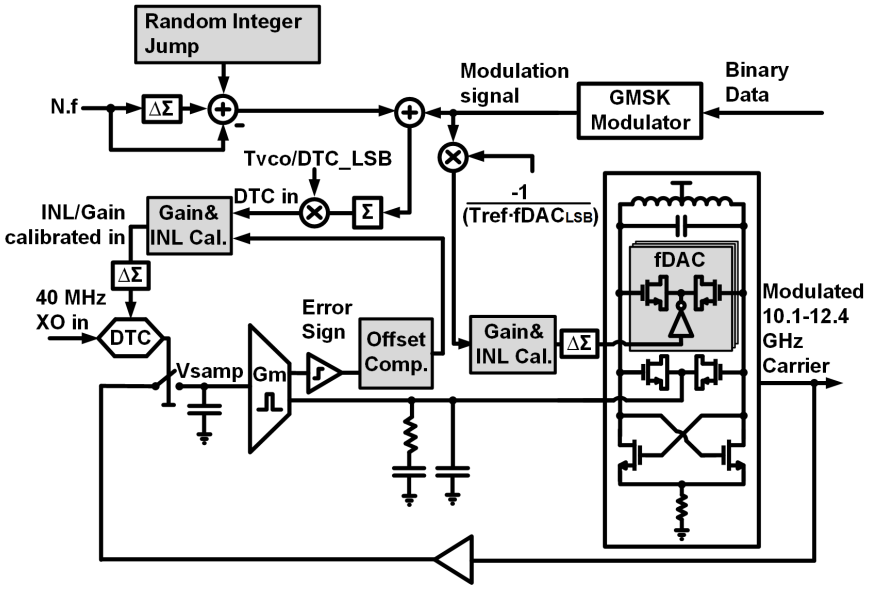


Fig. 14. DTC based FNSSPLL capable of self-calibrated fractional synthesis and two-point modulation.

As in the case of the DTC, correction for gain error of the fDAC is also inherently covered by this background calibration technique, since gain error also disturbs the zero-crossing condition of sampler. The LUT correction coefficients are simply adjusted in the background for appropriate gain-error cancellation, on top of the INL correction. Alternatively, a dedicated background calibration algorithm [17] can be enabled that serves only for initial gain calibration. The latter algorithm is used only for comparison purposes and it is not run in parallel to the presented one.

Besides the gain match and linearity requirements, accurate phase modulation necessitates minimal "delay spread" between the two injection points [17]. This effect originates from mismatch in the *time-instant* at which the modulation signal is injected into the two points. The intrinsic time mismatch in our design is constant and not data-dependent. Its value is approximately 150 ps, corresponding to the minimum DTC delay. A delay-spread cancellation algorithm similar to [17] has been implemented and is functional on chip, but the value of 150 ps is so small that even with this loop disabled it has negligible effect on the 10 Mbit/s GMSK modulation performance.

IV. Experimental Results

A complete system overview is depicted in Fig. 14. The prototype IC was fabricated in TSMC 28 nm bulk digital CMOS technology, with an active area of 0.25 mm^2 (Fig. 15). It operates on 0.9 V and 1.8 V supplies (IO interface and the Gm stage). Optionally, the VCO can be put in a high power/performance mode at a 1.4 V supply.

The frequency synthesizer consumes 5.6 mW in total, of which 1.8 mW is for the loop components, 2.7 mW for the VCO, and 1.1 mW for digital circuitry. The VCO tuning range is 10.1–12.4 GHz. The PLL output spectrum profile is first compared in modes with and without DTC

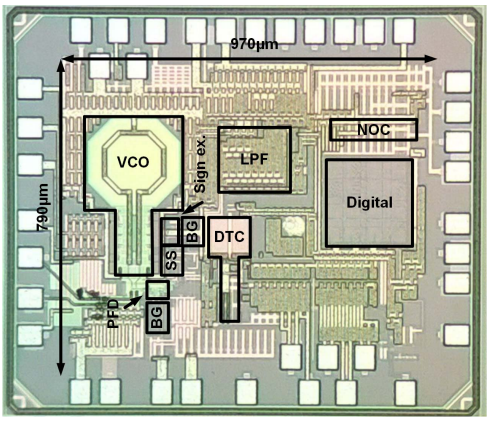


Fig. 15. Die microphotograph.

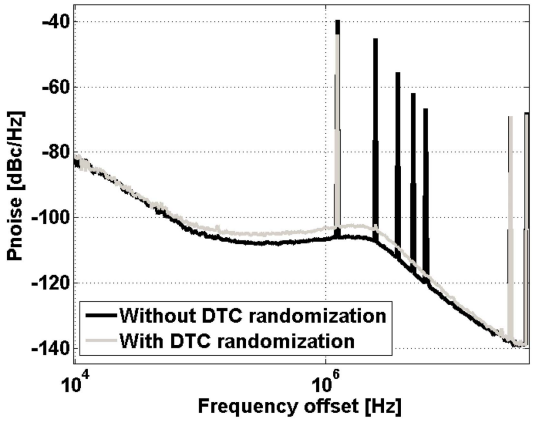


Fig. 16. Comparison between PLL output phase-noise profile without and with DTC random-jump. Spurs are indicated in dBc (the DTC INL calibration is not enabled).

Random-Jump (Fig. 16). A ~2 MHz BW was chosen as a compromise between VCO in-band noise suppression and reference path noise floor. As expected, turning the randomization

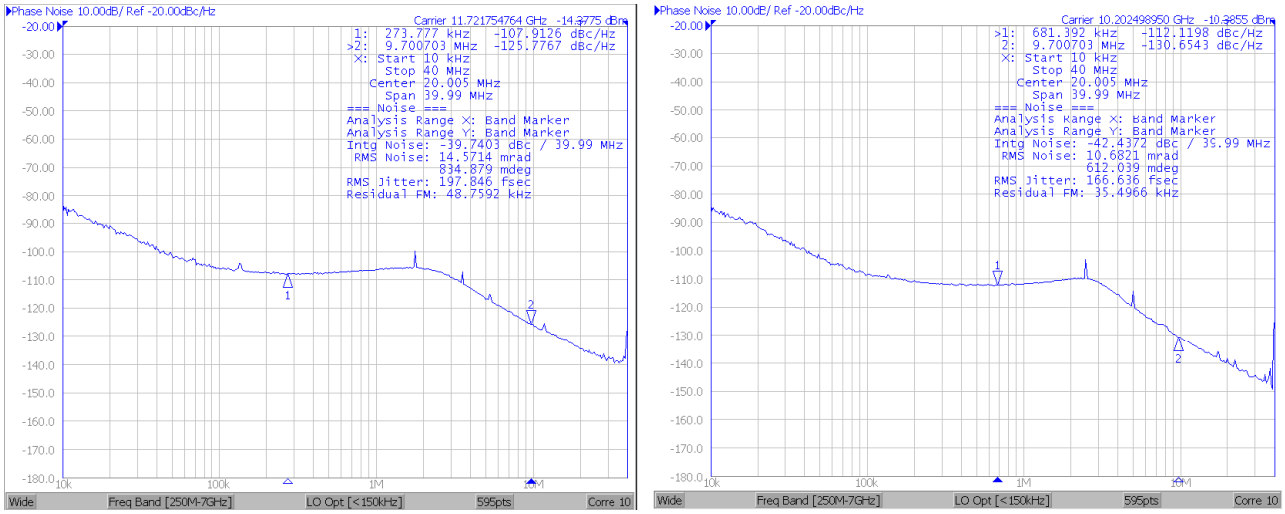


Fig. 17. Measured output phase noise profile: (a) low power VCO; (b) high power VCO. The integration range for RMS jitter calculation is 10 kHz–40 MHz and includes all spurs (including worst fractional and integer).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER RECENT PLLDESIGNS

	This work	Chen [32] ISSCC'15	Huang [33] ISSCC'14	Gao [45] ISSCC'16
Architecture	Subsampling Analog	Subsampling Digital	Subsampling Analog	Sampling Digital
Reference (MHz)	40	49.15	48	40
Output (GHz)	10.1-12.4	2.6-3.9	2.2-2.4	2.7-4.3
Tuning range (%)	20.4	40.0	8.7	46
Bandwidth (kHz)	1800	700	500	500[3]
In-band PN (dBc/Hz)[1]	-107.9	-97.8	-97.9	-99.4[3]
Ref. spur (dBc)	-69	-60	-55	-78
Worst fractional spur (dBc)	-56.6	-62	-53	-54
RMS jitter (fs) frac-N best/worst	176/197 (10k-40M)	226/240 (1k-100M)	266/400 (10k-30M)	159/n.a. (10k-40M)
Power (mW)	5.6	11.5	17.3	8.2
FOM (dB) [2] **worst/best**	Frac-N:-246.6/-247.6 Int-N: -248.5	Frac-N:-241.8/-242.3/ Int-N: n.a.	Frac-N:-235.6/-239.1/ Int-N: n.a.	Frac-N: n.a./ -246.8 Int-N: n.a.
Area (mm^2)	0.25	0.23	0.75	0.3
Process (nm)	28	65	180	28

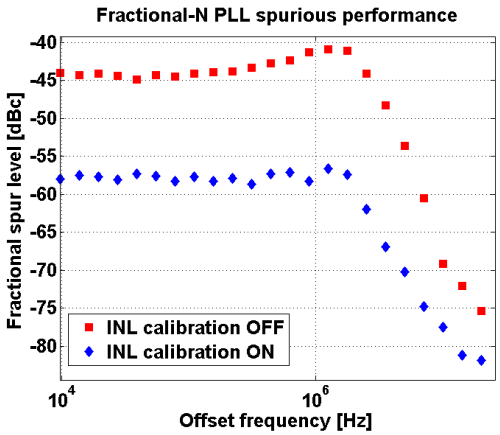
[1] Scaled to 11.72 GHz.

[2] $FOM_{PLL} = 10\,log_{10}\left[\left(\frac{\sigma^2_{t,PLL}}{1\,s}\right)\cdot\left(\frac{P_{PLL}}{1\,mW}\right)\right]$

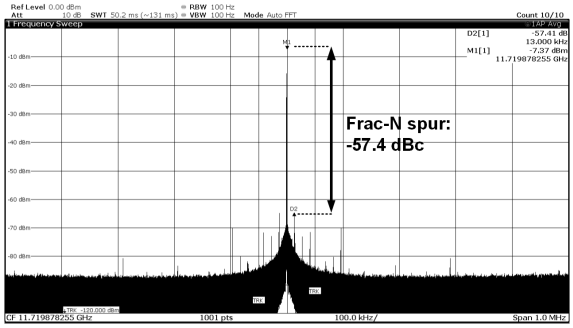
[3] Estimated from the source analyzer measurement.

algorithm on dithers the fractional spurs, spreading their power across the spectrum. Higher harmonics disappear and the fundamental spur decreases. The cost is, of course, a higher in-band noise floor.

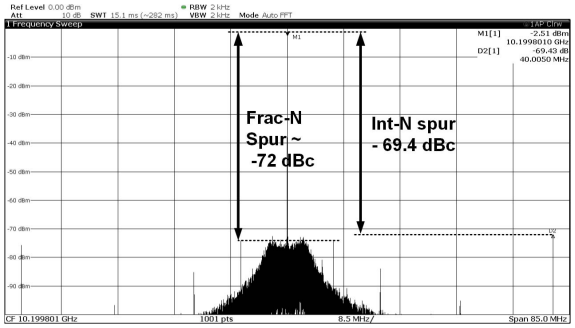
The background calibration of the DTC nonlinearity is enabled next, in parallel with the Random-Jump dithering and comparator offset compensation, which significantly improves the output spectral purity. The measured in-band phase noise around a close-to-integer fractional 11.72 GHz carrier is −107.9 dBc/Hz [Fig. 17(a)]. The measured RMS jitter is 198 fs with an integration range from 10 kHz to 40 MHz and all spurs (worst fractional and integer-N) included. In integer-N mode, the RMS jitter is 176 fs (only 22 fs below) which proves that the system's non-idealities were



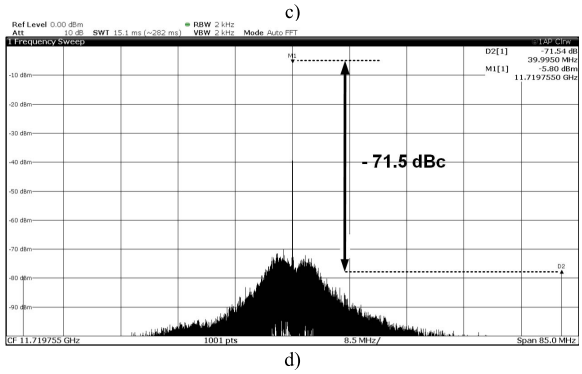
a)



b)



c)



d)

Fig. 18. (a) Fractional spur with and without calibration at different fractional offsets. (b) Spectrum analyzer output at a deep in-band fractional channel after calibration. (c) Spectrum analyzer plot at out-of-band fractional channel after calibration. (d) Spectrum analyzer plot at an integer-N channel.

well identified and successfully mitigated in this design. The measured spurious performance is shown in Fig. 18. The worst fractional spur before calibration appears at −41 dBc but drops by 15.6 dB after calibration to −56.6 dBc. The reference spur is at −69 dBc. The PLL achieves a competitive −246.6/−247.6 dB FOM (worst case/best case fractional-N mode), where $FOM_{PLL} = 10\log_{10}[(\frac{\sigma^2_{t,PLL}}{1\ s}) \cdot (\frac{P_{PLL}}{1\ mW})]$ as defined in [34]. Integer-N FOM, with the digital circuitry disabled is −248.5 dB. Moreover, the PLL can run in high-performance mode where the VCO operates at up to 22.4 mW from a 1.4. V supply [Fig. 17(b)]. The RMS jitter (all spurs included) is then between 167 and 147 fs for worst case fractional and integer-N mode. The small 20 fs difference, or 1 dB in terms of total integrated phase noise, shows again a well-calibrated environment. The in-band phase noise drops to −113.1 dBc/Hz. Due to excessive VCO power consumption, the FOM is now reduced to −242.6/−241.5 dB in the worst/best case. A summary of the PLL performance and comparison with other similar work [32], [33], [45] is depicted in Table I.

During modulation we operate the VCO in high power mode. The modulating fDAC was mistakenly designed to produce ∼ 5 times larger LSB than targeted (241 kHz/LSB instead 50 kHz/LSB) at low power i.e. at low output VCO swings. By running the VCO in high power mode (6.4–22.4 mW), the LSB reduces to 113–83 kHz/LSB. This is due to an increased swing at the VCO output which minimizes the effective ΔC [fF] of a digital cell [46] in the modulating fDAC. With a higher power consumption cost we ensure that the fDAC quantization noise does not limit the EVM performance. Fig. 19 shows the measured 10 Mb/s GMSK spectrum and constellation with all the background calibration algorithms enabled, around a fractional carrier close to 10.24 GHz. The modulated output has an undistorted spectral profile with bandwidth larger than 10 MHz even though the PLL loop BW is approximately 2.5 MHz. The best EVM RMS with DTC/DAC calibration is at −40.5 dB, which is only 1.9 dB above the fundamental limit of the total integrated phase-noise of a high-power mode synthesizer. Notably, EVM scales with $20\log_{10}(N)$, which means that the modulator would provide −49.6 dB EVM at 3.6 GHz. To prove the importance of calibration we show EVM at different fractional offsets (Fig. 20) with and without calibration. Using only gain correction results on average in 8 dB EVM improvement. The DTC and fDAC INL calibration results in additional 7 dB EVM improvement (6 dB after DTC calibration and then additional 1 dB after fDAC calibration). Enabling the delay spread algorithm does not change the results, as predicted. The DTC INL calibration proves to have a larger impact on the overall system performance. The overall performance overview and comparison to [17], [47], [48], [49] is given in Table II, with a note that this phase modulator's EVM is state-of-the-art and exceeds similar work.

V. Conclusion

We have presented a DTC-based FNSSPLL that achieves state-of-the-art performance during synthesis (−246.6/−247.6 dB FOM worst case/best case fractional-N mode) and wide-band, 10 Mb/s GMSK modulation (–40.5 dB EVM around a 10 GHz carrier) in 28 nm CMOS. This performance is

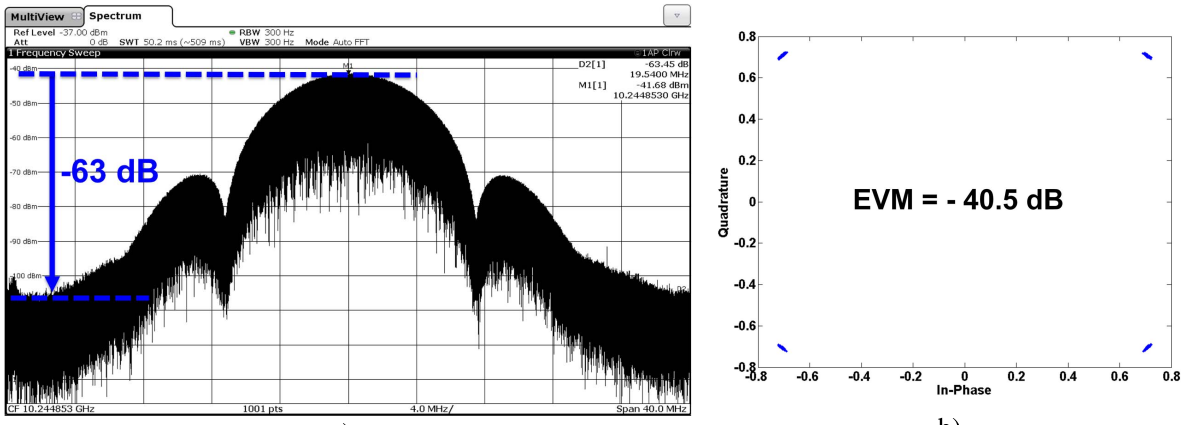


Fig. 19. GMSK spectrum and EVM with self-calibration enabled (10 Mb/s, close to a 10.24 GHz fractional carrier).

TABLE II

PERFORMANCE SUMMARY AND COMPARISON WITH OTHER RECENT PLL BASED MODULATOR DESIGNS

	This work (low VCO power)	This work (high VCO power)	Marzin [17] JSSC'12	Li [47] IWS'12	Shanan [48] ISSCC'09	Xu [49] JSSC'14
Architecture	Direct-FM		Direct-FM	Direct-FM	Direct-FM	Direct-FM
Clock frequency (MHz)	40		40	n.a.	52	26
Output (GHz)	10.1-12.4		2.9-4.0	1.5-1.8	2.4	1.7-2.1
Power dissipation (mW)	8.1	25.4	5	10	16	6.9
Modulation Type	GMSK		GMSK	GMSK	GMSK	GMSK
Data rate (Mb/s)	10		10	10	2	1.08
Energy/bit (nJ/bit)	0.8	2.5	0.5	1	8	6.4
Total Integrated Phase-Noise (dBc) [1]	-41.7	-42.4	-29.9	n.a.	n.a.	-20.3
EVM RMS (dB) [1]	-37.4	-40.5	-26.9	n.a.	-5.4	-13.9
Out of band emission (dBr)	-55	-63	-56	n.a.	n.a.	n.a.
Area (mm^2)	0.25		0.5	0.5	1.1	0.49
Process (nm)	28		65	65	180	65

[1] Scaled to 10.24 GHz

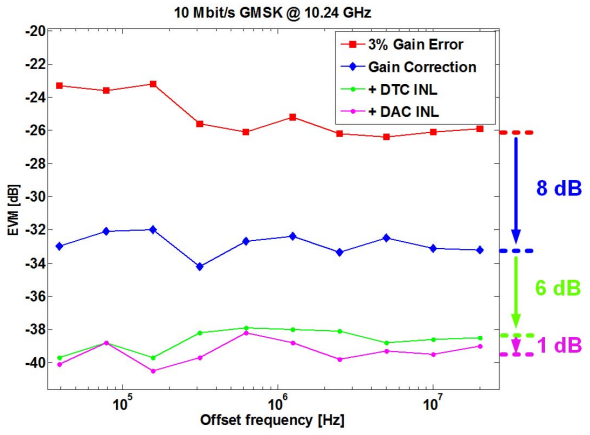


Fig. 20. EVM across different fractional offsets around a 10.24 GHz carrier without and with self-calibration.

derived from the analog subsampling phase-error detection core and efficient digital background calibration. This PLL can be used for low-power, low-noise LO synthesis. In the modulator mode, the system prototype offers an attractive solution for accurate, wideband phase modulation that can be used as part of a polar transmitter.

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