A 16nm 69dB SNDR 300MSps ADC with Capacitive Reference Stabilization

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Abstract

We present a 300 MSps 2 times interleaved pipelined SAR ADC in 16nm digital CMOS. It implements a new scheme to cancel reference voltage ripple due to DAC switching, greatly reducing requirements for decoupling capacitance and/or reference buffering, and achieves better than 76dB harmonic distortion. At 300 MSps, the peak ENOB is 11.2 bit with a power consumption of 3.6mW.

Introduction

Capacitive SAR architectures are among the most energy-efficient ADCs for medium resolutions and speeds [1]. With pipelining, interleaving, and digital calibration enhancements, accuracies up to 12 bit ENOB and speeds of several hundred MHz have been demonstrated [2]. However, the switching of the capacitive DAC during the SAR algorithm poses tough constraints on the reference voltages. For each conversion step, the DAC draws a *signal-dependent* charge from the reference, on which a very stable voltage must be maintained. Incomplete settling translates into modulation of the reference voltage which appears as harmonic distortion in the ADC output. Either high-speed reference buffers [3], or large decoupling capacitance [2] can be used, but at the expense of significant power consumption or area. We propose an alternative approach with an auxiliary DAC that makes the load on the reference *signal-independent*. This technique stabilizes the reference with only a small power and area cost. Unlike other approaches (e.g., [4][5]), it is compatible with most traditional DAC topologies.

Capacitive reference stabilization

Illustrated in Fig. 1, the basic concept is to cancel the signal-dependent ripple on the reference voltage due to DAC switching by ensuring that the charge drawn from the reference becomes code-independent. The nominal reference voltage V_{ref0} is sampled onto a charge reservoir C_{ref}. Then, when the DAC switches, a completely discharged auxiliary capacitor C_{aux} is connected to the reference node so that an extra charge Q_{aux} is drawn from C_{ref}. By selecting the appropriate value for C_{aux} per code, the sum of the charge drawn by the DAC and Q_{aux} is made constant over all DAC codes. As a result, the reference voltage drops to $V_{ref,final}$ independent of the DAC code, eliminating any signal-dependent ripple on the reference voltage.

Our implementation of this technique is shown in Fig. 2. Since the required value of C_{aux} is a very nonlinear function of the DAC code, and very susceptible to parasitics, C_{aux} is constructed as a DAC with a unit equal to $1/4^{th}$ of the unit size of the main DAC, and a look-up table that maps each DAC code to the correct setting for C_{aux}. To determine the values for the look-up table, a reference comparator with built-in offset (Ref. cmp) compares the stabilized reference voltage $V_{ref,final}$ after the amplification with the nominal reference level V_{ref0} as shown in Fig. 2. Its output is monitored in the background per DAC code and a calibration engine updates the values of the look-up table accordingly.

It is important to notice that also resetting the DAC to its initial state is signal-dependent. Hence, a second auxiliary capacitor C_{reset} is connected to the reference node during reset. The required value for C_{reset} is related to the DAC code by a simple piecewise linear function, and is also less critical for the overall linearity. Therefore, a decoder rather than another look-up table is used for C_{reset}.

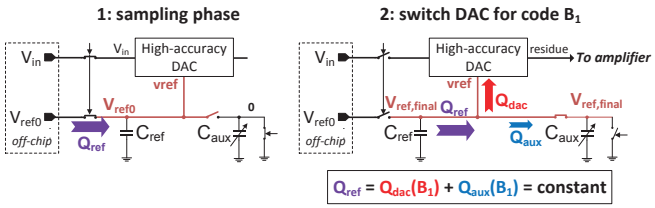

Fig. 1 Basic principle for cancelling reference voltage ripple.

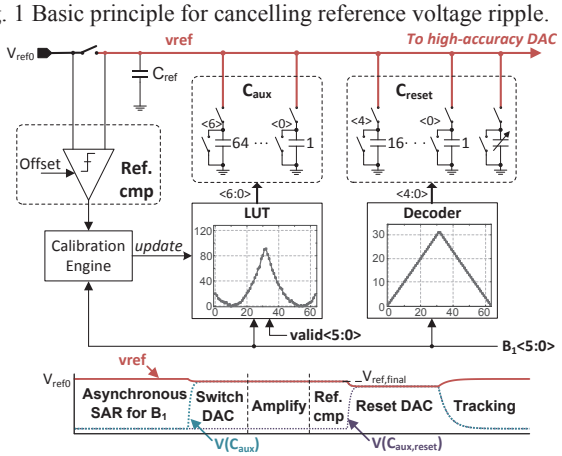

Fig. 2 Implementation of reference stabilization scheme (top) with timing and signal diagram (bottom).

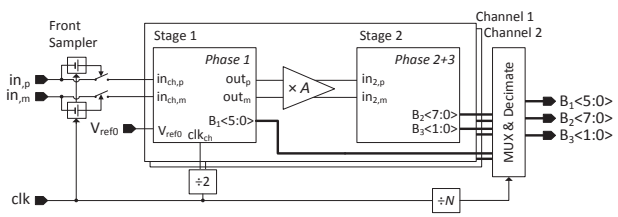

Fig. 3 Architecture overview of the ADC.

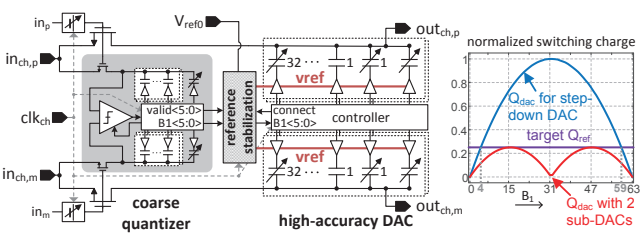

Fig. 4 Simplified schematics of the first stage with the switching energy of the high-accuracy DAC compared to a step-down DAC.

ADC architecture and design

Fig. 3 shows a block diagram of the complete ADC. A full-rate front sampler with bootstrapping is used to minimize clock skew between the two interleaved channels. Each channel consists of a first SAR stage which resolves 6 bits, a dynamic amplifier, and a second SAR stage which first resolves 8 bits and

then uses low-noise comparisons to generate 2 extra bits. Taking into account the redundancy between the different phases, the total quantization level becomes 13.5 bit.

Details of the first stage are depicted in Fig. 4. It contains a coarse 6-bit asynchronous SAR quantizer which determines the DAC code B_1 used by a high-accuracy DAC to generate the residue. Since only the linearity of this residue is important for the overall linearity of the ADC, the reference of the high-accuracy DAC is stabilized using the proposed technique.

Parallel switches sample the signal onto the coarse and high-accuracy DACs. The parallel switches are driven by the same control signal and sized to match the input-path time constants for the 2 paths to within 6-bit accuracy. These control signals are bootstrapped with a tunable bootstrap voltage to eliminate bandwidth mismatches between the 2 channels [2]. Also, the DAC of the coarse SAR quantizer contains a tunable capacitor connected to ground which allows it to match its signal range with that of the high-accuracy DAC. However, due to higher than expected layout parasitics, the reference voltage has been lowered to 610mV in measurements to match the input ranges.

The 4pF (single-ended) high-accuracy DAC is split into 2 sub-DACs for the positive and negative parts of the input range. This configuration is chosen to reduce the switching energy as shown in the right side of Fig. 4 where the charge drawn from the reference when switching the DAC with the 2 sub-DACs is compared with that obtained from a more traditional step-down DAC [2]. Several tunable capacitors are connected to the top plate of the high-accuracy DAC in order to correct for various sources of error. Calibration of the first 3 MSBs is done to lower the odd-order harmonic distortion. Also, gain mismatch between the 2 sub-DACs is calibrated to reduce even-order harmonic distortion. Finally, gain mismatch between the channels is calibrated to eliminate interleaving spurs.

The look-up table used to map the DAC code B_1 to the correct setting for C_{aux} has been optimized for minimum latency (one mux delay) by decoding the address bits B_1 concurrently with the coarse asynchronous SAR algorithm [6]. From simulations, the total energy required for the reference stabilization scheme of Fig. 2 including the reading energy from the look-up table is less than 5% of the total conversion energy.

The residue is amplified by a complementary dynamic amplifier [2] with enhanced CMRR. The 16nm FinFET technology permits a larger gain of 8 without linearity degradation. The gain is slightly larger than nominal to compensate for the drop of the reference voltage from V_{ref0} to $V_{ref,final}$. The second stage uses a step-down DAC as in [2] that does not need reference stabilization to achieve accuracy at a 9-bit level.

Measurement results

The ADC prototype has been fabricated in a 1P11M 16nm digital CMOS process and has a core area of 350 x 325µm^2 as shown in Fig. 6. The reference stabilization scheme of Fig. 2 including the charge reservoir C_{ref} of 50pF occupies about 16% of this area. There is no extra decoupling capacitance on the reference. Core supply is 800mV. Except for the values in the look-up table for the reference stabilization, all calibration is run off-line via Matlab control [2].

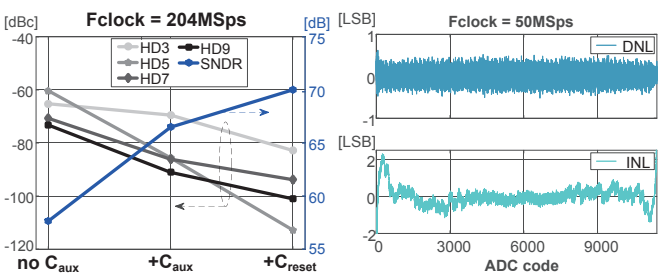

Fig. 5 Effect of C_{aux} and C_{reset} on harmonic spurs and SNDR for f_{in} = 30MHz (left) and ADC DNL and INL (right).

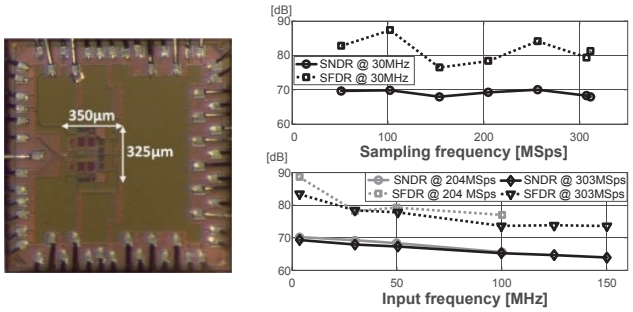

Fig. 6 Chip micrograph (left) and SNDR/SFDR for different input and clock frequencies (right).

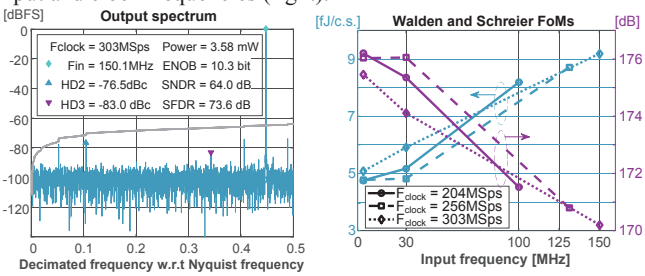

Fig. 7 Decimated output spectrum for f_{clock} = 303MSps (left) and efficiency for different input and sampling frequencies (right).

The reduction of the harmonic spurs by the proposed technique is shown in Fig. 5, which compares the odd-order harmonic tones without any auxiliary DAC, with the operation of only C_{aux} and also with both C_{aux} and C_{reset} operating. The last one suppresses the spurs below 80dBFS.

The right side of Fig. 6 shows that the ADC achieves a low-frequency SNDR of 70.2dB at 204MSps and of 69.3dB at 303MSps. With a Nyquist input, this reduces to 65.6dB and 64.0dB, respectively. The corresponding SFDR is 74.1/73.6dB which is limited by non-harmonic spurs as illustrated by the spectrum of Fig. 7. Power consumption is 3.6mW at 303MSps which results in peak Walden and Schreier Figures-of-Merit (FoMs) of 5.1fJ/conv.step and 175.5dB. For high-frequency inputs, the FoMs become 9.2fJ/conv.step and 170.2dB. These results indicate that the proposed reference stabilization technique is a viable solution for high-performance SAR-based ADCs with reduced area.

References

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