A Single-Channel, 600Msps, 12bit, Ringamp-Based Pipelined ADC in 28nm CMOS

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Abstract

A pipelined ADC is presented that exploits the low but very constant (over output swing) open-loop gain characteristic of the ring amplifier (ringamp) to achieve high SFDR in low-voltage nanoscale CMOS designs. A dynamic ringamp biasing scheme using CMOS resistors and an active ringamp-based common-mode feedback (CMFB) are also introduced. The implemented prototype achieves 56.3dB SNDR and 69.2dB SFDR at 600Msps, consuming 14.2mW from a 0.9V supply, resulting in a Figure-of-Merit (FoM) of 44.3fJ/conv.-step.

Introduction

For many ADC architectures the use of amplification imposes a limit on efficiency. This bottleneck explains much of the current FoM gap observed between amplifier-less architectures like SAR versus amplifier-based ones such as pipelined and delta-sigma. Yet, at the constantly expanding boundary of high-speed, high-accuracy ADC performance, amplifier-based solutions are often the only viable option.

Ring amplification suggests a new approach to building high-efficiency scalable amplifiers [1]. While its merit for high accuracy has already been demonstrated [2][3], its potential for high speed remains relatively unexplored. In this paper we demonstrate a highly efficient, single-channel, 600Msps, 12bit pipelined ADC in 28nm, which constitutes the highest-speed ringamp-based ADC implementation reported to date.

Architecture and Main-Path Ringamp Structure

The top-level view of the ADC is shown in Fig. 1 along with a simplified schematic of the pipeline stages. To maximize speed, a pseudo-differential 1.5b flip-around multiplying DAC (MDAC) is used for stages 1-10 (with downscaling to save power), followed by a 2b backend flash. In each stage two "main-path" ringamps amplify the MDAC residue to the output, while a separate single-ended "common-mode path" ringamp controls the common-mode (CM) level.

Fig. 2 shows the main-path ringamp introduced in this work. It is based on the self-biased scheme of [4], but uses a CMOS resistor instead of a fixed-value passive one, which provides several benefits. First, it allows the ringamp biasing to be adjusted post-fabrication via the gate biases $V_{BIAS,H}$ and $V_{BIAS,L}$. Second, simulations show that the CMOS resistor gives faster dynamic stabilization than a fixed resistor. Third, the CMOS resistor can be switched to a high impedance state during Φ_S, when the ringamp is idle and can be powered down, making it possible to use small pull-up/down transistors to disconnect the ringamp from the output without impacting speed or linearity and ensuring a signal-independent state.

Exploiting the Properties of Ringamp Open-Loop Gain

To minimize distortion while maximizing bandwidth, most high-speed pipelined ADCs resort to single-stage amplifiers operating at e.g. 2.5V [5] or 1.8V [6] to provide enough swing. In this design, the main-path ringamps are biased so that their output stages will settle into weak inversion (WI) during steady state, as in [2-4]. Although amplifier gain is low in nanoscale CMOS, a key property of this biasing is that the ringamp open-loop (OL) gain is reasonably constant across a wide output swing. To illustrate this, Fig. 3 compares the ringamp OL gain characteristics and linearity simulated in a unity-gain SHA circuit with those of a best-design-effort 2-stage Miller-OTA with the same gain and optimized for output swing and speed. Notably, the ringamp has a flatter gain characteristic across a wider range (with significantly higher speed and less power).

An ideally flat OL gain vs. output swing characteristic will result in a simple first-order gain error when the amplifier is placed in feedback, enabling high linearity to be achieved even with a low-gain amplifier. In the SHA example of Fig. 3, despite an OL gain of only 42dB in the ringamps, an overall stage linearity of 72dB is achieved (vs. just 61dB for the OTA). In the implemented ADC this is exploited by calibrating the stage gain coefficients applied during digital reconstruction from the ideal value of 2 to the best-fit radix value. Supply and temperature variations can also affect this value and should be tracked by a background calibration such as the scheme of [7]. In this work, for demonstration purposes, we determine the stage gain coefficients using an off-chip foreground calibration.

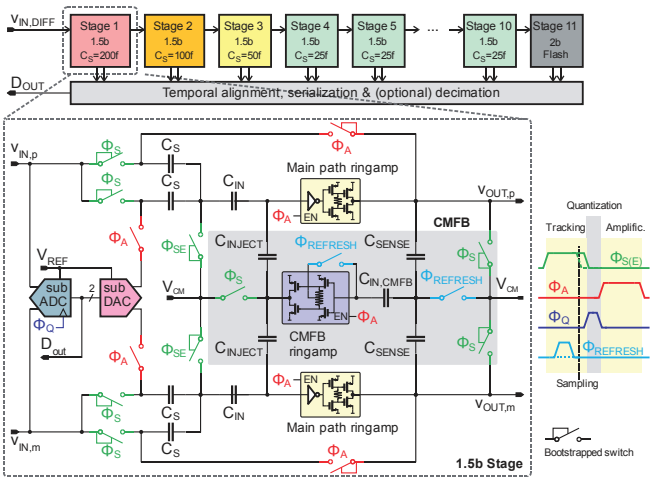

Fig. 1: ADC structure (top) and 1.5b stage schematic (bottom).

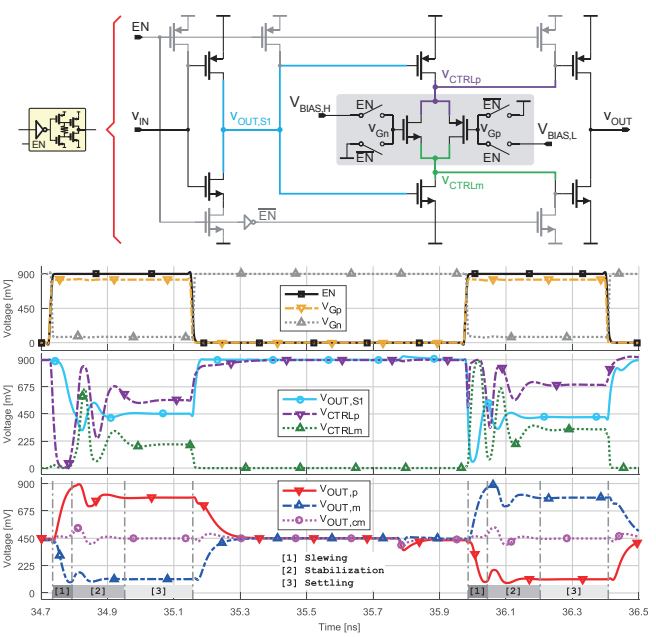

Fig. 2: Main-path ringamp with adjustable bias and power-down features (top), and operating waveforms within an MDAC (bottom).

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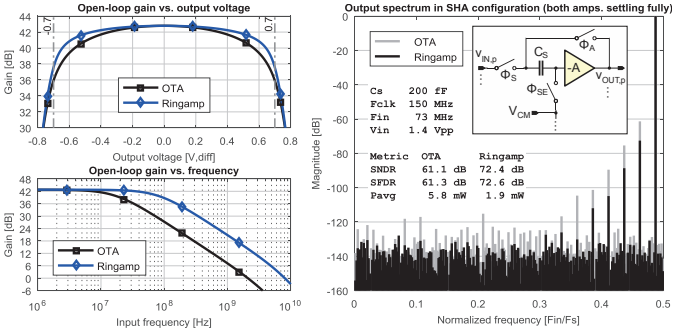

Fig. 3: Main-path ringamp vs. fully-diff. OTA: OL gain flatness & freq. response (left), and spectrum (w/full settling) in a SHA (right).

Ringamp-Based Common-Mode Feedback

Providing robust and accurate CMFB is a major challenge for ringamps, particularly in high-speed pseudo-differential implementations. As seen in the waveforms of Fig. 2, the MDAC output CM voltage during initial slewing and early stabilization is a poor predictor of the steady-state CM voltage; CMFB is only useful *after* the initial slewing, which leads to stringent CMFB bandwidth requirements. Passive capacitor-based CMFB schemes are attractive for this reason [1-4], but suffer from a tradeoff between CM accuracy, CM stability, and differential path efficiency, which results in a CMFB that is often not particularly robust. In Fig. 1 we introduce an active CMFB network which alleviates this tradeoff. It uses the 2-stage ringamp of Fig. 4 to generate gain in the CM-path. The static DC component of CM error is removed with the offset-canceling capacitors C_{IN} in Fig. 1 using a charge transfer scheme similar to [2], and the CMFB network actively cancels whatever remaining dynamic CM errors are present. To ensure stability, the CMFB ringamp is biased to have a large non-conduction "dead-zone" similar to [1] (in contrast, the main-path ringamps lack a true dead-zone, as they remain in WI). Due to this dead-zone, the high-gain, high-bandwidth CMFB rapidly drives the CM-level close to the target value and then self-limits, rather than fully settling to it. The result is a robust CMFB that holds the CM-level within an acceptable error range and rapidly eliminates any larger CM errors that arise.

Measurement results

The ADC is fabricated in a 1P9M 28nm CMOS technology (see Fig. 5) and operates entirely from a single 0.9V supply. The measured performance is illustrated in Fig. 6. At 600Msps, it achieves 56.3dB SNDR and 69.2dB SFDR with a total power consumption of 14.2mW, of which 4.9mW are consumed by the ringamps and 6.9mW by clocks and digital (see Fig. 5). The INL and DNL are 1.4LSB and 0.8LSB, respectively, and the CMFB is able to correct input CM variations above ±120mV. In Fig. 7 the performance is compared with other state-of-the-art single-channel ADCs. With Walden and Schreier FoMs of 44.3fJ/conv.-step and 159.5dB, respectively, this work achieves the highest power efficiency reported to date among single-channel ADCs of at least 500Msps and greater than 8ENOB, offering opportunities for the realization of power-efficient, multi-gigasample ADCs through interleaving.

References

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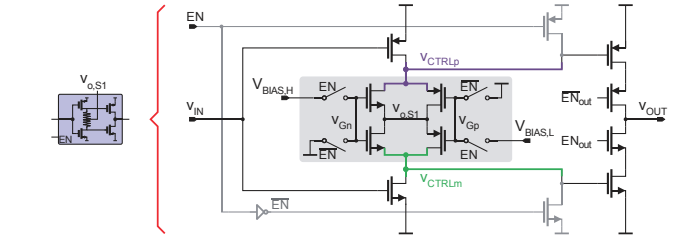

Fig. 4: Ring amplifier used in the active CMFB proposed in Fig. 1.

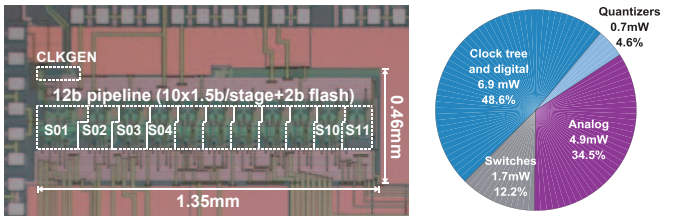

Fig. 5: Chip micrograph (left) and power breakdown (right).

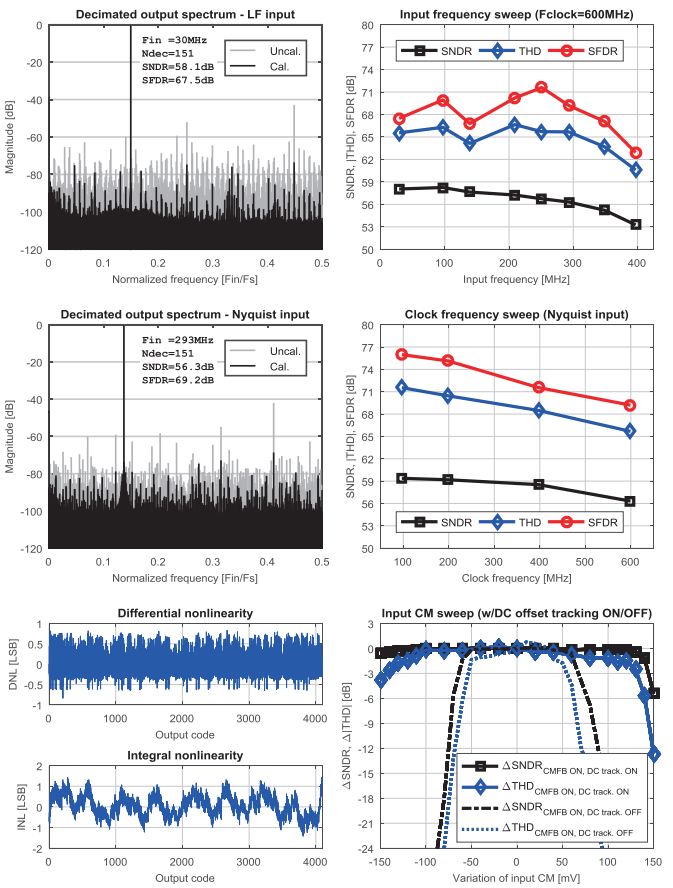

Fig. 6: Measured ADC performance.

		This work	VLSIC'16 A.M. Ali	ISSCC'15 El-Chammas	ISSCC'14 A.M. Ali	VLSIC'13 S. Wood	VLSIC'12 B. Sahoo	ISSCC'09 A. Verma
Resolution [bit]		**12**	14	14	14	10	11	10
Technology [m]		**28n**	28n	180n SiGe	65n	65n	65n	90n
Supplies [V]		**0.9**	2.5/1.8/0.9	3.3/1.8	3.3/2.5/1.2	1.0	1.2	1.2
Input range [V, pk-pk]		**1.6**	1.3	2.5	2.0	-	1.2	1.2
Sampling rate [sps]		**600M**	2.5G	500M	1G	800M	1G	500M
ERBW [Hz]		**350M**	1.5G	700M	1G	400M	330M	230M
ENOB [bit]	LF input	**9.4**	10.3	10.5	11.2	8.8	9.1	8.8
	Nyquist	**9.1**	10.0	10.3	11.0	8.4	8.4	8.5
SNDR [dB]	LF input	**58.1**	64	64.8	69	55	56.5	55
	Nyquist	**56.3**	61.7	64	68	52.2	52.4	53
SFDR [dB]	LF input	**67.5**	80	93	86	-	-	-
	Nyquist	**69.2**	73	82	82	60	60	56
Power [W]		**14.2m**	1150m	550m	1200m	19m	32.9m	55m
FoM_{Walden} [J/c.step]		**44.3f**	463f	849f	585f	71f	97f	301f
$FoM_{Schreier}$ [dB]		**159.5**	152.1	150.6	154.2	155.4	154.2	149.6
Core area [mm^2]		**0.62**	-	2.5	18	0.18	0.23	0.49

Fig. 7: Performance summary and comparison with state-of-the-art.