Wide-tuning range programmable threshold comparator using capacitive source-voltage shifting

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A comparator circuit with a built-in programmable threshold is proposed. The threshold is embedded by providing different initial source voltages to each of the input transistors. This source-voltage shifting is done by means of a tunable capacitance, which can synthesise a very wide range of initial voltages, even voltages beyond the supply. This results in a power-efficient comparator structure with a very wide programmable tuning range and low decision delay. The inherently small integrating capacitance of the structure allows for high speed operation even when using small device sizes, minimising input capacitance and maximising efficiency. A practical transistor-level implementation is simulated in a standard 16 nm CMOS technology on a 0.8 V supply, with a tuning range of at least ±568 mV.

Introduction: The ability to programme a threshold into a comparator is broadly useful in analogue and mixed signal circuits. Sometimes this programmability is used to cancel the comparator's process-dependent offset and tune it back to zero. In other cases, a non-zero threshold is explicitly desired. To name a few examples, built-in thresholds can be used to replace the reference ladder in a flash ADC [1], to perform a successive approximation by dynamically reconfiguring the threshold of a comparator [2, 3], or to do the same by using a tree of comparators with static thresholds [4]. In all these cases, a wide threshold tuning range is desirable, since it allows for larger signal ranges to be processed with better signal-to-noise ratio. It is furthermore advantageous if noise and speed are as constant and independent of the programmed threshold as possible, so that the comparator can be guaranteed to meet a target performance specification regardless of the particular configuration.

A common scheme for generating a programmable threshold is to place tunable capacitances or tunable current sources at the drain nodes of the input pair of the first stage of the comparator, and sense the difference in integrated voltage on these nodes with a latch [1, 2, 4]. For example, in Fig. 1, this can be done for the case of a tunable capacitance when C_1 and C_2 are tunable and the batteries are shorted such that $V_{B1} = V_{B2} = 0$. This approach is advantageous from a noise perspective because the capacitance is located at the signal integrating nodes and thus serves to reduce the comparator's input-referred noise, but it comes at the price of speed and/or larger device sizes and does not lead to a particularly wide or linear tuning range. The range is mainly limited by the dependence of the integrating current I_{DS} on that of the input, since $V_{GS} = V_{IN} - V_{DD}$. As I_{DS} varies roughly quadratically with respect to V_{IN}, expanding the tuning range requires a correspondingly quadratic increase in capacitance, and the ratio of C_{MAX}/C_{MIN} ultimately places a hard limit on the tuning range that can be achieved since it is usually only a fraction of the range of currents that can be provided by the input transistors across all possible inputs. By coupling the source nodes together with a current source transistor, it is possible to constrain I_{DS} and linearise the tuning characteristic [2], but this requires extra biasing headroom and for large inputs one input transistor will be biased in saturation while the other will be forced into weak inversion due to current limiting; additional drain capacitance tuning range will be of little help beyond this pinch-off point.

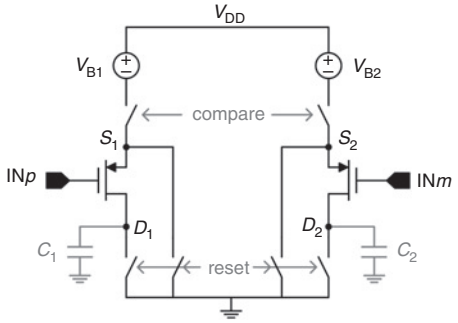

Fig. 1 *Input stage of two-stage comparator with tunable elements required for drain-capacitance weighting (C_1 and C_2) and source-voltage shifting (V_{B1} and V_{B2}). Reset and compare clocks are non-overlapping as in e.g. Fig. 2.*

Source-shifted comparator: Many of these limitations can be overcome by embedding the threshold as a set of tunable voltages at the source nodes [3]. In Fig. 1, this would be when the batteries V_{B1} and V_{B2} are independently tunable and the drain capacitances C_1 and C_2 are finite and equal. With equal-sized integrating capacitances at D_1 and D_2, the threshold will always lie at the operating point that makes the two branch currents equal. As a first example, suppose that $V_{B1} = V_{B2}$ (i.e. the systematic offset $V_{OS} = V_{B1} - V_{B2} = 0$) and the input is such that $V_{INp} - V_{INm} = 100\,\text{mV}$. In this condition, the voltage at D_2 will ramp up faster than D_1, and the comparator will make a '1' decision. However, if we also shift the source offsets by an equal amount relative to the input, that is, to say when $V_{OS} = 100\,\text{mV}$, the integrating currents are (to first order) equal and the comparator is at its metastability threshold. Notably, this direct relationship between the difference in source offsets and the resulting input-referred threshold is true for any common-mode input level, in contrast to the drain-capacitance tuning scheme discussed earlier or other offsetting schemes such as variable current sources [5]. Even though common-mode levels affect the absolute value of the current in each branch (and thus comparator decision speed), the *relative* relationship between the two branches as described above is invariant. Also, it is noteworthy that this source-shifting approach provides a relatively constant noise performance regardless of offset code due to the constant integration capacitances C_1 and C_2.

Capacitive source shifting: In this Letter, we propose to implement the source-voltage shift using a charge-redistribution capacitor DAC. One such circuit is shown in Fig. 3, where we use a step-down DAC and a two-stage comparator, though other DAC and comparator schemes following the same approach are also possible. The comparator operates using the three timing signals depicted in Fig. 2. During *reset*, the drain nodes D_1 and D_2 are discharged to V_{SS} while the source nodes S_1 and S_2 are pre-charged to V_{DD} (disconnecting from V_{DD} at the end of *reset*). Then, when the *shift* signal asserts, the capacitor arrays $C_{S1}[1:N]$ and $C_{S2}[1:N]$ are switched according to the applied digital codes $B_p[1:N]$ and $B_m[1:N]$ and redistribute the charge present at nodes S_1 and S_2. Note that the total capacitance at each node remains equal, maintaining capacitance symmetry independent of code and voltage asymmetry. With *shift* continuing to be asserted, the *compare* signal is then asserted. This connects S_1 and S_2 to the source nodes of the input pair transistors, and the two input branches begin integrating charge onto the capacitance present at nodes D_1 and D_2. When one of these nodes ramps high enough to cause current to conduct in one of the second-stage N-channel MOS input transistors, the second-stage latch regenerates and the decision is resolved at the output.

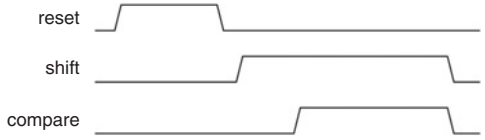

Fig. 2 *Example timing control for Figs. 1 and 3. 'Shift' signal is only used in Fig. 3*

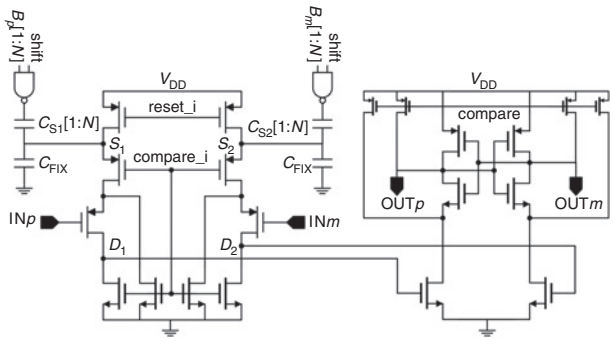

Fig. 3 *Proposed comparator circuit with source-voltage shifting implemented using charge-redistribution capacitor DACs*

The comparator of Fig. 2 is simulated in a 16 nm CMOS technology on a 0.8 V supply using estimated parasitics. An example transient waveform is shown in Fig. 4 for the case when the input voltage is

very close to the programmed threshold, i.e. near the metastability point. The input-referred threshold versus control code is shown in Fig. 5. Performance is summarised in Table 1. No optimisation for noise was made, the input capacitance was kept low by sizing the input transistors to be only 2× the minimum size, and the drain capacitances are only constituted of parasitics (to further reduce noise, a designer can choose to add additional capacitances to D_1 and D_2). For the nominal split-source comparator simulation (*SS-CMP Basic*), the control scheme for the two 8b step-down DACs is chosen, so that only one DAC will step down for any given code (Fig. 5). Note that for this coding scheme there will be a code-dependent common-mode voltage between the two source nodes, and thus code-dependent drain currents through the input pairs. Although there are downsides to this for certain applications, one benefit is that it leads to the shortest possible decision delay in the middle of the code range (e.g. the *MidCode* setting corresponding to zero threshold shift). However, as we can see in Table 1, at extremes of the code range (*MinCode*), the common mode is much lower due to the large programmed source shift, and the decision delay is consequently larger. If a common-mode invariant coding scheme were used, this code-dependent effect can be removed, but then the decision delay will be larger for all codes.

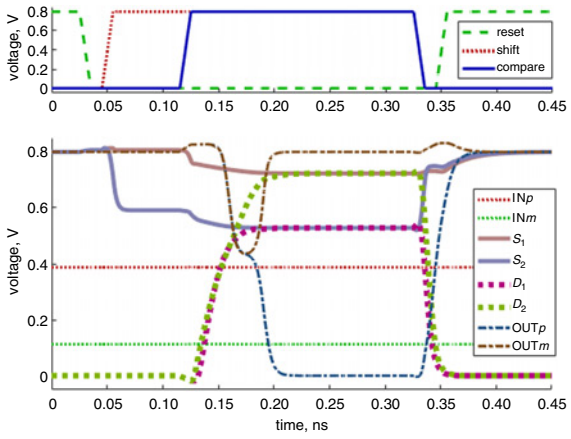

Fig. 4 *Example transient operation of circuit in Fig. 3 for configuration near threshold*

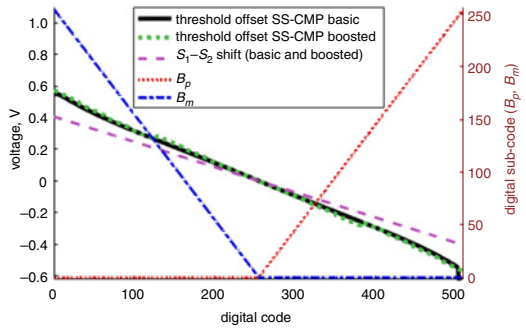

Fig. 5 *Programmed threshold versus digital control code applied to Fig. 3*

Table 1: Simulated performance for input 1 mV from threshold

	SS-CMP basic		SS-CMP boosted	
Tuning range	± 568 mV		± 589 mV	
	MinCode	MidCode	MinCode	MidCode
Threshold shift (mV)	568	0	589	0
Decision delay (ps)	185	46	62	46
Energy per conv. (fJ)	27	12	36	12
Noise (input-ref.) (mV)	1.6	1.5	1.7	1.5

Considering this, it is possible to extend the tuning range and/or decrease the worst-case decision delay by synthesising initial source voltages above the supply. This source boosting can be achieved with some simple modifications to the DACs, so that certain sub-elements step-up the voltage when selected instead of stepping down. We also report in Table 1 one such boosting scheme, where the MSB-1 and MSB-2 capacitors are set to operate in step-up. Nothing else is changed with respect to the 'SS-CMP Basic' case. For approximately the same tuning range, the worst-case decision delay is significantly reduced. Although the voltage at nodes S_1 and S_2 will now exceed V_{DD} for certain codes, if we choose all the transistors connected to those nodes to be standard-V_T doped, we can typically go beyond the supply by up to 150 mV without significant sub-threshold leakage.

A number of more subtle second-order effects and design optimisations are worth mentioning. First, unlike the ideal batteries in Fig. 1, the capacitor 'batteries' of Fig. 3 can only source a finite amount of charge, and the voltages at S_1 and S_2 will begin to droop from their initial values as they source current to the drain nodes. It is, therefore, advisable that the value of C_{S1} and C_{S2} be several times larger than the capacitance at D_1, D_2 such that this droop is minimised and speed and tuning range are not significantly impacted.

Second, ignoring parasitics, the source-shifting DAC can in theory synthesise any initial offsetting voltage between V_{DD} and V_{SS} at S_1 and S_2. However, the lower end of this range is not useful since the input pair transistors cannot conduct. Thus, to minimise the required DAC resolution for a given precision target, the tuning range can be adjusted to span only the desired range by adding an extra fixed capacitance C_{FIX} to each side.

Third, for certain applications where there are only two clocking phases available [2, 3], the addition of the extra *shift* clocking phase can complicate implementation or add to the critical delay path. However, in many cases only the comparator's decision delay is a part of the critical timing path [4]. In these situations, the extra phase is not a major concern or penalty.

Finally, from Fig. 5 note that the relation of V_{OS} ('$S_1 - S_2$ shift' in Fig. 5) to comparator threshold is not exactly one-to-one. This is primarily due to the very slightly different time that S_1 and S_2 connect and begin charging D_1 and D_2, as can be seen in Fig. 4. It is caused by the asymmetric, offset-dependent gate–source voltages across the two switches that allow charging to begin. Although this results in $V_{OS} < V_{INp} - V_{INm}$, the relationship between programmed offset and comparator threshold remains first-order linear and performance is not negatively affected.

Conclusion: Capacitive source-voltage shifting is a versatile and broadly applicable technique for building wide-tuning range programmable threshold comparators. The proposed switched capacitor implementation enables low-power, fully dynamic, digitally controlled operation with small device sizes and minimal input capacitance. A variety of coding and switching approaches are possible when programming voltages with a charge-sharing DAC, and schemes such as source-boosting can be used to further increase speed.

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One or more of the Figures in this Letter are available in colour online.

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