3.1 A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

Benjamin Hershberg, Davide Dermit, Barend van Liempd,
Ewout Martens, Nereo Markulic, Jorge Lagos, Jan Craninckx

imec, Leuven, Belgium

Giga-sample ADCs targeting high performance communication applications such as direct-RF sampling all rely on some form of residue amplification to minimize the number of interleaved channels and meet demanding specifications. Despite architectural efforts to reduce the total number of amplifiers in the system, the challenges associated with designing them for high bandwidth and linearity has limited reported power efficiencies [1]. In this work, we show that ring amplification [2] can overcome this longstanding bottleneck. In an architecture using 36 ringamps, the 3.2GS/s ADC consuming 61.3mW has a Nyquist SNDR of 61.7dB, SFDR of 73.3dB, Walden FoM of 19.2fJ/conv-step, and Schreier FoM of 165.9dB. Furthermore, we demonstrate a general technique whereby the signal-to-distortion ratio (SDR) of any amplifier in the system can be independently monitored in the background with an analog hardware overhead of only one comparator.

The top-level system details are provided in Fig. 3.1.1. The ADC input is buffered by an AC-coupled pseudo-differential class-AB push-pull source follower. A clock buffer converts a differential sine into a single-ended square. The ADC core consists of four interleaved pipeline channels, each containing nine scaled 1.5b MDAC stages followed by a 1.5b+3b backend.

The stage 1 MDAC of the channel is shown in Fig. 3.1.2. Here, we introduce a passive-hold mode into the operation of the MDAC. In the illustrated switching scheme, during φ_0 the voltage at node X will be $-\alpha V_{IN}$, where α represents attenuation due to parasitics. The sub-ADC is attached to node X, and uses this held value for quantization during φ_0. Because the charge sampled onto the MDAC capacitors (C_U) is used for both quantization and residue amplification, all skew and bandwidth related mismatch between the MDAC and sub-ADC is eliminated. This also eliminates the need for a dedicated sub-ADC sampling network, reducing the input buffer load. To minimize its parasitic influence on analog loop performance during φ_A, the sub-ADC comparator uses the source-shifted programmable threshold topology of [3] which gives low decision delay even with near-minimum sized input transistors.

The fully differential ring amplifier is illustrated in Fig. 3.1.3. Because it is only needed during φ_A, the structure is designed to support rapid power cycling. Stability is enforced with a CMOS resistor [4], which operates as a switch during power-down and a tunable bias control during normal operation. The effective resistance can be adjusted with the two charge-sharing DACs of Fig. 3.1.3. These set a trapped-charge bias voltage onto the gates of the CMOS resistor. The common-mode feedback (CMFB) of the ringamp consists of three feedback loops. Two of these loops operate on the trapped-charge present at floating node B1. This approach ensures correct biasing in the presence of kickback due to power cycling. Charge can only enter or exit node B1 through C_{SMALL}, and the first CMFB loop uses this slow injection path to regulate DC biasing. Per-cycle common-mode variations are suppressed by the fast second loop formed by C_{FB}. Transistors M_{CM1} and M_{CM2} form the third loop, and ensure stability by increasing phase margin.

To ensure optimal performance of the ringamps in the presence of PVT variation, a general technique for background measurement of SDR in switched capacitor feedback circuits is introduced in Fig. 3.1.4. It is based on the observation that the summing-node voltage V_X is equal to the input-referred error of V_{OUT}. A portion of this error is due to the finite gain of the amplifier (A_{OL}), and in [5] it is shown how repeated measurements of V_X and V_{OUT} can be used to estimate and correct for it. However, other well-known background calibration techniques can correct not only for finite gain error but also capacitor mismatch, so we are not directly concerned with the V_{OUT}/A_{OL} component of V_X in this work. Rather, we are interested in the remainder of V_X, which contains all other noise and distortion components of the feedback system – that is, SNDR. As described by the equations of Fig. 3.1.4, the estimated average open loop gain $\hat{A}_{OL}$ can be calculated with a linear regression, and after its removal from V_X, the SNDR can be estimated.

In a pipelined ADC, $D(V_{OUT})$ is already available in the pipeline's digital output. However, obtaining an accurate estimate of V_X requires additional hardware and is non-trivial due to the sensitivity of node X and the small amplitude of the signal – on the order of ~1mV. A direct approach using a high-resolution auxiliary ADC [5] is too complex and area-intensive to be practical for inclusion in each pipeline stage we wish to monitor.

An elegant alternative is to use a single-comparator stochastic ADC [6]. The procedure is summarized in Fig. 3.1.4. In an initial preparation step, the comparator is connected to an on-chip reference ladder, its threshold offset is nulled, and it is provided with several scaled reference values, e.g. $k \cdot V_{REF}/1024$, k = -3 to 3. The comparator output for each of these trials is used to determine its noise distribution in absolute terms (volts per sigma). In a second preparation step, the comparator is re-connected to node X and its threshold offset is again nulled while sampling V_X. Now the main measurement begins. As samples of V_X are quantized by the comparator, they are sorted with respect to $D(V_{OUT})$ into "bins". To reduce computational complexity, each bin processes a contiguous range of $D(V_{OUT})$ codes, rather than just one code per bin, without loss of final estimation accuracy. Sorting is simply a matter of demuxing with respect to the MSBs of $D(V_{OUT})$. Each bin computes the mean value of its binary input vector and converts this cumulative-distribution value to a corresponding probability-density "sigma" with the inverse error function. The output is then multiplied by the volts-per-sigma conversion factor acquired earlier and muxed with respect to $D(V_{OUT})$. The resulting output is an estimate of V_X that, due to the processing procedure, has been stripped of noise, but still contains a high accuracy estimate of all non-random errors. Consequently, the output of the estimator block becomes SDR rather than SNDR.

In Fig. 3.1.5 we show in measurement how this estimation technique is used to characterize the performance of the CH0, STG1 ringamp with respect to its digital bias control. For comparison, the THD of CH0, calculated from an FFT of its digital output, is overlaid. Considering that THD and SDR are not identical quantities, and that the THD also includes distortion from other stages in the channel, the correspondence between these two curves is very close. Also notable is the broad range of bias codes that give near-optimal performance, indicating that the ringamp is robust to variation.

The ADC is fabricated in a 16nm CMOS technology and occupies an active area of 0.194mm² (360µm × 540µm), excluding decoupling (Fig. 3.1.7). A single, fixed configuration of digital settings and stage gain correction coefficients (determined off-chip) are used in all measurements. Performance is summarized in Fig. 3.1.5 and Fig. 3.1.6. At 3.2GS/s, total power consumption is 61.3mW, with 11.2mW in the input buffer, 2.4mW in the clock buffer, and 11.9mW per channel. The references are 50mV and 800mV, allowing the ringamps to utilize 88% of the available 0.85V supply. In the input frequency sweep of Fig. 3.1.5, the dip in SFDR around 1GHz is dominated by HD3, and found to be packaging related. Compression near full-scale is due to input buffer HD3.

Compared to all ADCs above 1.7GS/s achieving SNDR > 51dB in [1], this work achieves the highest reported SNDR at Nyquist and advances the Walden and Schreier FoM state-of-the-art by 8× and 12dB respectively. This is made possible not only by the direct performance advantages of ring amplifiers, but also the indirect advantage of greater design freedom when amplification is relaxed as an architectural constraint.

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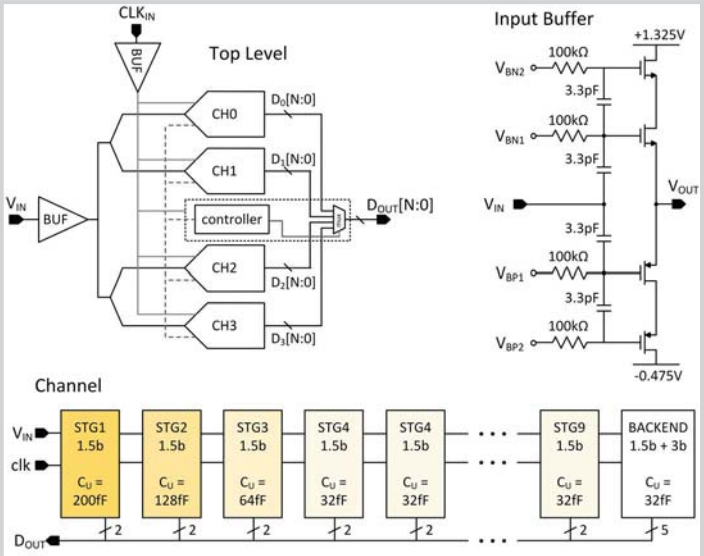


Figure 3.1.1: Top-level architecture.

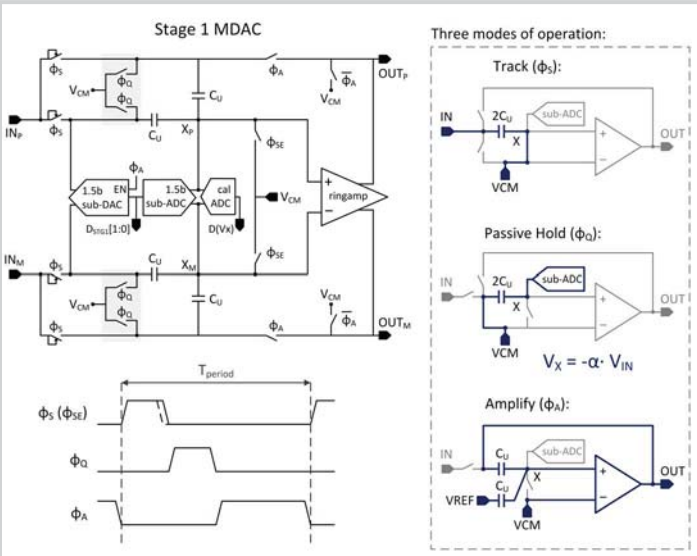


Figure 3.1.2: Merged MDAC and sub-ADC with passive hold mode.

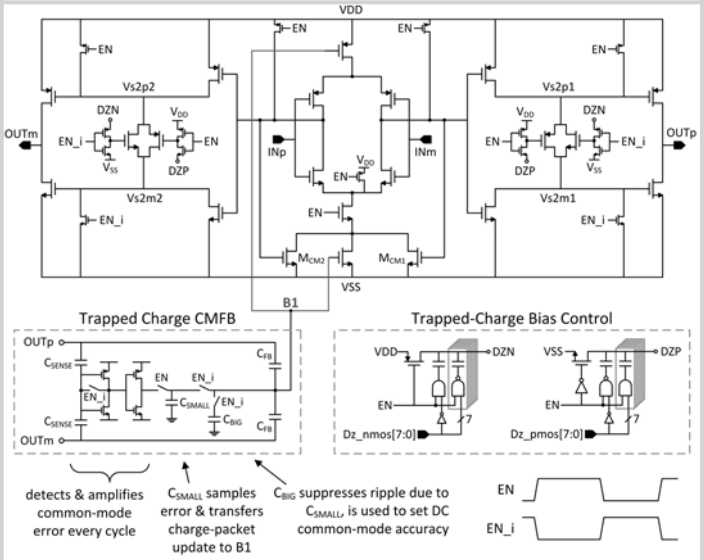


Figure 3.1.3: Fully differential ring amplifier.

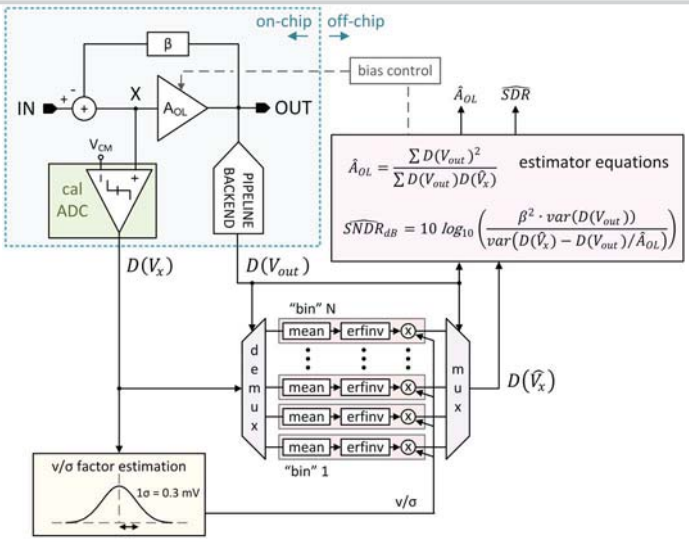


Figure 3.1.4: Method for background estimation of signal-to-distortion ratio (SDR).

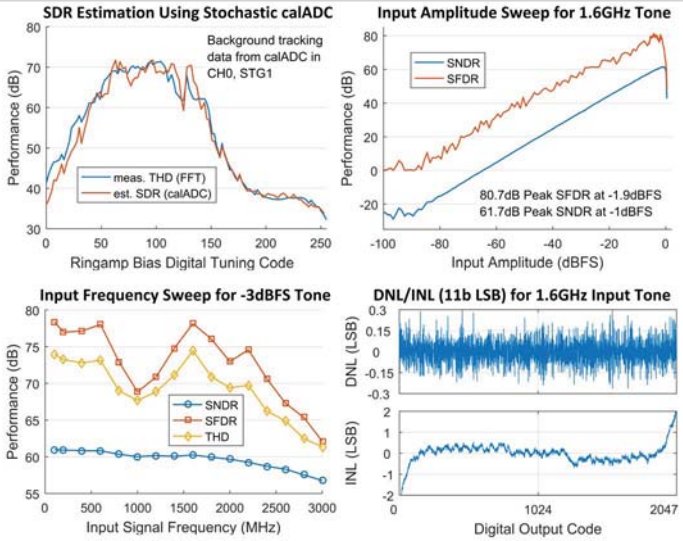
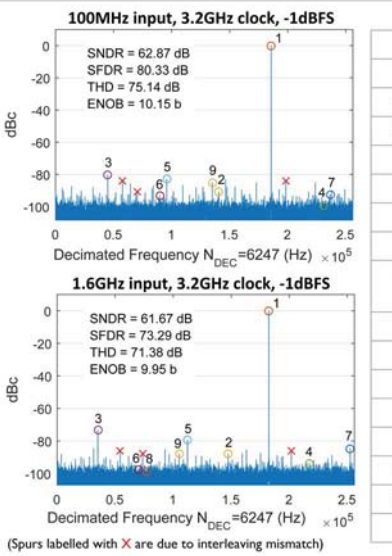


Figure 3.1.5: Demonstration of SDR measurement and key performance metrics.



Performance Summary

Technology	16nm CMOS	
Core Supply	0.85 V	
Buffer Supply	1.8 V	
Sampling rate	3.2 GS/s	
Interleave	4x	
Resolution	13 b	
Input Range	1.5 V pk-pk diff.	
Calibration	static 1st order stage gain	
Performance at -1dBFS:	*100 MHz input:*	*1.6 GHz input:*
ENOB	10.15 b	9.95 b
SNDR	62.9 dB	61.7 dB
SFDR	80.3 dB	73.3 dB
THD	75.1 dB	71.4 dB
Power	61.3 mW	
Walden FoM	19.3 fJ/c-step	
Schreier FoM	165.9 dB	
Active Area	0.194 mm^2	

Figure 3.1.6: Spectrums for LF/HF inputs and performance summary.

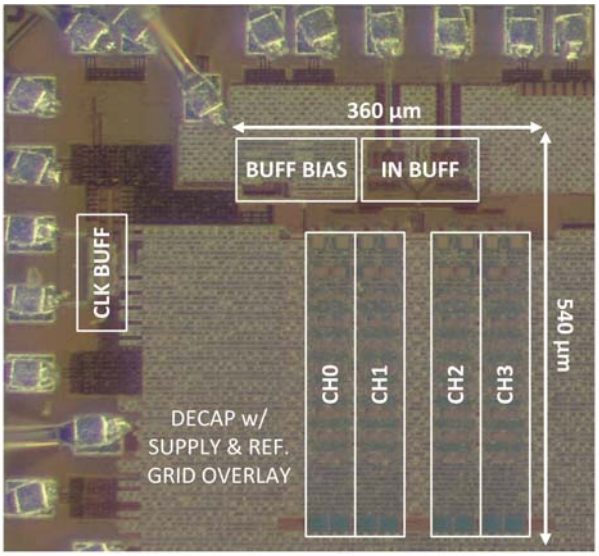


Figure 3.1.7: Chip micrograph.

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