A Single-Channel, 600-MS/s, 12-b, Ringamp-Based Pipelined ADC in 28-nm CMOS

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***Abstract*— Achieving high linearity and bandwidth with good power efficiency makes the design of ADCs in deep nanoscale CMOS processes very challenging, as the constraints of low-voltage operation and limited intrinsic gain often dictate the use of power-consuming analog circuits and intensive digital calibration. This paper addresses these problems by introducing a pipelined ADC that exploits the low but very constant open-loop gain versus output voltage characteristic of the ring amplifier (ringamp) to achieve both high speed and linearity in low-voltage nanoscale CMOS designs. A tunable ringamp biasing scheme using an anti-parallel arrangement of CMOS transistors and an active ringamp-based common-mode feedback are also introduced. A single-channel prototype ADC is implemented in a standard 28-nm CMOS process, achieving 58.7-dB SNDR and 72.4-dB SFDR at 600 MS/s while consuming 14.5 mW from a single 0.9-V supply, resulting in Walden and Schreier figure-of-merit (FoM) values of 34.4 fJ/conv.-step and 161.9 dB, respectively.**

***Index Terms*— Active common-mode feedback (CMFB), gain calibration, pipelined ADC, ring amplifier (ringamp), single channel.**

I. Introduction

THE ever-increasing demand for higher data throughput that pushes the boundary of ADC performance has fueled the development of converters that seek to simultaneously maximize both linearity and bandwidth (BW). Typical applications that benefit from such ADCs include software-defined radios, cellular base stations, satellite and radar receivers, cable TV set-top units, and instrumentation equipment. The adoption of wide-BW, high-speed data converters in these applications provides benefits not only in terms of system complexity reduction but also in terms of reconfigurability, encouraged by the availability of cheap digital processing power in deeply scaled CMOS processes.

ADCs targeting the above requirements often rely heavily on the use of time interleaving (TI) and digital calibration [1]–[9]. These techniques are used to overcome the intrinsic speed and linearity limits of the technology and to correct the artifacts arising from TI itself [10]. However, since the complexity of TI calibration grows rapidly with the number of interleaved channels, the maximization of the per-channel speed becomes of paramount importance for the implementation of ADCs with high linearity and BW.

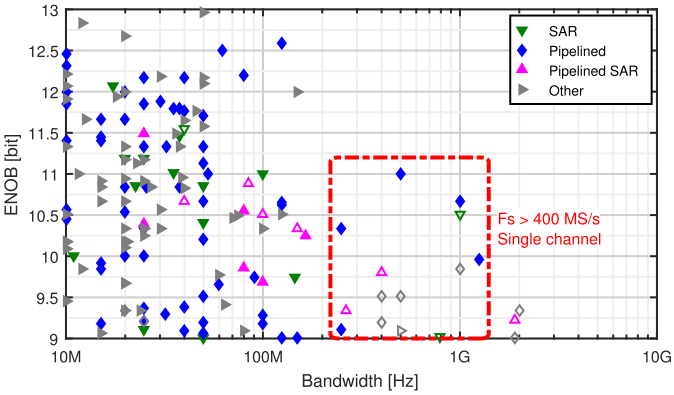

Fig. 1. Effective number of bits versus BW for ADCs with more than 9 ENOB (Nyquist input) published at ISSCC and VLSI conferences from 1997 to 2018 [11]. Unfilled symbols denote the TI systems.

As shown in Fig. 1 [11], most ADCs reported to date with greater that 9 ENOB and higher than 400 MS/s employ TI, while only a handful reaches this performance region with a single channel. The power efficiency of those fast single-channel solutions, as typically expressed by their Schreier and Walden figure-of-merit (FoM) values, is, however, not particularly high. Inspired by these observations, this paper proposes an alternative approach for pushing the per-channel performance into this region while attaining improved power efficiency.

Within the realm of high linearity and BW ADCs,[1] the fastest channel architecture tends to be some form of pipelining with a low number of bits per stage. The attainable power efficiency of such designs is usually limited by the amplifiers needed for the residue amplification at each stage. The classical and still predominant approach to residue generation is closed-loop (CL) amplification with operational transconductance amplifiers (OTAs), which are limited by their high power consumption and poor scaling properties [1], [3], [5], [8], [12]–[14]. In the high-speed designs, multistage Miller-compensated amplifiers are too slow, and highly cascoded single-stage topologies using special high-voltage

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[1] In the remainder of this paper, we denote by high-linearity, high-BW converters those achieving ≥400 MS/s and ≥9 ENOB with a Nyquist input.

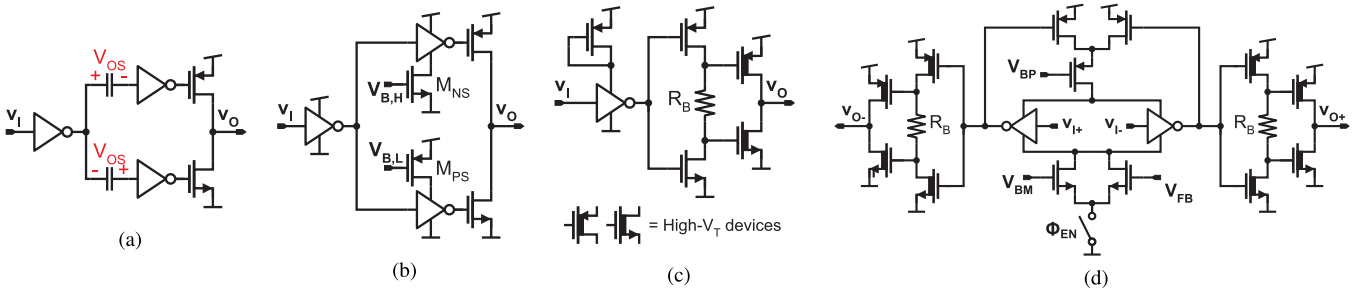


Fig. 2. Previous ringamp implementations reported in the literature. (a) Original. (b) Current-starved inverters. (c) Self-biased. (d) Differential.

supplies must be used instead [3], [8], [13]. Moreover, since the technology-limited gain–BW (GBW) of these amplifiers is often still not adequate, the problem of non-linear incomplete settling must be addressed in the digital domain through complex, high-order gain calibration.

More recently, several open-loop (OL) amplification schemes have emerged as possible alternatives within this performance region [2], [15]–[17]. These solutions have several attractive speed, noise, and efficiency advantages, but often they also require complex gain calibration and background monitoring. Furthermore, to achieve acceptable harmonic distortion levels, the input and output residues processed by the amplifier must be a small fraction of the supply. This is unfortunately not an acceptable tradeoff for pipelines with low numbers of bits/stage.

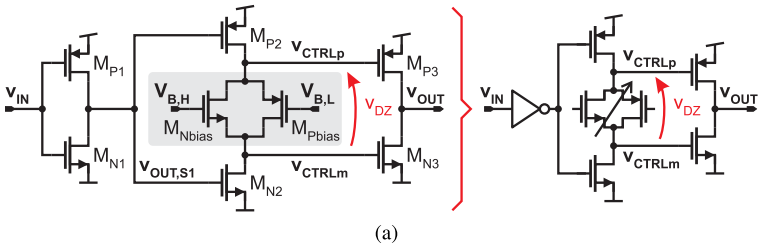
A recent approach for implementing high-efficiency scalable amplifiers is ring amplification [18]. In a nutshell, a ring amplifier (ringamp) is a multi-stage amplifier that begins charging a capacitive output load in an initially unstable (but high-slew-rate) configuration and then dynamically adjusts its biasing such that a dominant pole appears at its output, providing increasing phase margin (PM) that enforces stability through feedback mechanisms. This is achieved by introducing the so-called "dead zone" (DZ) in the input–output characteristic of the amplifier for which the output-stage devices are cutoff or in weak inversion (WI), increasing dramatically the output pole resistance and driving it toward low frequencies [18]. Ring amplification has several advantages in the context of switched-capacitor (SC) circuits, including efficient slew-based load charging, high gain and BW, almost rail-to-rail output swing, compact layout, and good scaling with technology [18]. While the merits of this technique for high accuracy have already been demonstrated [19]–[21], its application to high-speed contexts has remained unexplored. In this paper, we demonstrate a 600-MS/s, 12-bit single-channel pipelined ADC in 28 nm, which takes the advantage of the OL gain characteristics of ringamps to achieve both high linearity and BW with good power efficiency [22]. This is made possible by realizing that the overall linearity achieved in a pipelined ADC is limited by the flatness of the OL gain versus output voltage characteristic of its residue amplifiers and not just by the raw value of their maximum gain, when first-order gain calibration is used.

This paper is organized as follows. Section II reviews the foremost ringamp implementations proposed in the past. Section III discusses the speed-optimized ringamp introduced in this paper, describing its operation and main properties and how these are exploited to achieve high linearity and BW while maintaining good power efficiency. The implementation of these ideas in a prototype pipelined ADC is detailed in Section IV, and the experimental results are reported in Section V. Finally, Section VI summarizes the conclusions.

II. Review of Existing Ringamp Implementations

Since its inception, the concept of ring amplification has been embodied by implementations mainly focused toward improving linearity and robustness rather than exploring the speed limits of the technique. Fig. 2(a) shows the original ringamp introduced in [18]. In this circuit, the stabilizing mechanism was achieved by inducing offset voltages between the first two stages, programed into floating capacitors. Fig. 2(b) shows another ringamp implementation which also features a split second stage, but in which the DZ is created by using current-starved inverters [23] and can be tuned by acting on the bias voltages of the starving devices M_{NS} and M_{PS}.

The self-biased ringamp shown in Fig. 2(c) was proposed in [24]. This circuit features a consolidated second stage where the DZ is created by means of a polysilicon resistor. Upon settling, the current through the second stage induces a voltage drop in R_B which reduces the overdrive of the output-stage transistors, thus increasing their output resistance and pushing the output pole to lower frequencies to increase the PM. This self-biasing mechanism has the added advantage of naturally adjusting the DZ in a manner proportional to variations of both the supply voltage and the current flowing through it, resulting in a more inherently robust implementation. To reduce the overdrive of the output transistors and increase their resistance and gain even further, they are implemented with high threshold voltage (V_T) devices. This enhancement, however, reduces the slewing current available to charge the load and results in wider devices required to meet a given slew time duration [24]. To minimize the first-stage noise contribution while limiting its power consumption, a diode-connected pMOS is used as a power regulator to reduce the effective supply voltage seen by the inverter in this stage, allowing the use of wide, large-g_m transistors without incurring excessive quiescent current. However, this enhancement comes at the expense of overdrive reduction and has the downside of limiting the speed of the first stage, resulting in bigger devices with larger parasitics.

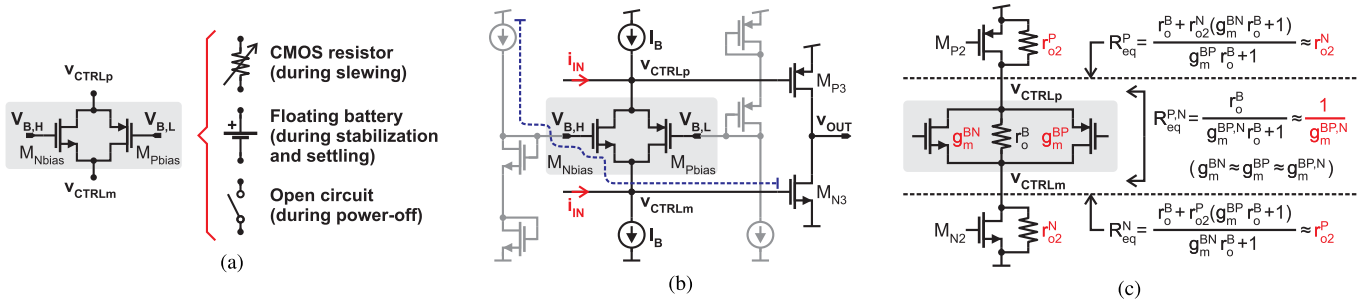


(a)

Parameter	Stage 1	Stage 2	Stage 3	Total
$W_{M_{Pi}}$, $W_{M_{Ni}}$	16 µm	8 µm	8 µm	–
$W_{M_{Pbias}}$, $W_{M_{Nbias}}$	–	1.2 µm	–	–
$L_{M_{Pi}}$, $L_{M_{Ni}}$	30 nm			–
I_{avg} @ 600 MS/s	1.5 mA	0.6 mA	100 µA	2.2 mA
Gain	16 dB	26 dB		42 dB
GBW (output settled at mid-rail, V_{DZ}=500 mV)				2.77 GHz
PM (output settled at mid-rail, V_{DZ}=500 mV)				61.4°

(b)

Fig. 3. Proposed high-speed ringamp. (a) Core schematic along with the simplified representation. (b) Relevant design parameters.



(a) (b) (c)

Fig. 4. AP-CMOS arrangement. (a) Symbolic representation of operation modes in the proposed ringamp. (b) Use in a Monticelli class-AB output stage. (c) Notable small-signal resistances in the floating-battery mode (ringamp second stage).

Thus, while constituting a power-efficient and robust solution, the use of high-V_T devices and first-stage supply reduction limits the speed achievable with this circuit.

An evolution of the self-biased ringamp is the fully differential implementation shown in Fig. 2(d) [20], where the input inverter was replaced by a switchable class-A differential stage composed of two complementary differential pairs, and high-V_T devices were introduced also for the second stage. The advantages provided by these modifications—common-mode (CM) rejection and improved gain—also come at the expense of speed. In particular, the transformation of the first stage into a class-A circuit imposes a hard limit on the slewing current of this stage. Moreover, the overdrive of the differential pair devices is reduced due to the V_{DS} voltage drops in the tail current sources and CM feedback (CMFB) transistors in series with them. Likewise, the use of high-V_T devices in the second stage for increasing the gain by minimizing their $V_{DS,sat}$ values [20] results in reduced overdrive and slewing current, yielding bigger devices with larger parasitics and therefore lower frequency non-dominant poles that limit the achievable BW. Thus, while enhancing gain and linearity, these modifications render the differential ringamp less amenable to high-speed applications. A similar structure with an additional class-A differential stage was later reported in [21] to achieve a four-stage ringamp with >90-dB OL gain, enabling a high-linearity, calibration-less pipelined-SAR ADC operating at 100 MS/s.

III. Proposed Speed-Optimized Ringamp

Fig. 3(a) shows the core schematic of the ringamp proposed in this paper. It is based on the self-biased implementation of Fig. 2(c) but to maximize the overdrives and slewing strengths, the first-stage supply regulation is not implemented and the high-V_T output devices are not used. Moreover, the biasing resistor is replaced by an anti-parallel (AP) arrangement of CMOS transistors, which provides two advantages: the capability of tuning the DZ voltage amplitude and of powering down the ringamp efficiently (the former is symbolically indicated in the simplified representation of Fig. 3(a) by the arrow between the output-stage control nodes.) The (static) DZ voltage V_{DZ} is defined, for the remainder of this paper, as the potential difference between these nodes when the second-stage gain devices M_{P2} and M_{N2} are in saturation

$$V_{DZ} \triangleq V_{CTRLp} - V_{CTRLm}\big|_{M_{P2},M_{N2}\text{ in saturation}}. \quad (1)$$

The operation and most important properties of the proposed ringamp, and how they can be exploited to achieve high linearity and BW, are discussed in Sections III-A–III-E.

A. Anti-Parallel CMOS Arrangement

At the core of the proposed ringamp lies an AP-CMOS arrangement that changes electrical behavior during various phases[2] of the ringamp transient. As depicted in Fig. 4(a), this arrangement undergoes the following three modes of operation.

1) CMOS Resistor: During the slewing phase, the second-stage devices M_{P2} and M_{N2} operate (mutually exclusively) in triode and cutoff regions, pulling v_{CTRLp} and v_{CTRLm} toward one of the supplies. Under these circumstances, the voltage difference at the nodes of the AP-CMOS arrangement becomes smaller than $V_{DS,sat}$ of M_{Pbias} and M_{Nbias}, so these devices operate in the triode region. The arrangement, thus, behaves like a CMOS resistor, whose resistance decreases as v_{CTRLp} and v_{CTRLm} are pulled toward the target supply rail.

[2]Slewing, stabilization, and settling [18].

2) Floating Battery: During the stabilization and settling phases, M_{P2} and M_{N2} operate increasingly in saturation, behaving as current sources for the AP-CMOS arrangement. Moreover, as the DZ voltage builds up, the voltage difference at the nodes of the AP-CMOS arrangement increases past $V_{\mathrm{DS,sat}}$ of M_{Pbias} and M_{Nbias}, pushing these devices into saturation. Under these circumstances, the AP-CMOS arrangement behaves like the floating battery used in the Monticelli class-AB output stage shown in Fig. 4(b) [25]–[28].

3) Open Circuit: The AP-CMOS arrangement can be easily put into a high-impedance state by pulling $V_{B,H}$ and $V_{B,L}$ to the supplies rails, which is useful for powering down the ringamp efficiently, as described in Section IV-B.

The use of the AP-CMOS arrangement makes the operation mechanisms of the proposed ringamp different from those of either a passive-resistor self-biased ringamp or a standard class-AB amplifier. From the perspective of ringamps, during the settling and stabilization phases, the proposed ringamp benefits from the properties of the floating battery: as shown in Fig. 4(c), the resistance between the nodes of the AP-CMOS arrangement is small ($\approx g_m^{-1}$ of M_{Pbias} and M_{Nbias} [27]), while the resistance looking into one node is essentially the resistance loading the opposite node [29]. Thus, the output resistance r_o^B of the AP-CMOS arrangement is "transparent" to the signal, and from the pole–zero point of view, these nodes are tightly tied together as if the arrangement was not there at all. In this sense, the use of the AP-CMOS arrangement for generating the DZ has a close-to-ideal behavior: 1) during slewing its resistance is minimized and 2) during stabilization and settling its (large-signal) behavior allows the DZ to build up while staying transparent to the (small) signal. This is in contrast to using a passive resistor, as in this case: 1) a constant resistance is presented to the second stage during slewing and 2) during stabilization and settling this resistance affects the pole frequencies of the second-stage output nodes. However, the AP-CMOS arrangement has comparatively higher capacitive parasitics than a polysilicon resistor and these reduce its speed advantage, so in practice, its main benefits with respect to a passive resistor remain the DZ tunability and the ability to multiplex multiple bias voltages for the sake of power down. From the perspective of standard class-AB amplifiers, applying the AP-CMOS arrangement to a ringamp offers instead clear advantages, including full rail-to-rail driving capability of the output-stage control nodes and increased speed due to the lack of internal dominant poles. In contrast, the class-A biasing of the floating battery in a Monticelli cell limits the maximum overdrive applicable to the output devices [28, pp. 76] [in Fig. 4(b), v_{CTRLm} cannot go above $V_{\mathrm{DD}} - V_{\mathrm{DS,sat}} - V_{\mathrm{GS},M_{\mathrm{Nbias}}}$], and Miller compensation must be used to create internal dominant poles [26], [27].

B. Transient Behavior

The magnitude of the DZ voltage plays a critical role in the determination of the ringamp transient behavior and is especially important in high-speed applications where the ringamp is made to operate on the verge of incomplete settling. From (1), it can be seen that the output-stage overdrives are directly controlled by V_{DZ} (V_{DD} is the supply voltage)

$$V_{\mathrm{SG},M_{P3}} + V_{\mathrm{GS},M_{N3}} = V_{\mathrm{DD}} - V_{\mathrm{DZ}}. \tag{2}$$

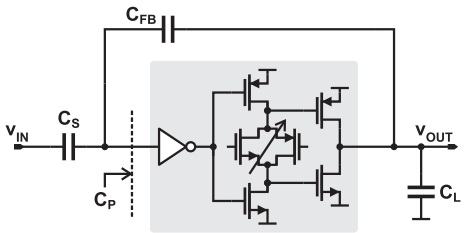


Fig. 5. Ringamp in an amplifying configuration with capacitive feedback.

While V_{DZ} also has a subtle indirect effect on the slewing phase of the output transient,[3] its largest impact occurs during the stabilization and settling phases through its modulation of the output-stage resistance and transconductance and the ensuing shifting of dominant pole and GBW frequencies. This can be explained by recalling the expression for the drain conductance of the output-stage devices using an all-region MOS model (where μ denotes the carrier mobility, C_{ox} denotes the gate capacitance per unit area, W and L denote the device width and length, V_{FB} denotes the flatband voltage, ψ_{sL} denotes the surface potential at the drain, γ denotes the body-effect parameter, and $i=\{P, N\}$) [30]

$$g_{\mathrm{ds3}}^i = \mu_i C_{\mathrm{ox}} \left(\frac{W}{L}\right)_i \left(V_{\mathrm{GS3i}} - V_{\mathrm{FB}}^i - \psi_{\mathrm{sL}}^i - \gamma^i \sqrt{\psi_{sL}^i}\right); \tag{3}$$

from (2) and (3) it can be seen that variations in V_{DZ} impact the dominant pole location ($C_{L,\mathrm{total}}$ is the total load capacitance seen by the amplifier)

$$f_{dp} = \frac{1}{2\pi} \frac{g_{\mathrm{ds3}}^P + g_{\mathrm{ds3}}^N}{C_{L,\mathrm{total}}} \propto (V_{\mathrm{DD}} - V_{\mathrm{DZ}}). \tag{4}$$

Similar considerations apply to the (OL) ringamp GBW, as

$$f_{\mathrm{GBW}} = \frac{1}{2\pi} A_{\mathrm{stage1}} A_{\mathrm{stage2}} \frac{g_{m3}^P + g_{m3}^N}{C_{L,\mathrm{total}}} \tag{5}$$

will vary in time as g_{m3}^i changes due to V_{DZ} variations. Note that when the ringamp is in feedback, $C_{L,\mathrm{total}}$ will include the loading from the feedback and input networks and from the capacitance at the ringamp input, in addition to any explicit load C_L. For instance, for the generic configuration in Fig. 5

$$C_{L,\mathrm{total}} = C_L + \frac{C_{\mathrm{FB}}(C_S + C_P)}{C_{\mathrm{FB}} + C_S + C_P} = C_L + \beta(C_S + C_P) \tag{6}$$

where the feedback factor β is given by

$$\beta = \frac{C_{\mathrm{FB}}}{C_{\mathrm{FB}} + C_S + C_P}. \tag{7}$$

To illustrate the effects of V_{DZ} in the transient behavior, the ringamp step response is simulated using the circuit in Fig. 6(a), where the response to a 400-mV step in a

[3]Since the resistance of the AP-CMOS arrangement limits how fast the control nodes v_{CTRLp} and v_{CTRLm} can be charged/discharged, it affects the delay after which the maximum slewing overdrive at the output is reached.

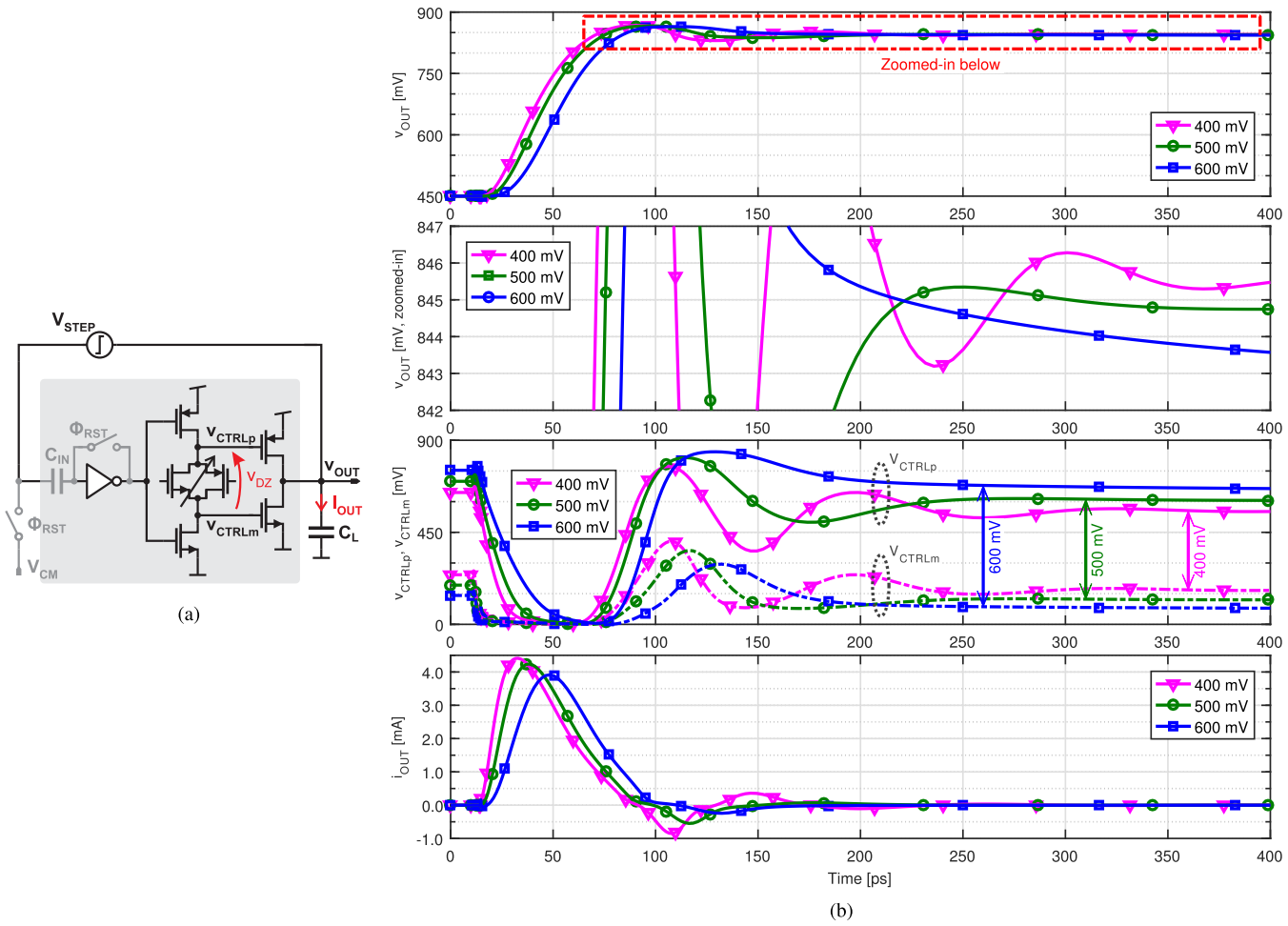


Fig. 6. Simulated step response of the proposed ringamp for various DZ voltages. (a) Circuit (400-mV step at t=10 ps and V_{DD} = 0.9 V). (b) Transient waveforms for $V_{DZ} \approx$ 400, 500, and 600 mV (first and second rows: output voltage, third row: output-stage control voltages, and fourth row: output current).

unity-gain feedback configuration[4] is analyzed for varying V_{DZ} in a 28-nm CMOS technology with V_{DD}=0.9 V. Fig. 6(b) shows the evolution of the ringamp voltages and of the current through the load.

1) For V_{DZ} = 400 mV, the overdrive of the output stage is the largest and is reached with minimum delay, causing a fast slewing of the output. However, this DZ voltage is too small to enforce settling in the given time frame, resulting in an underdamped output and incomplete settling. An effective gain of 39.1 dB can be computed for this case.
2) For V_{DZ} = 600 mV, the overdrive of the output stage is the smallest and is reached after a larger delay, resulting in the slowest slewing of the output voltage. Moreover, upon stabilization, the output presents an overdamped settling behavior, causing distortion due to incomplete settling. In this case, the effective ringamp gain is 35.5 dB.
3) For V_{DZ} = 500 mV, the overdrive is optimal and is reached with almost minimum delay: the output rises with fast slewing and settles in a critically-damped manner, providing the most complete settling among the three cases. The effective ringamp gain is 37.9 dB in this case.

To achieve maximum BW, the following sizing procedure is adopted. First, ultralow-V_T devices with minimum channel length are used for all the transistors to maximize the overdrive strength and thereby minimize the parasitic capacitances for a given g_m. Then, the widths of the output-stage devices are chosen to drive the load with enough slewing strength. Finally, the widths of the first and second stages and the AP-CMOS arrangement are chosen to push the non-dominant poles at these stages high enough in frequency to provide the sufficient PM[5] to settle within the allowed time, as in the previous example (V_{DZ} = 500 mV case). Following this procedure, the sizes and performance metrics shown in Fig. 3(b) are obtained. It can be seen that this speed-centric sizing procedure, while ensuring high BW, yields an OL gain of only 42 dB in

[4]Note that this is a worst case condition, as stability is the worst for β=1. Thus, the simulation results presented in this section and in section III-D correspond to a conservative, worst case analysis, and in a circuit with β<1, the ringamp is expected to exhibit improved settling behavior [31].

[5]A simulation-based approach was used during the design for stability validation, as PM cannot be used to ensure the large-signal ringamp stability [24], [32].

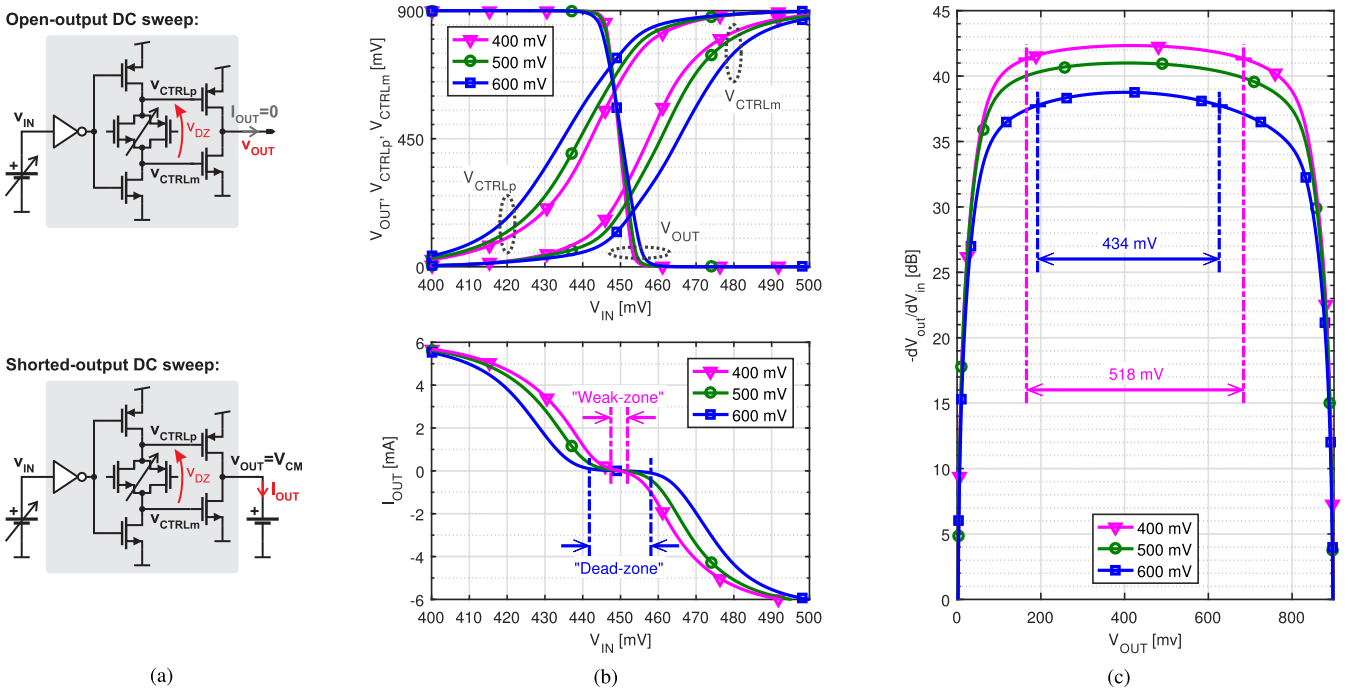


Fig. 7. Simulated dc behavior of the proposed ringamp for various DZ voltages ($V_{DD} = 0.9$ V). (a) Simulated circuits: open-output input sweep (top) and shorted-output input sweep (bottom). (b) Output and control voltages for the open-output input sweep (top) and output current for the shorted-output input sweep (bottom). (c) OL dc gain versus output voltage, calculated from the open-output input sweep, with two −1-dB compression ranges indicated.

the 28-nm technology used. As shown in the following sections, this limitation can be overcome by exploiting the OL gain flatness of the proposed ringamp and first-order gain calibration.

C. Open-Loop Gain Properties

The key property exploited in this paper to achieve high linearity is the enhanced flatness of the OL gain versus output voltage characteristic of the ringamp, which is comparatively flatter than that achievable with class-A or class-B amplifiers for on-par specifications and power consumption. This can be understood by considering the voltage bounds for the output-stage devices to stay in saturation

$$V_{\mathrm{DS,sat,M}_{N3}} \leq v_{\mathrm{OUT}} \leq V_{\mathrm{DD}} - |V_{\mathrm{DS,sat,M}_{P3}}|. \tag{8}$$

In the proposed ringamp, the output stage is biased so that during steady state, M_{P3} and M_{N3} do not shut off completely but settle into WI, thereby yielding a maximal output range due to the reduced $V_{\mathrm{DS,sat}}$ values in WI [33]. This is in contrast to class-A or class-B amplifiers, where the output devices must still remain saturated in strong inversion for output voltages close to the supply rails voltages close to the supply rails and require, therefore, larger values of $V_{\mathrm{DS,sat}}$, resulting in decreased output voltage ranges. Since the $V_{\mathrm{DS,sat}}$ voltages of the output devices during settling are defined by their overdrives, the DZ voltage also plays an important role in defining the shape of the ringamp OL gain characteristic. To illustrate this, the dc behavior of the proposed ringamp is simulated using the circuits in Fig. 7(a), where the input voltage is swept under open-output and shorted-output conditions considering the same V_{DZ} values as in Fig. 6. The evolution of the output (V_{OUT}) and output-stage control (v_{CTRLp}, v_{CTRLm}) voltages and of the output current (I_{OUT}) is shown in Fig. 7(b). From the latter, it can be seen that for large DZ voltages, a true "DZ" can be created where the output stage is cutoff and no current can be supplied to the load. However, for small DZ voltages, this "DZ" transitions into a "weak zone," where the output devices are not cutoff but remain in WI. Thus, by an appropriate choice of the DZ voltage, the ringamp can be operated either as a class-B or class-AB amplifier.[6] As discussed in Section IV, we take the advantage of this property and bias the ringamps in the main signal path as class-AB and in the CMFB path as class-B to optimize for their different linearity and speed requirements.

The OL gain versus output voltage characteristic of the ringamp is shown in Fig. 7(c) for various DZ voltages, along with the −1-dB gain compression ranges for the two extreme V_{DZ} values considered. It can be seen that the OL gain is flatter when the ringamp is biased with a "weak zone." Moreover, the gain drops for larger V_{DZ} values, a result of the gain reduction that the second stage experiences for large V_{DZ}.[7]

D. Static and Dynamic Linearities

The ringamp CL and OL gains are related according to [35]

$$A_{\mathrm{CL}} = \frac{A_{\mathrm{OL}}}{1 + \beta A_{\mathrm{OL}}} = \frac{1}{\beta}\left(\frac{1}{1 + \frac{1}{\beta A_{\mathrm{OL}}}}\right). \tag{9}$$

[6] i.e., the output-stage quiescent current can be 0 (class-B) or very small (class-AB) compared to the actual current sourced to/sunk from the load.

[7] In fact, for this stage, it holds that [Fig. 3(a)] $V_{\mathrm{DS},M_{N2}} + |V_{\mathrm{DS},M_{P2}}| = V_{\mathrm{DD}} - V_{\mathrm{DZ}}$ and thus any increase in V_{DZ} translates into $|V_{\mathrm{DS}}|$ reductions that degrade the gains of M_{N2} and M_{P2}. In the limit, a too large V_{DZ} will eventually push these devices into the triode region, reducing the gain even further.

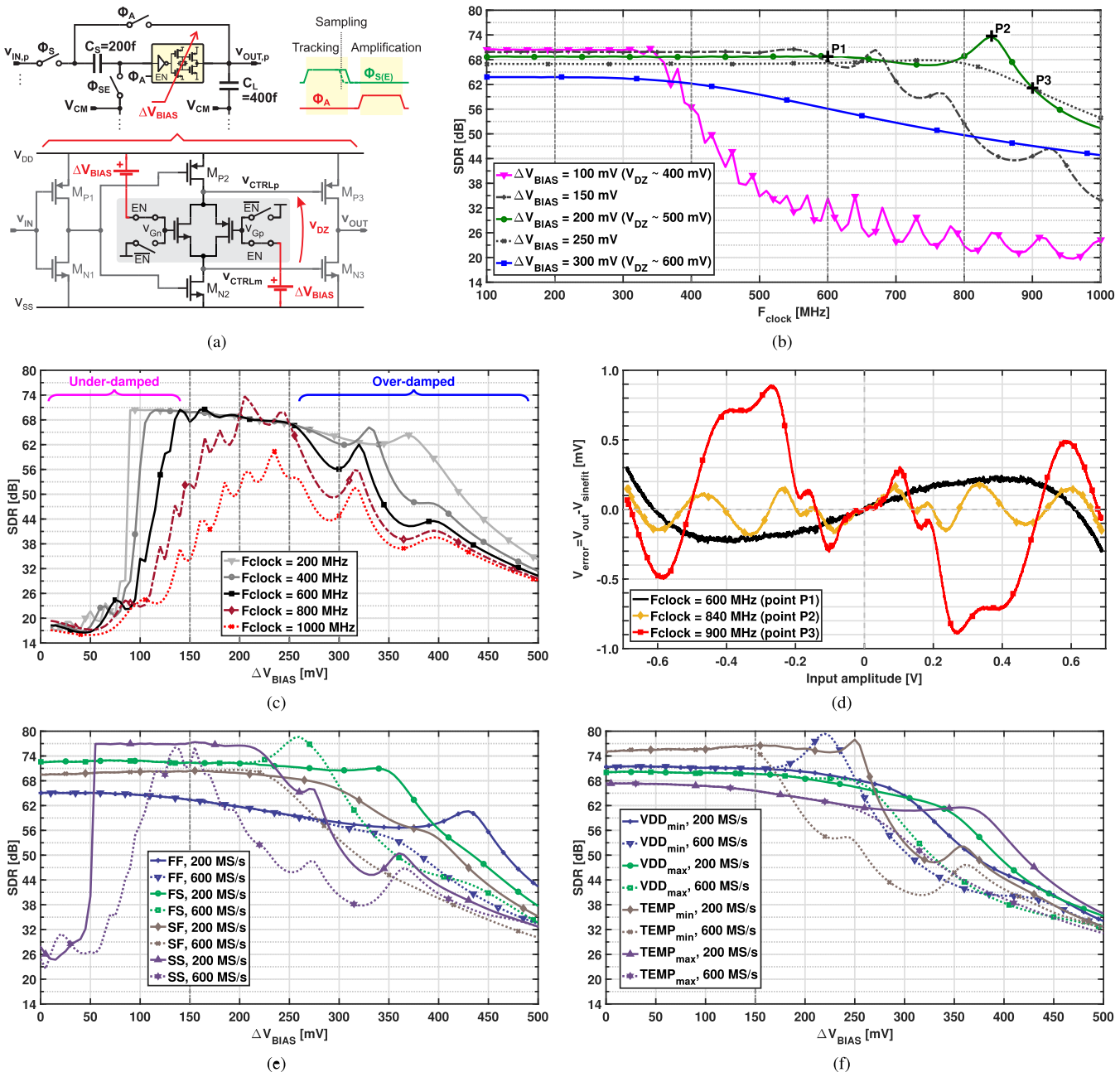


Fig. 8. Simulated performance in a unity-gain SC sample-and-hold configuration (V_{FS}=1.4 $V_{pp,d}$, Nyquist input, and V_{DD} = 0.9 V). (a) Simulated circuit (with ideal switches and capacitors). (b) SDR versus sampling frequency for various DZ control voltages. (c) SDR versus DZ control voltage for various sampling frequencies. (d) Error with respect to a sinusoidal fit on the output versus input amplitude for various sampling frequencies (ΔV_{BIAS} = 200 mV and 4096 points). (e) Results in (c) repeated at four process corners (FF, FS, SF, and SS). (f) Results in (c) repeated at four environmental corners (T = −40°C and 85°C and V_{DD}= 0.855 and 0.945 V).

From (9), it follows that in the absence of incomplete settling, the static linearity achievable in CL is dependent on the variability of A_{OL} with respect to signal and, thus, is also dependent on the ringamp biasing. To illustrate this, the proposed ringamp is simulated in the unity-gain, flip-around sample-and-hold amplifier shown in Fig. 8(a).[8] As noted in Fig. 8(a), in our implementation the DZ voltage can be varied by acting on the AP-CMOS arrangement bias voltages V_{Gn} and V_{Gp} through the parameter ΔV_{BIAS}, which quantifies the deviation of these voltages with respect to the supply rails. (The larger the ΔV_{BIAS}, the larger is the effective resistance and resulting V_{DZ}, and vice versa.)[9] The achievable linearity, measured as the signal-to-distortion ratio (SDR) at the output of this circuit, is plotted versus sampling frequency (50% duty cycle) in Fig. 8(b) for various ΔV_{BIAS} values and a 1.4-$V_{pp,d}$

[8]To capture just the intrinsic ringamp behavior, the simulations in this section and section III-E consider switches with small ON-resistance, in accordance to the actual values targeted in the design. However, larger switch resistances can be used to improve the ringamp settling behavior [32].

[9]With the sizes reported in Fig. 3(b), $V_{DZ} \approx \alpha \Delta V_{BIAS} + 300$ mV, where $\alpha \approx 1$.

full-scale input. In the lower frequency range ($F_{\text{clock}} <$ 200 MHz), the ringamp, despite its low OL gain of ∼42 dB, is able to achieve a high static CL linearity in the order of 65-70 dB. Moreover, the attained linearity is better for smaller DZ voltages, for the reasons stated in Section III-C.

As the clock frequency is increased, the effects of incomplete settling start to degrade the CL linearity, as one would expect. By extension of the discussion in Section III-B, this degradation also depends on the magnitude of the DZ voltage. These two factors allow one to characterize the behavior of the proposed ringamp in terms of biasing, linearity, and speed as follows: for small DZ values, the static CL linearity is the largest but the underdamped nature of the transient response results in a poor frequency behavior and low BW; for large DZ values, the static CL linearity is low and also the achievable BW is low due to overdamped settling; finally, a tradeoff can be achieved for DZ values in between these limits, for which both high linearity and BW can be attained. The impact of the DZ bias voltage in the achieved CL linearity is more evident in Fig. 8(c), which shows the linearity versus ΔV_{BIAS} at various sampling frequencies. In Fig. 8(c), the linearity degradation due to incomplete settling can be clearly seen, which translates in a progressive reduction of the range of ΔV_{BIAS} values for which high linearity can be attained. At 600 MS/s, a "safe" range of ≈100 mV centered around $\Delta V_{\text{BIAS}} = 200$ mV is observed where the linearity remains around 68 dB (11 bit).

The SDR peaking observed in Fig. 8(b) and (c) at high frequencies for some ΔV_{BIAS} values is an artifact of the way in which the incomplete settling affects the circuit output and distorts it from its ideal sinusoidal shape. To illustrate this, Fig. 8(d) shows the output voltage error with respect to a sinusoidal fit versus input amplitude, for various sampling frequencies and $\Delta V_{\text{BIAS}} = 200$ mV, corresponding to the points labeled P1, P2, and P3 in Fig. 8(b). Since at 600 MS/s, the ringamp is unaffected by incomplete settling (P1), it achieves the static linearity bound and the error is solely defined by the flatness of the CL gain characteristic, presenting a typical HD3-limited INL shape. At 840 MS/s, the ringamp is affected by incomplete settling (P2), but for this particular sampling frequency and ΔV_{BIAS} combination, the amplification time and the ringamp damping are such that the output is sampled close to the ideal settled value, yielding an error of reduced magnitude. At 900 MS/s, these "lucky" conditions are not met anymore (P3), and the error is higher, as expected.

To assess the robustness of the ringamp against process, supply voltage, and temperature (PVT) variations, the simulations in Fig. 8(c) were repeated at 200 and 600 MS/s considering four process corners (FF, FS, SF, and SS) and four environmental corners (T={−40, 85} °C, V_{DD}={0.855, 0.945} V, TT process corner), obtaining the results in Fig. 8(e) and (f). The ringamp maintains up to 10 bit (62 dB) of linearity at 600 MS/s for $\Delta V_{\text{BIAS}} \sim 150$ mV. While it was out of the scope of this paper to devise a PVT-robust biasing mechanism, in a practical implementation, the bias voltages of the AP-CMOS arrangement could be generated using replica-bias techniques to ensure the proper tracking of PVT variations [36].

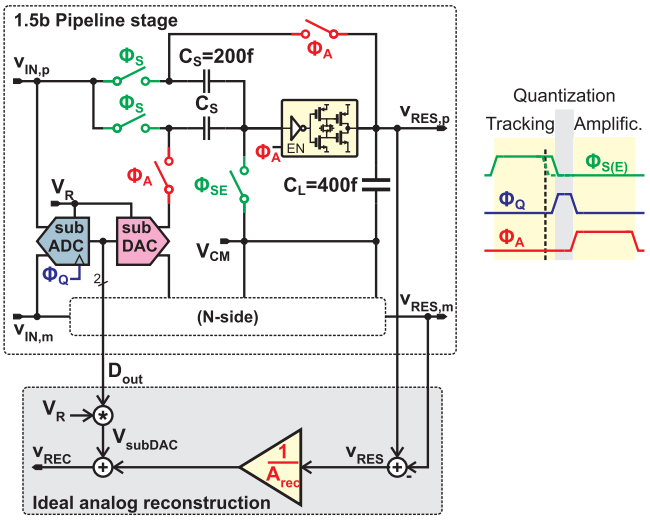


Fig. 9. Proposed ringamp in a 1.5-bit pipeline stage (flip-around MDAC [34]) with the ideal analog reconstruction.

E. Ringamp-Based, High-Linearity, and BW Pipeline Stage Using First-Order Gain Calibration

The output of a pipelined ADC is obtained by combining the digital outputs of the individual stages, which requires the precise knowledge of the CL gains of the residue amplifiers (i.e., the effective stage gains). These gain values can be obtained through several calibration techniques [37], [38]. In the case of 1.5-bit/stage pipelines, a simple first-order gain calibration can be used to compensate for all the linear errors in the stage gains, including the ones due to finite amplifier gain. As a result, high levels of linearity can be achieved even with very low-gain amplifiers, provided that their gains are sufficiently linear, which is the case of the speed-optimized ringamp presented here. To illustrate this, the 1.5-bit pipeline stage in Fig. 9 is considered, where input is reconstructed by combining the quantizer bits with the output residue by scaling the latter using a reconstruction gain A_{rec}. Fig. 10 shows the reconstructed input linearity and gain calibration details using the proposed ringamp: while using the uncalibrated nominal gain (A_{rec}=2) results in a linearity of only 45 dB (7.2bit) and an SFDR of 47 dB, after first-order gain calibration these values rise to 71.5 dB (11.6bit) and 75 dB, respectively. Moreover, the shape of the error with respect to a sinusoidal fit on the output confirms that after gain calibration, the linearity is limited by the static amplifier OL gain flatness [cf. Fig. 8(d), case P1].

In this work the hardware implementation of the first-order gain calibration was not attempted, as known solutions exist to this problem [14], [39]–[43]. However, it must be noted that in an actual implementation, the on-chip correction of the stage gains will impact the attainable power efficiency, as the alignment of the pipeline data needs to be performed at speed. Moreover, the estimation of the stage gains must run in the

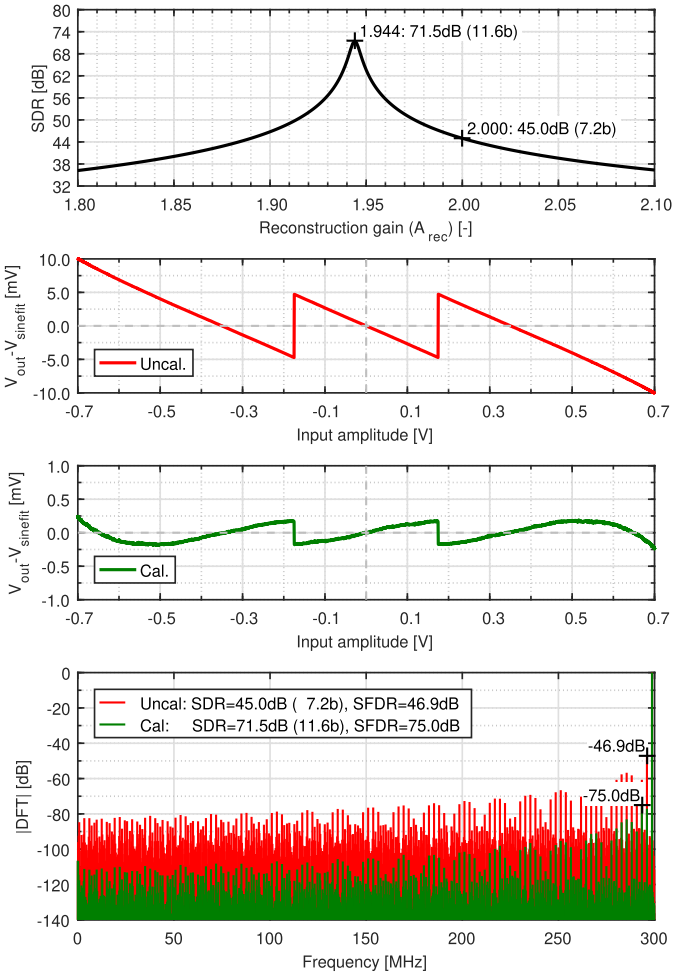


Fig. 10. Simulated performance of the pipelined stage in Fig. 9 at 600 MS/s (ΔV_{BIAS} = 200 mV, V_{FS} = 1.4 $V_{pp,d}$, near-Nyquist input, V_{DD} = 0.9 V, and 4096 points). SDR versus reconstruction gain, with uncalibrated and calibrated gain points noted (top). Errors with respect to a sinusoidal fit on the reconstructed output versus input amplitude, before and after gain calibration, respectively (middle). Spectrum of the reconstructed output before and after gain calibration (bottom).

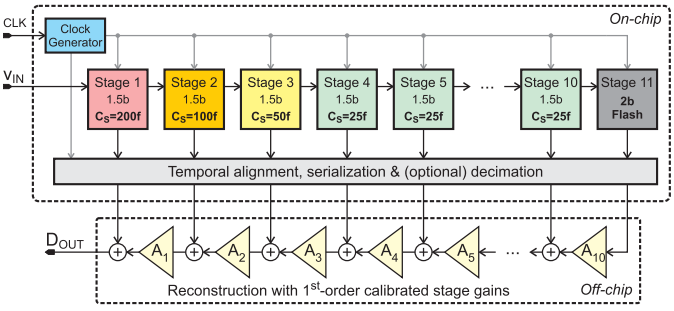


Fig. 11. ADC architecture and off-chip digital reconstruction.

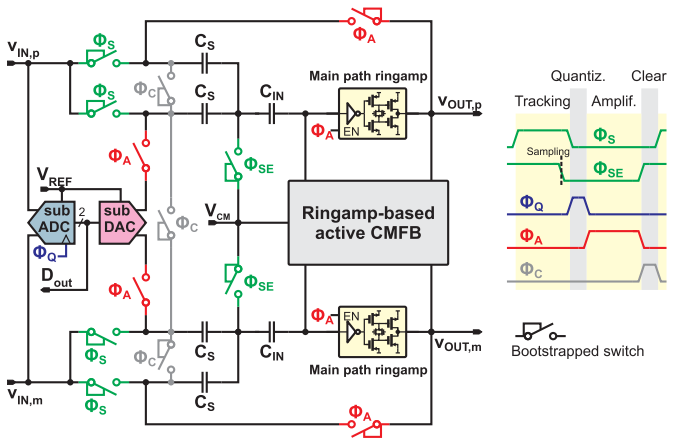


Fig. 12. Structure of each pipeline stage (stages 1–10).

background to track the PVT variations, although the associated power is much lower as it can be implemented with simple hardware and need not run at speed [40]. Also, in a practical implementation, the minimum OL gain allowed for the residue amplifiers might be dictated by other considerations, such as power-supply rejection requirements.

IV. ADC Implementation

A. Architecture

To demonstrate the performance of ringamps in high-speed discrete-time sampled circuits, a pipelined ADC was implemented, of which the architecture is shown in Fig. 11. It consists of a SHA-less pipeline plus a global clock buffer/generator and digital circuitry for the alignment, serialization, and decimation of the output bits. The pipeline is composed of ten 1.5-bit stages (to maximize speed) plus a 2-bit termination flash, setting the quantization noise floor to about 12 bit. A sampling capacitance of 200 fF is chosen for the front-end stage on the basis of kT/C noise considerations, and to minimize the power, it is progressively scaled down along with the analog circuitry by a factor of 2 up to stage 4, yielding an overall thermal noise floor of ~10 bit. The digital reconstruction and gain calibration are done off-chip.

B. Stage Structure and Main Signal Path Ringamp

The structure of each pipeline stage is shown in Fig. 12. It is a pseudodifferential implementation of the 1.5-bit flip-around MDAC, where two ringamps in the main signal path generate the differential residue at the output and an active CMFB loop controls the CM using a third ringamp, as described in Section IV-C. Due to the poor ON-resistance of CMOS pass gates in 28 nm at 0.9 V, heavy use of bootstrapped switches [44] is required. The implementation of the main signal path ringamp is detailed in Fig. 13. Besides the possibility of adjusting the ringamp biasing post-fabrication, the use of an AP-CMOS arrangement for implementing the DZ voltage confers the ringamp a dynamic slewing property which provides a slightly faster slewing and stabilization with respect to a fixed resistor, since its allows for a faster charging and discharging of the second-stage output nodes during these phases due to its effective resistance being minimum when the nodes v_{CTRLp} and v_{CTRLm} are close to the supply rails. Moreover, since the AP-CMOS arrangement can be easily put into a high-impedance state, it makes it possible to use minimum-size pull-up/down devices to disconnect the ringamp from the output during the sampling phase (when the ringamp is idle and can be powered down) without impacting speed,

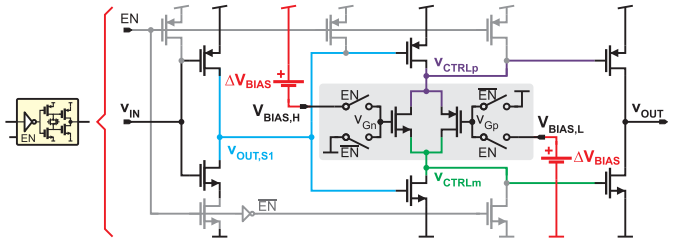


Fig. 13. Detailed implementation of the proposed ringamp.

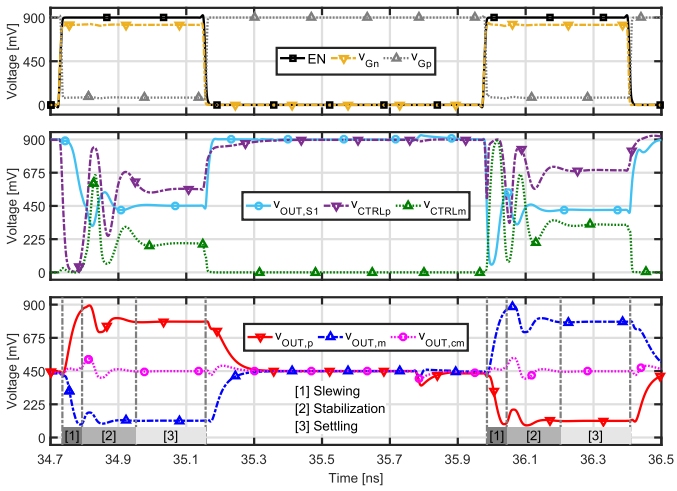


Fig. 14. Transient simulation of the proposed ringamp within an MDAC ($v_{\mathrm{OUT,cm}}$ denotes the output CM, $v_{\mathrm{OUT,cm}} \triangleq (v_{\mathrm{OUT},p}+v_{\mathrm{OUT},m})/2$).

ensuring a signal-independent OFF-state beneficial for linearity. These properties are illustrated in Fig. 14, where the simulated operation of the ringamp at 600 MS/s with a Nyquist input is shown: the ringamp completes the slewing–stabilization–settling cycle in less than 400 ps and is easily powered down in between cycles.

C. Ringamp-Based Common-Mode Feedback

Providing robust and accurate CMFB is particularly challenging for ringamp-based circuits due to the stringent BW that is required in the CM loop. This stems from the fact that during the initial slewing and early stabilization phases, the CM voltage is a poor predictor of its steady-state value (Fig. 14), and as a consequence, during these phases the CMFB loop might initially drive its output in the wrong direction, requiring even more time to reverse course and undo the mistake. While capable of wide BW, the passive capacitor-based CMFB schemes that have been proposed in the past [18]–[21], [24] are limited in their accuracy and robustness by often insufficient gain in the CMFB loop to counter the attenuation in the passive feedback network. As a result, they must contend with a tradeoff between CM accuracy, CM stability, and differential path efficiency. To tackle these issues, in this paper we introduce the active CMFB shown in Fig. 15, which uses the two-stage ringamp of Fig. 16 to generate gain in the CM path, thereby relaxing the constraints of the aforementioned tradeoff. A key point in the operation of this loop is that the CMFB ringamp is

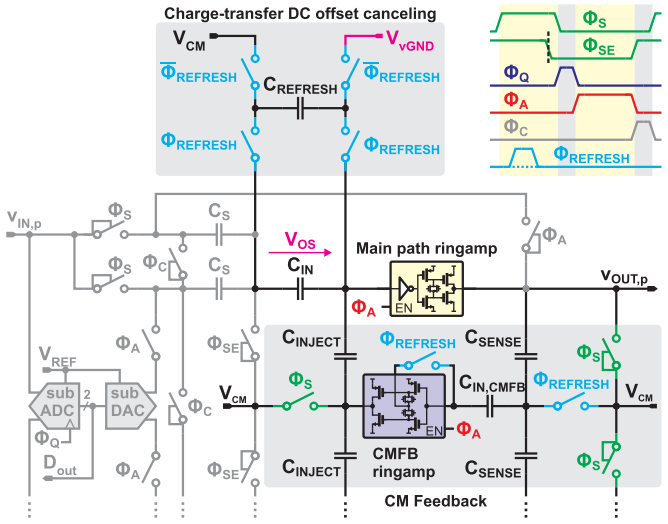


Fig. 15. Active CMFB used at each pipeline stage along with the charge-transfer-based circuit for setting the dc voltage on the offset-cancelling capacitors.

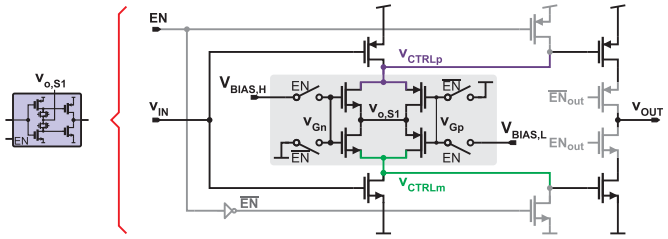
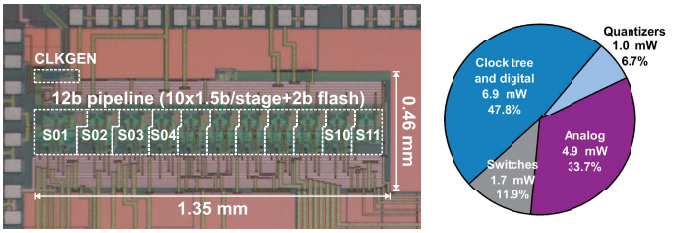


Fig. 16. Two-stage ringamp used in the CMFB of each MDAC.



(a) (b)

Fig. 17. (a) Chip microphotograph and (b) measured power breakdown by supply domain at 600 MS/s ($V_{\mathrm{DD}} = 0.9$ V).

biased to have a large non-conduction "DZ" (Section III-C) during settling to ensure the stability. This is in contrast to the ringamps in the main signal path, which are biased with a "weak zone" and remain in WI during settling, as discussed in Section III-C. In normal operation, the CMFB ringamp rapidly drives the CM level close to the target value and self-limits, rather than fully settling. This class-B behavior is still sufficient to place the output CM voltage within an acceptable error range, eliminating any larger CM errors that may be present. In this implementation, the systematic dc component of CM error is compensated in the foreground (by tuning the reference voltage V_{vGND}) and removed by programing the MDAC offset-cancelling capacitors C_{IN} using the charge transfer scheme shown in Fig. 15 [19], while the active CMFB

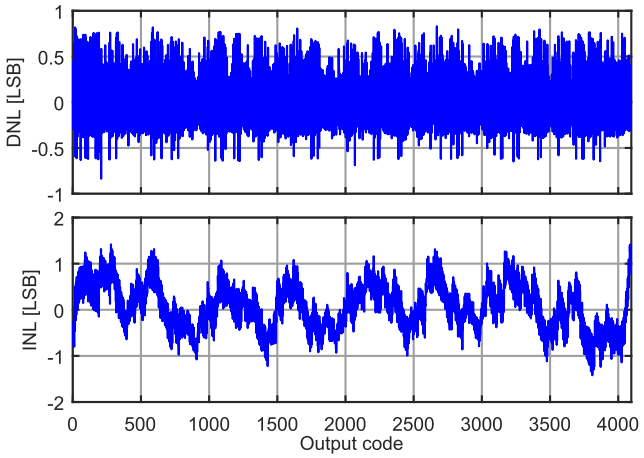


Fig. 18. Differential and integral non-linearities (code histogram method, $F_{\text{clock}} = 100$ MHz and $F_{\text{signal}} = 30$ MHz, 12-bit quantization).

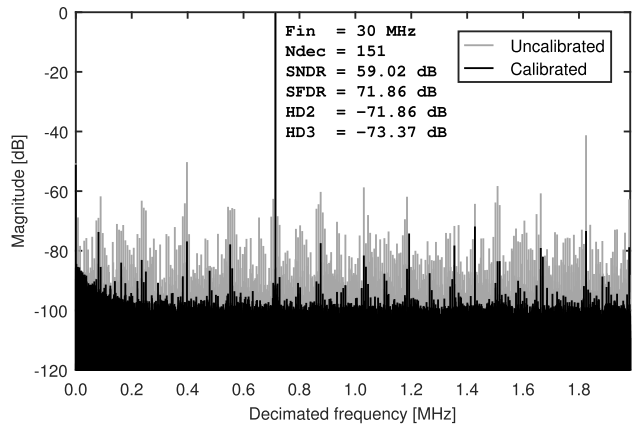


Fig. 19. Measured output spectrum for a 30-MHz full-scale input at 600 MS/s [decimation factor = 151 and 128-kpoint fast Fourier transform (FFT)].

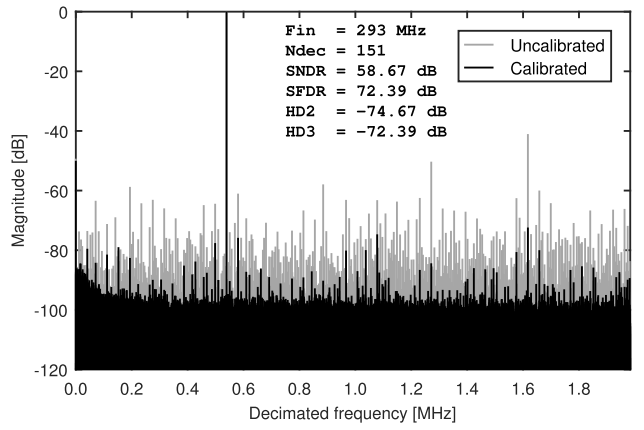


Fig. 20. Measured output spectrum for a 293-MHz full-scale input at 600 MS/s (decimation factor = 151 and 128-kpoint FFT).

is used to cancel whatever remaining dynamic CM errors are present. In a practical implementation, V_{vGND} could be set by a servo-loop to track the PVT variations.

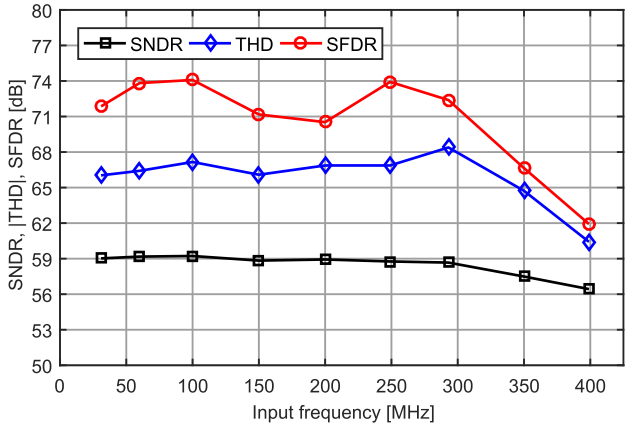


Fig. 21. Measured performance at 600 MS/s for variable input signal frequency (full-scale input amplitude and decimation factors = 151 and 32-kpoint FFTs).

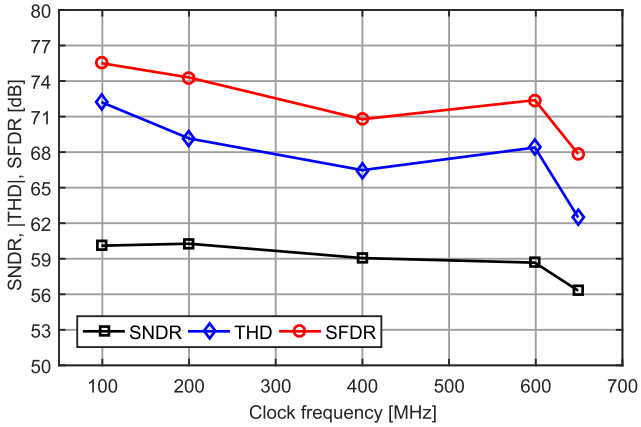


Fig. 22. Measured performance for variable clock frequency and Nyquist input (full-scale input amplitude and decimation factor = 151 and 32-kpoint FFTs).

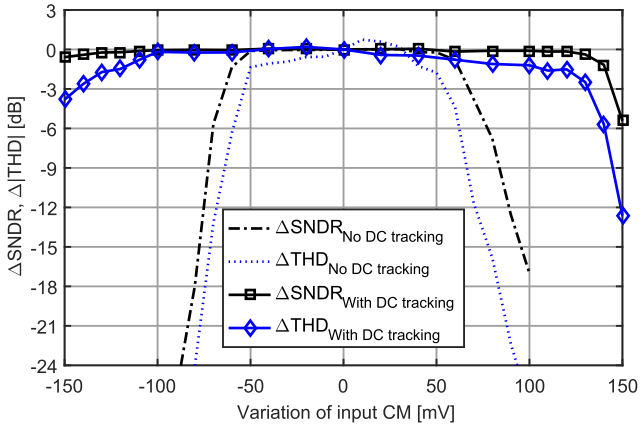


Fig. 23. Measured SNDR and THD variations versus input CM voltage static deviations ($F_{\text{clock}} = 600$ MHz, $F_{\text{signal}} = 293$ MHz, and $V_{\text{CM,in,nominal}} = 450$ mV), with a fixed offset-cancelling voltage in the first-stage MDAC (dashed lines) and an offset-cancelling voltage that tracks the CM deviation (solid lines).

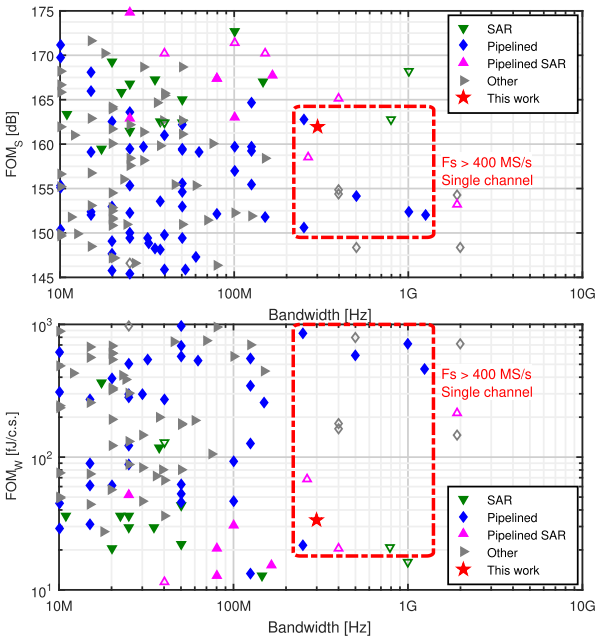
V. Measurement Results

The ADC prototype is fabricated in a 1P10M 28-nm CMOS technology. Fig. 17(a) shows a photograph of the pipeline

		This work	[17] Moon VLSI'17	[12] Shibata ISSCC'17	[5] Ali VLSI'16	[13] El-Chammas ISSCC'15	[14] Ali ISSCC'14
Architecture		**Pipelined**	Pipelined SAR	CT Pipeline	Pipelined	Pipelined	Pipelined
Residue amplifier		**Ringamp**	Gm cell	Opamp	Opamp	Opamp	Opamp
Resolution [b]		**12**	10	–	14	14	14
Technology [m]		**28n**	28n	28n	28n	180n	65n
Supplies [V]		**0.9**	1.0	1.8/±1.0	2.5/1.8/0.9	3.3/1.8	3.3/2.5/1.2
Input range [$V_{pp,d}$]		**1.6**	–	2.0	–	2.5	2.0
Sampling rate [Hz]		**600M**	500M	9G	2.5G	500M	1G
ERBW [Hz]		**400M**	–	1.125G	1.5G	700M	1G
ENOB	LF in.	**9.51**	9.1	–	10.3	10.5	11.2
[b]	Nyquist	**9.45**	9.1	10.7	10	10.3	11
SNDR	LF in.	**59.0**	56.7	–	64	64.8	69
[dB]	Nyquist	**58.7**	56.6	66	61.7	64	68
SFDR	LF in.	**71.9**	73	79	80	93	86
[dBc]	Nyquist	**72.4**	69.2	79	73	82	82
Power [W]		**14.5m**¶	6m	2330m	1150m*	550m*	1200m*
FoM_W [J/c.-step]		**34.4f**	22f	715f	463f	849f	585f
FoM_S [dB]		**161.9**	162.8	152.3	152.1	150.6	154.2
Area [mm^2]		**0.621**†	0.015†	5.1†	14.4‡	2.5†	18§
Gain calibration		**1st-order, off-chip**	1st-order, on-chip	>1st-order on-chip	1st-order, on-chip	No	1st-order, on-chip

¶ Does not include gain calibration (performed off-chip).
* Design includes a buffer for the input signal. † Core area. ‡ Full chip area.
§ Core area, including on-chip digital calibration circuitry.

(a)



(b)

Fig. 24. (a) Performance summary and comparison with state-of-the-art single-channel ADCs ($ENOB_{HF} \geq 9$ bit and $F_s \geq 400$ MS/s). (b) Schreier and Walden FoM comparison with the ADCs published at ISSCC and VLSI conferences from 1997 to 2018 ($ENOB_{HF} \geq 9$ bit) [11], unfilled symbols denote the TI implementations.

core, which occupies an area of 0.62 mm^2. All the required supplies and references are generated off-chip, so the prototype includes no supply regulators or reference buffers. The stage gains are determined off-chip through a foreground calibration, where for each stage (starting from the end of the pipeline and going backwards), the optimum reconstruction gain that maximizes SNDR is found through a 16-step binary search. The ringamp bias voltages ($V_{B,H}$ and $V_{B,L}$) and offset-cancelling reference voltages (V_{vGND}) are also manually tuned to their optimum values during this foreground calibration. The gains and voltages thus determined are then frozen and used to produce all the reported measurements.

The power breakdown of the ADC is shown in Fig. 17(b). At 600 MS/s, it consumes 14.5 mW operating entirely from a single 0.9 V supply, of which 34% (4.9 mW) are consumed by the ringamps and 48% (6.9 mW) by the clock tree and clock generation circuitry. The pseudo-static performance measured at 100 MS/s is shown in Fig. 18. The measured DNL and INL are 0.8 LSB and 1.4 LSB, respectively.

The dynamic performance and the effectiveness of first-order gain calibration can be appreciated from Figs. 19 and 20, which show the reconstructed output spectrums at the full clock rate with full-scale low-frequency (LF) and near-Nyquist inputs, respectively. With first-order gain calibration, the ADC achieves an LF-input SNDR of 59.0 dB with an SFDR of 71.9 dB and a Nyquist-input SNDR of 58.7 dB with an SFDR of 72.4 dB. The achieved SNDR is noise limited although the measured SNR is ~3 dB lower than expected from transient noise simulations. A 1.6-$V_{pp,d}$ input was used to maximize the SNDR and show the rail-to-rail operation of the ringamp.

The dynamic performance versus input signal and input clock frequencies is shown in Figs. 21 and 22, respectively. An effective resolution BW (ERBW) in excess of 400 MHz and a maximum sampling frequency of 600 MS/s are measured, the latter being limited by incomplete settling. SFDR levels above 70 dB are maintained throughout these ranges. A post-layout analysis revealed that despite a ringamp amplification window of less than 450 ps, excess delays in some aspects of the clock tree limited the design to 600 MHz. A re-optimization of the clock tree would, therefore, allow even higher speeds.

The resilience of the active CMFB against dynamic and static CM perturbations is reported in Fig. 23, where the variations in SNDR and THD are plotted versus a static deviation of the input signal CM with respect to its nominal value, considering two scenarios where: 1) the voltage programed in the offset-cancelling capacitors is kept constant (dashed traces, "no dc tracking" case) and 2) it is made to track the input CM deviation (solid traces, "with dc tracking" case). From these measurements, dynamic and static CM error correction ranges of ±50 and ±140 mV are observed.

Fig. 24(a) shows the comparison of this work with other recently published single-channel ADCs with ≥9 ENOB and ≥400 MS/s. With Walden and Schreier FoMs of 34.4 fJ/conv.-step and 161.9 dB, respectively, this work achieves state-of-the-art power efficiency, as further illustrated in Fig. 24(b).

VI. Conclusion

In this paper we demonstrated a high-efficiency, single-channel, 600-MS/s, 12-bit pipelined ADC that leverages the flatness of the ringamp OL gain versus output voltage characteristic and first-order gain calibration to simultaneously achieve high speed and BW in low-voltage

nanoscale CMOS. A speed-optimized ringamp was introduced and its operation and main exploited properties discussed and illustrated though simulations, including transient response, gain versus output voltage flatness, and static and dynamic linearities. An active CMFB circuit using a two-stage ringamp was also introduced to satisfy the need for robust, fast, and power-efficient MDAC CM regulation.

Fabricated in a standard 1P10M 28-nm CMOS process, a prototype ADC consumes 14.5 mW at 600 MS/s operating entirely from a single 0.9-V supply and achieves a Nyquist-input SNDR of 58.7 dB with an SFDR of 72.4 dB, resulting in Walden and Schreier FoMs of 34.4 fJ/conv.-step and 161.9 dB, respectively. Achieving the highest power efficiency among single-channel ADCs of at least 500 MS/s and greater than 9 ENOB reported to date, this paper proposes an effective approach toward the realization of power-efficient, multi-GS/s ADCs through TI.

ACKNOWLEDGMENT

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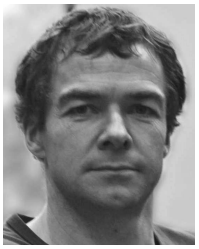

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