A 1MS/s to 1GS/s Ringamp-Based Pipelined ADC with Fully Dynamic Reference Regulation and Stochastic Scope-on-Chip Background Monitoring in 16nm

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Abstract

This paper presents an 11 bit fully dynamic pipelined ADC with an integrated reference buffer that consumes only 8% of total power. It operates from 1MS/s to 1GS/s and maintains 59.5dB SNDR and 14fJ/conv-step FoM_W across this range. Furthermore, a small circuit is introduced that provides background reconstruction of amplifier settling behavior.

Introduction

High-speed fully-dynamic event-driven ADCs provide unparalleled reconfigurability for multi-standard applications due to constant energy-per-conversion, independent of clock rate [1]. To maintain this advantage at the system level, all support circuitry, including reference buffers, must also be fully dynamic. Existing dynamic buffering solutions tend to be constrained by either ripple and noise [2] or an architecture specific implementation [3]. In this work, we present a dynamic, discrete-time reference regulation technique that is generalizable to many classes of ADC and capable of supporting arbitrarily high levels of performance.

Fully Dynamic Discrete Time Regulator

The proposed regulation technique stems from a simple but fundamental insight: ADC reference voltage accuracy and power consumption are often mutually exclusive with respect to time. When a circuit pulls a large amount of charge from a reference, it rarely requires high accuracy. And when it requires high accuracy, it usually pulls very little charge. For example, in an MDAC in this ADC, >98% of the reference charge is pulled when the amplifier is slewing and <2% is pulled when settling. The overall design requirements of a regulator can thus be dramatically relaxed by splitting the reference into "dirty" and "clean" replicas and switching from one to the other at the appropriate moment.

Fig. 1 outlines the full regulation system. For each reference voltage, a discrete time comparator monitors the reference level and provides iterative charge-packet updates through a small "charge-source" capacitor (C_P, C_M) into a larger charge reservoir (C_R) [2]. Due to the nature of charge pull in a pipeline MDAC, VREFP_dirty and VREFM_dirty always collapse toward VCM, and uni-directional regulator blocks are sufficient for those. By contrast, the "clean" and VCM replicas require bi-directional charge-sources. A clean replica is not needed for VCM due to relaxed accuracy requirements. Deterministic ripple on the clean replicas is very small (<100uV), and comparator noise dominates instead. Thus, the clean replica comparators are intentionally over-designed for low noise, with the option to decimate (only clocked once every Nth cycle) in order to optimize for power efficiency.

Fig. 2 shows how a single set of regulated replicas are fed into all stages of the pipeline and used locally by each MDAC circuit. During amplification within an MDAC, as soon as the ringamp has finished slewing the sub-DAC should switch from the dirty to clean replica. The control signal to do this can be generated with either a fixed time delay or a slew-done detector, which are both conveniently already present in this system [1]. To avoid shorting dirty/clean replicas together, the crossover must be non-overlapping. The sub-DAC selection

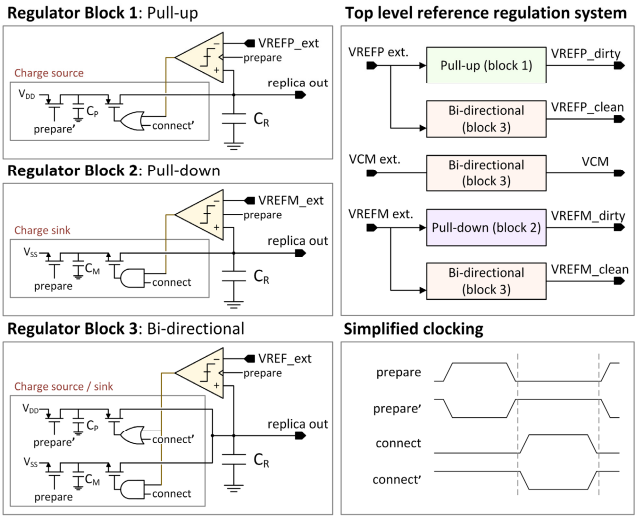


Fig. 1: Fully dynamic, discrete-time reference regulation system.

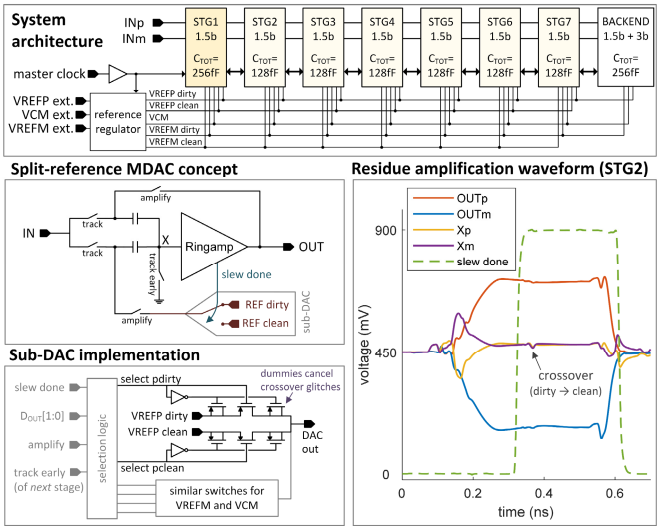


Fig. 2: Integration of regulation system into the ADC.

logic implements this with a non-overlap window of only one gate delay. Clock feedthrough glitches during crossover are cancelled by complementary dummy switches at the sub-DAC outputs. To isolate the clean replica from kickback, the sub-DAC is disconnected before the amplifier is powered down.

Ringamp and Settling Monitor

The ringamp of Fig. 3 combines the tunable CMOS-resistor and bias-enhancement of [4,5] with the fully differential structure of [6]. In addition to speed benefits, this leads to a particularly elegant self-resetting behavior. All necessary pull-up, pull-down, and power-gating functions required for reset and power-down are implicitly implemented by the core transistors, minimizing parasitics at critical internal nodes.

Attached to the ringamp's output is a small background monitor circuit (bottom of Fig. 3). Its purpose, illustrated by Fig. 4, is to reconstruct the transient settling behavior of the ringamp. The principle of operation is as follows: each cycle, two samples are taken, $V(t_{xN})$ and $V(t_{end})$. These are

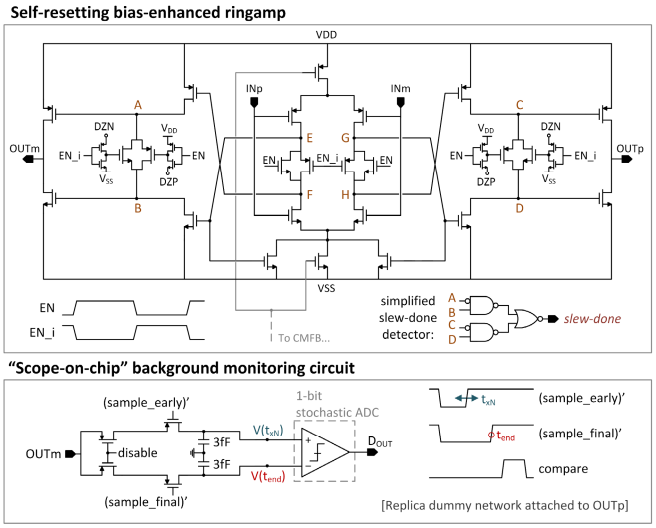


Fig. 3: Ring amplifier and attached "scope-on-chip" monitor.

compared, stripping away the settled signal value and leaving only the relative difference. Due to this self-referencing, it is possible to treat the captured data from many cycles across a wide range of amplifier output levels (e.g. 15% of backend codes) as if they were all coming from a single waveform in a single period. Thus, by sweeping t_{xN} and sorting w.r.t. backend code, an approximate settling waveform can be reconstructed for any number of ringamp output voltage levels of interest. A high-resolution reconstruction is obtained by treating the monitor circuit as a stochastic ADC [6]. Distortion is not critical in this context, so the accumulated 1-bit data is simply averaged, resulting in a low processing complexity.

Measurement Results

The ADC is fabricated in a 16nm technology, occupying an active area of 0.095mm^2 (270µm x 350µm). It operates from a single 0.9V supply with V_{REFM}=50mV and V_{REFP}=850mV. Performance for different regulator modes is compared to a "bypass" (no regulator) baseline in Fig. 5. All other reported measurements are with regulation enabled and 12x decimation (dec=12 mode). The capacitors of Fig. 1 (C_P, C_M, C_R) are made tunable for both test purposes and for scaling w.r.t. the decimation factor. The bottom half of Fig. 5 shows waveforms captured by the stochastic scope-on-chip for different ringamp biasing conditions. The backend code sorting range is set to 15% of full scale (240mV). This wide range suggests that the digital Range Detect block of Fig. 4 can also be implemented as a simple analog detector, making the technique generally applicable as a standalone circuit. It offers a lightweight, non-invasive tool for gaining unique insight into transient effects in physical systems. It may also be useful for ringamp bias optimization and PVT tracking. For example, the objective function in Fig. 5 can be generated with simple processing (but has not been tested in a closed control loop). Background operation of the monitor circuit negligibly impacts SNDR and THD and only degrades SFDR by <3dB in the worst case.

System performance is summarized in Fig. 6. At 1GS/s with a 500MHz input the ADC achieves 59.5dB SNDR and 75.9dB SFDR. The sweep of clock frequency in Fig. 6 demonstrates that the ADC, including all reference regulation, exhibits fully dynamic power consumption. This results in a near-constant energy efficiency and performance profile from 1MS/s to 1GS/s and Walden and Schreier Figures-of-Merit of 14.1fJ/conversion-step and 166.1dB respectively.

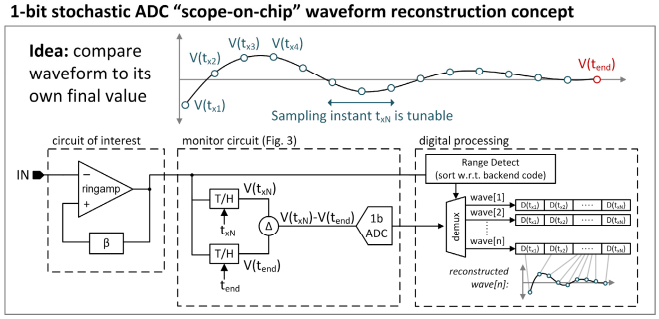
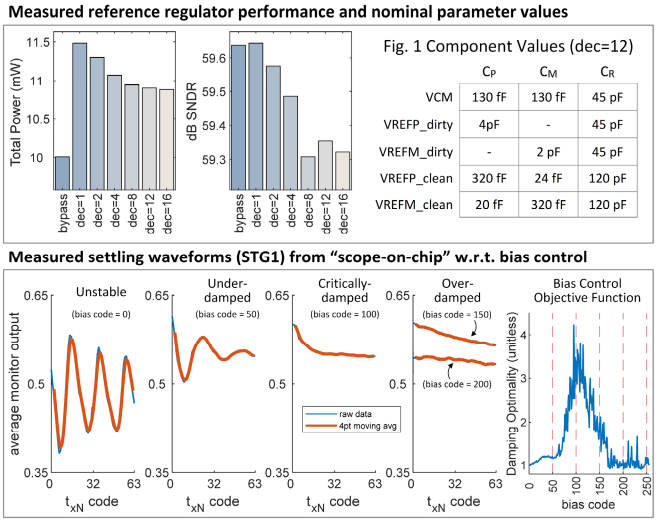
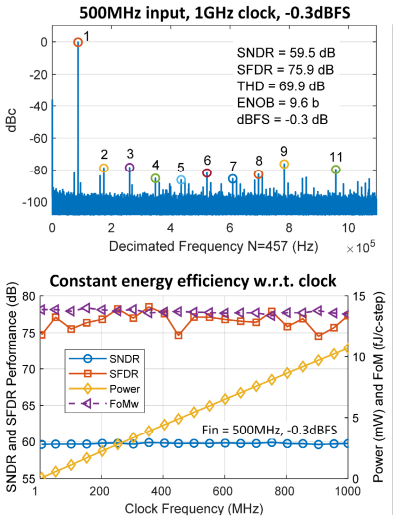


Fig. 4: Concept of amplifier settling waveform reconstruction.



	C_P	C_M	C_R
VCM	130 fF	130 fF	45 pF
VREFP_dirty	4pF	-	45 pF
VREFM_dirty	-	2 pF	45 pF
VREFP_clean	320 fF	24 fF	120 pF
VREFM_clean	20 fF	320 fF	120 pF

Fig. 5: Measured performance of regulator and ringamp monitor.



Performance Summary		
Technology	16nm CMOS	
Supply	0.9 V	
Sampling Rate	1MS/s - 1 GS/s	
Resolution	11b	
Input Range	1.6 V pk-pk diff.	
Performance at 1GS/s:	*100 MHz input:*	*500 MHz input:*
ENOB	9.7 b	9.6 b
SNDR	59.8 dB	59.5 dB
SFDR	78.6 dB	75.9 dB
THD	71.8 dB	69.9 dB
Total Power	10.9 mW	
ADC	10.0 mW (92%)	
Regulator	0.9 mW (8%)	
Walden FoM	14.1 fJ/c-step	
Schreier FoM	166.1 dB	
Active Area	0.095 mm^2	

Fig. 6: Nyquist spectrum, clock frequency sweep, and summary.

References

[1] B. Hershberg et al., ISSCC 2019 (Paper 3.6)

[2] L. Kull et al., JSSC, Dec. 2013.

[3] E. Martens, et al., JSSC, Apr. 2018.

[4] J. Lagos, et al., JSSC, Mar. 2019.

[5] Y. Chen, et al., TCASII Nov. 2018

[6] B. Hershberg et al., ISSCC 2019 (Paper 3.1)

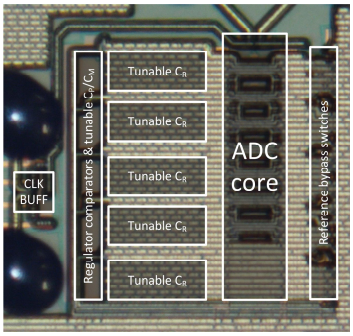


Fig. 7: Die photograph.