A 47.5MHz BW 4.7mW 67dB SNDR Ringamp Based Discrete-Time Delta Sigma ADC

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***Abstract*— This work presents a discrete-time (DT) delta sigma modulator (DSM) ADC that uses ring amplifiers to relax critical speed and efficiency bottlenecks. The DSM is designed as a 3rd-order Cascade of Integrator with Feed Forward (CIFF) with a 4-bit quantizer, and it achieves a peak SNDR of 67dB and DR of 70.0dB with 47.5MHz bandwidth when clocked at 950MHz. This is the highest bandwidth reported to-date among single-channel DT DSM ADCs and demonstrates a viable alternative to continuous-time (CT) DSM ADCs for wideband oversampling applications. With a power consumption of 4.7mW from a 1V supply, FOMS and FOMW are 167.0dB and 27.0fJ/c.s. respectively, demonstrating efficient DT delta-sigma conversion with high bandwidth.**

I. Introduction

Up until this point, the achieved bandwidth of single-channel DT DSM ADCs with competitive power efficiency has been limited to 20MHz [1]. This upper bound is mainly imposed by the high GBW requirements of the OTA-based amplifiers that are used in switched-capacitor integrators. Meanwhile, CT DSM ADCs have proven to be a compelling alternative to wideband oversampling converters but face the challenge of increased sensitivity to component values and jitter, complicated calibration schemes, and a loop filter that is not easily reconfigurable. By contrast, DT architectures are easier to design, inherently amenable to clock frequency reconfiguration, and typically more robust to PVT variations.

In this work, ringamps are explored as a solution to improve the clocking speed of DT DSM ADCs while keeping the performance and power efficiency, enabling this design to achieve performance regions previously only accessible to CT DSM ADCs. The use of ring amplifiers in deep sub-micron CMOS nodes state-of-the-art performance and efficiency has been demonstrated in single-channel gigasample pipelined ADCs [2,3]. Ring amplifiers benefit from large linear output voltage swings to achieve a high dynamic range. Efficient slewing and dynamic bandwidth settling allows achieving high clock speed. Both advantages are beneficial when implementing integrators in DSM loop filters. Their settling behavior reduces the amount of time needed to achieve the target settling accuracy for a given noise shaping resolution, while the large output swing supports a better dynamic scaling in the filter that decreases the input-referred noise. Split-source (SS) comparators [4] are used as components of the flash quantizer ladder, improving the power efficiency. We also introduce a data

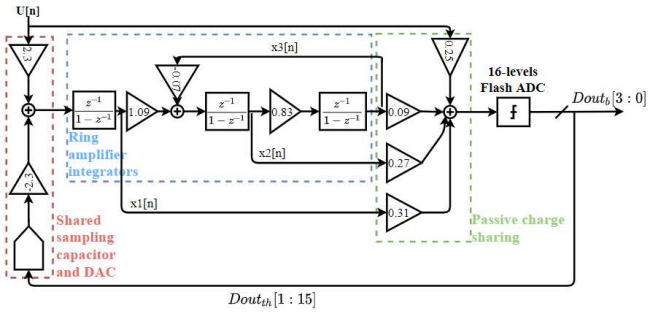

Fig. 1 System Level Implementation of the DT DSM ADC

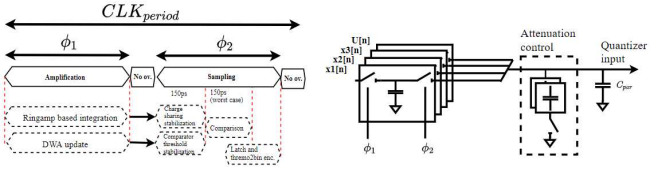

Fig. 2 Time scheduling for the DT DSM ADC (left). Charge sharing summation node (right).

weighted averaging (DWA) algorithm embedded in these comparators. The DWA is built such that the algorithm processing time is out of the feedback path, thus allowing the speed of the modulator to take full advantage of the speed of the ringamps. Due to both techniques, the ADC could reach clock speeds up to 950MHz resulting in a 47.5MHz bandwidth. Section II will show an overview of the chosen architecture to implement the ADC, including the circuit level implementation of the ringamps and the quantizer. Section III consolidates the measurement results, placing this work in perspective with the state-of-the-art DT and CT DSM ADCs. Finally, Section IV concludes this work with directions to future steps.

II. Architecture

A. System-level overview

Fig. 1 shows an overview of the ADC. All integrators are ringamp-based. The CIFF topology is chosen to exploit the large output voltage swing capability of the ringamps. That enables a dynamic-range scaling of the coefficients which increases the integrator gain and improves the rejection of non-idealities and noise from the interstage nodes when referred to the input. The architecture was modeled using a Python version of Schreier's DSM toolbox where non-idealities such as finite DC gain, settling problem for the

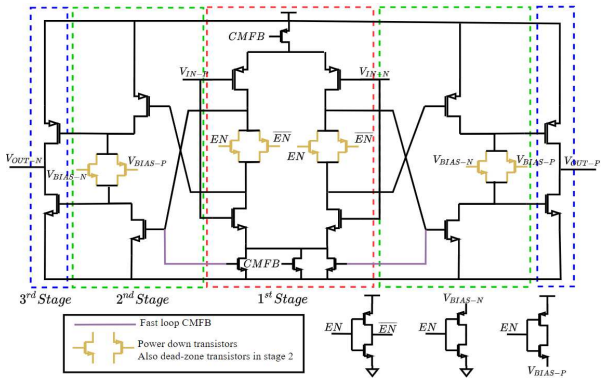

Fig. 3 Circuit level implementation of the ringamp

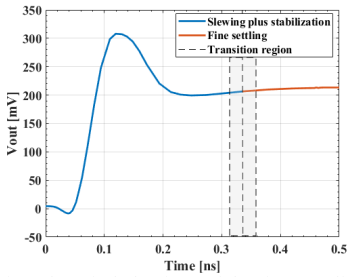

Fig. 4 Time domain behaviour of the ring amplification

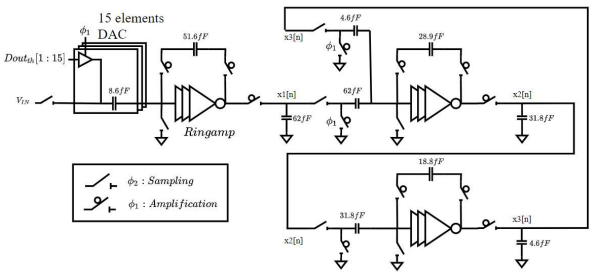

Fig. 5 Single-ended model of the ringamp-based DSM architecture

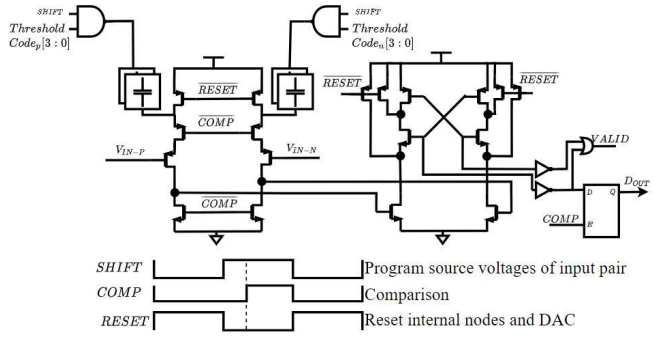

Fig. 6 Comparator circuit implementation with programmable thresholds

ringamps and mismatches were added to a 1st order degree. Aiming for a low OSR of 10, a good compromise was found in the use of a 3rd order loop filter together with a 4-bit quantizer to achieve the peak SNDR of 70dB already accounting for the modeled degradations.

The input DAC comprises 15-unit elements sized for thermal noise requirements. The comparator output thermometer code directly feeds the DAC input. The summation node is implemented using a passive charge sharing between the top plates of the sampling capacitors to save power (Fig. 2), and an extra attenuation capacitor can be added to that node to match the summation gain to the quantizer gain. Due to this scheme, the input signal fed to the summation node must be sampled one half clock phase later than the input sampled on the first integrator. Simulations show no SNDR degradation within the bandwidth from this phase difference.

The time scheduling to perform all the signal processing within the ADC is shown in Fig. 2. Two non-overlapping phases are generated from a master clock which defines the amplification and sampling phases. The sampling phase is used both for the input signal sampling and quantization, while the amplification covers the ringamps amplification time and the comparator threshold codes update.

B. Ringamp-based integrators

The ringamps used in this design use the differential implementation (see Fig. 3) similar to [3]. They have a differential input stage with a CMOS resistor implementing the dead-zone voltage in the second stage. Controlling the dead-zone voltage allows achieving better noise shaping by setting the settling performance to an optimal value. This ringamp improves its power efficiency by having a power down capability when the intermediate nodes are put in a high impedance mode, cutting down the static current to almost zero. Another advantage is with regards to the local feedback between the second stage input and the first stage current source, enabling a fast path for common-mode feedback. At the same time, an external capacitive division between the outputs gives rise to another CMFB signal which is also fed to the ringamp 1st stage.

Fig. 4 illustrates in detail the settling behavior of the ringamp-based integrator in two regions: (1) slewing plus stabilization and (2) fine settling. The first part provides fast coarse charging that brings the output of the integrator close to the desired voltage level. The second region is made of a slower but more stable settling to the target voltage level with the output transistor biased in weak inversion. Simulations show that a properly biased ringamp in 28nm can achieve 1% settling accuracy in 0.4ns, while 1st order settling OTAs would require a GBW of 9GHz for the same accuracy at the same allocated time. A single-ended version of the ringamp-based loop filter is shown in Fig. 5, it was implemented such that all amplification phases of the 3 stages happen simultaneously, and the passive summation can be done in the following phase. The alignment of the phases calls for extra capacitors at the integrator's input to decouple from the amplification of the previous stage. The incurred attenuation of this integrator output resampling is accounted for in the design of the integrators' coefficients. During the sampling phase, all ringamps are powered down to save power.

C. Quantizer with embedded DEM

The 4-bit quantizer is a flash ADC using the SS comparator structure of [4] shown in Fig. 6 together with the internal signal timings. Each comparator has a digitally programmable decision threshold set by small capacitive

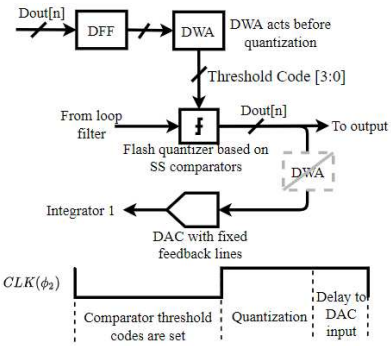

Fig. 7 Implementation of the DEM allowing lowest delay from comparators output to the DAC elements

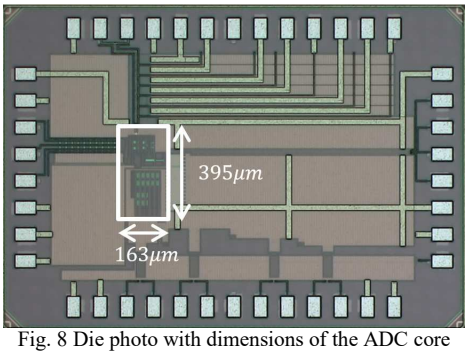

Fig. 8 Die photo with dimensions of the ADC core

DACs in the sources of the input pair transistors. During reset, their top plates are pre-charged to V_{DD} and when SHIFT gets high, the DAC is switched to generate a voltage difference in the sources that sets the threshold. This results in a very large tuning range that can be updated every clock cycle. Some delay is inserted after switching the DACs and before the comparison starts to account for the settling of the source voltages. Extra capacitors in the source DACs allow to easily compensate offset of the comparator.

The threshold programmability is also exploited to enhance the overall system speed by removing the DWA operation from the critical timing path. As shown in Fig. 7, the DWA of the feedback DAC elements is implemented indirectly by shuffling thresholds of the flash comparators rather than more directly at the input of the DAC. This eliminates the delay penalty of the DWA.

III. Measurement Results

The ADC is fabricated in a 1P9M 28nm CMOS process with a core area of only 0.064mm^2 as shown in Fig. 8. When clocked at 950MHz (47.5MHz of decimated bandwidth) it consumes 4.7mW. Fig. 9 shows a sample FFT from the output signal. In Fig. 10 the input power is swept with an insert showing the region near the MSA (Maximum Stable Amplitude). The biggest source of power consumption in this design is the quantizer (50%) due to its flash architecture, while the amplifiers are responsible for only 25% of the total power. The converter achieves a peak SNDR of 67dB (ENOB of 10.8b) and Dynamic Range (DR) of 70dB. Measurements show that the input DAC matching was good enough to run the ADC with the DWA algorithm turned off, saving power, and achieving the described peak performance.

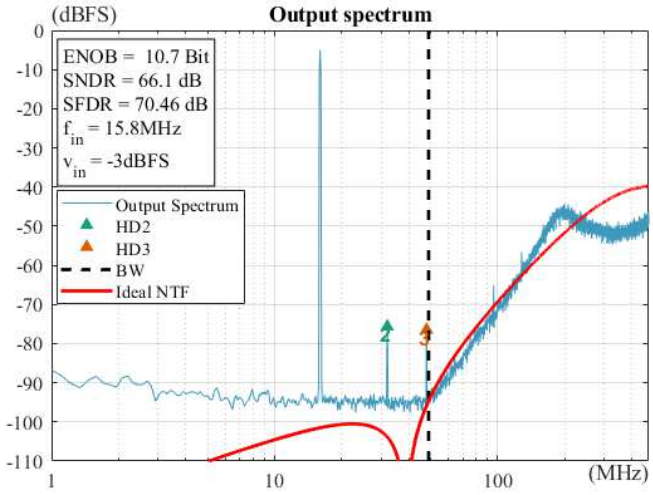

Fig. 9 8k-points FFT spectrum for a clock at 950MHz, an input frequency equal to 15.8MHz, and an input power of -3dBFS

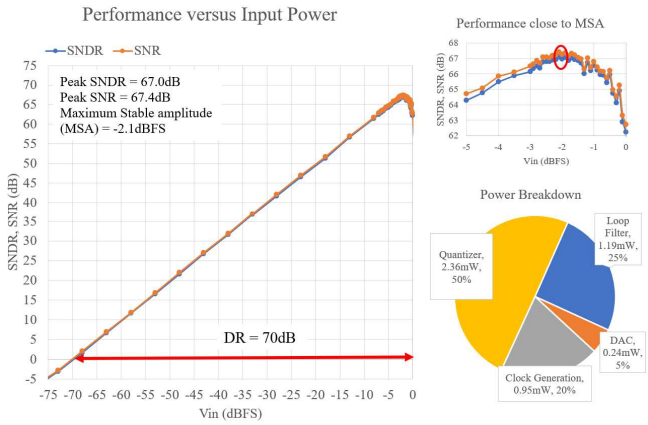

Fig. 10 Input power sweep for an input clock of 950MHz and an input frequency equal to 41.6MHz

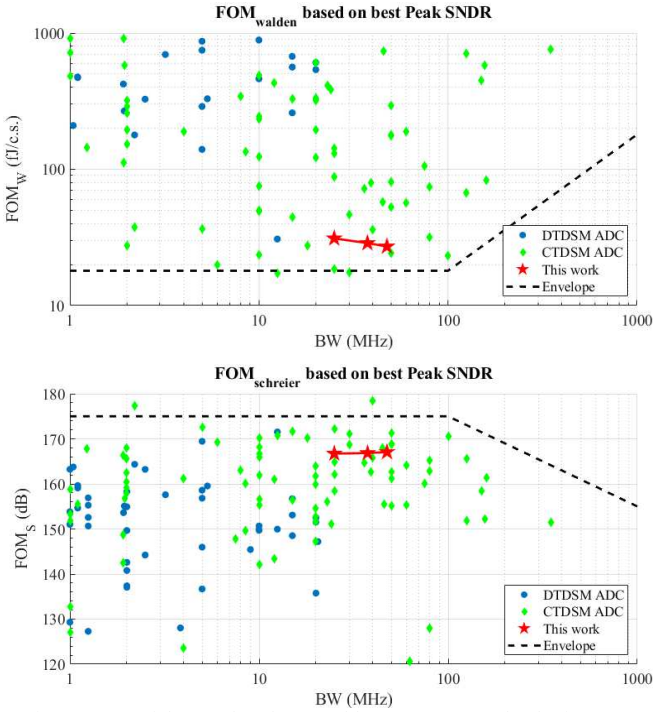

Fig. 11 State of the art plots from Walden FoM (top) and Schreier FoM (bottom)

TABLE I. COMPARISON WITH STATE OF THE ART DSM ADCS TARGETING SIMILAR BANDWIDTHS

	This work	Y. Song [5] VLSI18	S. Wu [6] JSSC13	C. Lee [7] VLSI13	B. Carlton [8] VLSI11	T. He [9] ISSCC18	C. Wang [10] ISSCC19	W. Wang [11] ISSCC19	P. Cenci [12] VLSI19
Architecture	DT	DT	DT	DT	DT	CT	CT	CT	CT
Node	28nm	65nm	65nm	22nm	32nm	28nm	28nm	28nm	28nm
Power (mW)	**4.7**	**4.5**	**94**	**12.7**	**28**	**64.3**	**7.3**	**16.3**	**3.2**
Clock (MHz)	950	200	1100	240	400	2000	960	2000	2400
OSR	10	8	32	8	10	20	6	10	30
BW (MHz)	**47.5**	**12.5**	**16.6**	**15**	**20**	**50**	**80**	**100**	**40**
SNDR (dB)	67	77.1	74.3	66	63	79.8	64.9	72.6	77.5
DR (dB)	70	78.5	81	-	66	82.8	68	76.3	78.2
FoM_S SNDR (dB)	167.0	171	156	156	151	168.7	165.3	170.5	178.5
FoM_S DR (dB)	170.0	172	163	-	154	171.7	168.4	174.2	179.2
FoM_W (fJ/c.s.)	**27.0**	**31**	**667**	**259**	**606**	**80.5**	**31.9**	**23.4**	**6.5**

FoM_S = (SNDR or DR) – $10*\log_{10}$(Power/BW); FoM_W = Power/((2*BW)*2^(ENOB))

This performance leads to a Walden FoM of 27.0fJ/c.s.; and an SNDR-based Schreier FoM of 167.0dB and DR-based FoM of 170.0dB. This ADC has a bandwidth at least 2x higher than other single-channel DT DSM ADCs [5-8] and power efficiency on par with CT DSM ADC aiming the same application bandwidth [9-12]. Fig. 11 plots the FoM Schreier and Walden of the state-of-the-art DSM ADCs together with this work operating at clock frequencies of 500MHz, 750MHz, and 950MHz, showing the performance is maintained at different clocks. Table I summarizes the most important performance metric of the DSM ADC.

IV. CONCLUSIONS

This work has proved how ringamps are suitable candidates to increase DT DSM ADC bandwidth while keeping the power efficiency on par with state-of-the-art CT DSM ADCs targeting similar application bandwidths. That was enabled by the fast and efficient amplification of the ringamps when compared to traditional OTAs, which pushed the clocking speed closer to the GHz range.

While the single-channel structure presented here reached performance regions only achievable by the CT counterparts, the DT implementation allows further improvement around the ringamp based integrators, e.g., via MASH or event time-interleaved structures.

ACKNOWLEDGMENT

The authors would like to acknowledge the help of L. Pauwels, H. Suys, and A. Dewilde for support with tests and measurements; D. Dermit for the support with measurement scripts and laboratory setup.

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