A 10.0 ENOB, 6.2 fJ/conv.-step, 500 MS/s Ringamp-Based Pipelined-SAR ADC with Background Calibration and Dynamic Reference Regulation in 16nm CMOS

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Abstract

We present a single-channel fully-dynamic pipelined SAR ADC that leverages a novel quantizer and narrowband dither injection to achieve fast and comprehensive background calibration of DAC mismatch, interstage gain, and ring amplifier (ringamp) bias optimality. The ADC also includes an on-chip wide-range, fully-dynamic reference regulation system. Consuming 3.3 mW at 500 MS/s, it achieves 10.0 ENOB and 75.5 dB SFDR, yielding a Walden FoM of 6.2 fJ/c.s.

Introduction

Pipelined SAR ADCs reported in recent years that utilize a ringamp for residue amplification have helped to advance the state-of-the-art in power efficiency [1-3]. However, all of these implementations employ a calibration-free approach where PVT robustness is ensured through extra design margin, at the cost of speed. In this work we demonstrate with the architecture of Fig. 1 how ring amplification can be exploited to simultaneously achieve high bandwidth and power efficiency, by utilizing background calibration to ensure robustness and optimize performance.

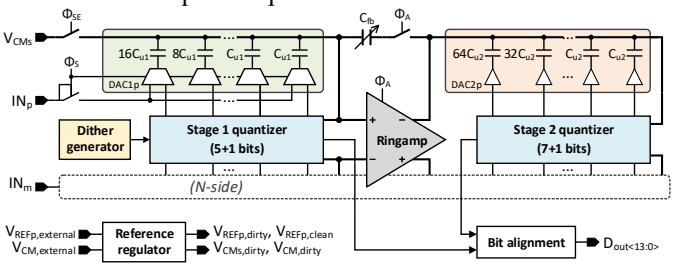


Fig. 1: ADC architecture.

SAR Quantizer with Dither Injection Capability

At the core of this work lies the quantizer shown in Fig. 2a. It is composed of a single preamplifier followed by "M" latches. Each separate latch is directly hardwired to a unique bit of the M-bit DAC. This lies topologically half-way between the traditional *single-comparator* [4] and *loop-unrolled* SAR paradigms [5]. It retains the benefits of the single-comparator topology in terms of reduced calibration complexity because the single shared preamplifier dominates the input-referred comparator offset due to random mismatch. It also inherits the benefits of the loop-unrolled topology by eliminating the 1-bit-comparator-to-M-bit-control-register demux from the critical path. Instead, the latches themselves serve as the data capture register and directly drive the DAC. Moreover, it avoids the critical drawbacks of offset calibration complexity and large input capacitance found in the loop-unrolled scheme.

Fig. 2b details the implementation of the proposed quantizer. It is based on a conventional 2-stage dynamic comparator [6] where the 2nd stage (i.e. latch) has been modified and replicated to support both the core monotonic-switching-based binary search and the injection of dither. The former is achieved with event-driven control logic, and the latter with programmable source-degeneration devices placed at the latch tail nodes that introduce intentional imbalances and can be set on a per-bit basis. This enables variable-amplitude, per-bit dither injection.

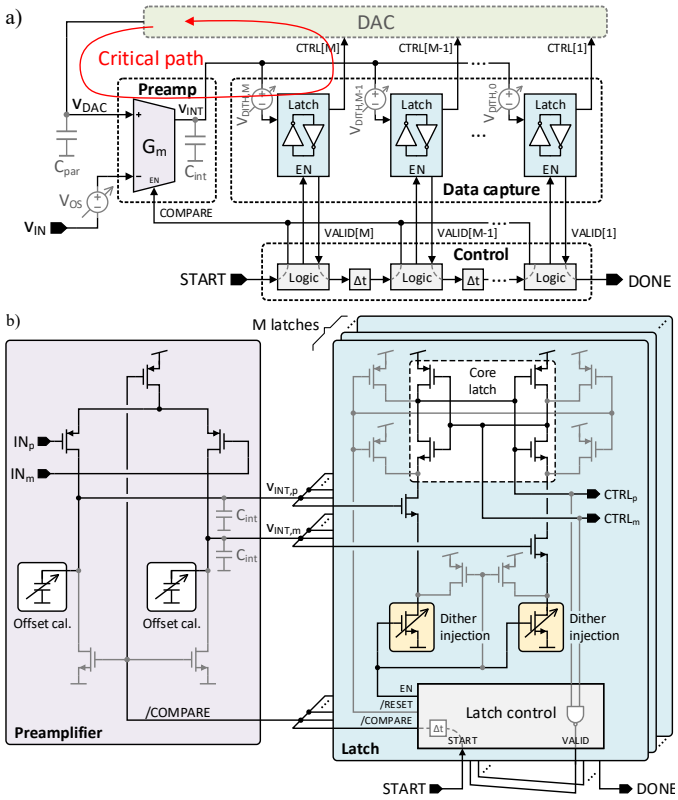


Fig. 2: (a) Proposed quantizer and (b) its implementation.

Narrowband-dither-based Background Calibration

In this work, both interstage gain and Stage-1 DAC mismatch are background-calibrated with a *band-limited* dither that improves convergence speed by orders of magnitude w.r.t. traditional *wideband* dither techniques [7]. The scheme is illustrated in Fig. 3a. The dithering of the individual quantizer thresholds injects a small Stage-1 residue error. If the resulting error falls within the interstage redundancy range, these perturbations are cancelled in the digital domain when the reconstruction weights are accurate (i.e., $w_{Ai}=w_{Di}$, $G_A=G_D$). If they are wrong, the ADC output will carry non-zero energy *correlated* to the injected dither, which can then be measured and minimized in the background by adjusting the digital weights (w_{Di}, G_D). To maximize sensitivity, dither is injected and extracted using narrow-band FIR filters (Fig. 3b) set to a frequency where spectral energy (signal power) is minimum.

Ringamp bias optimization [8] can also be performed in the background by exploiting the proposed quantizer. To this purpose, 3-level dither (-1/0/+1) is injected and the total power of *nonlinear components* of the output residue is measured and used to tune biasing. The method, illustrated in Fig. 3c, is based on an analysis of the backend histograms that result for each applied dither value. With linear amplification, injecting dither only modifies the histogram with predictable signal folding and alignment effects. Nonlinear amplification reshapes the histogram further: distortion is *larger* close to the extremes of the residue range, excited more often for +1/-1 dither, and is *less severe* for 0 dither, which excites mostly the linear region.

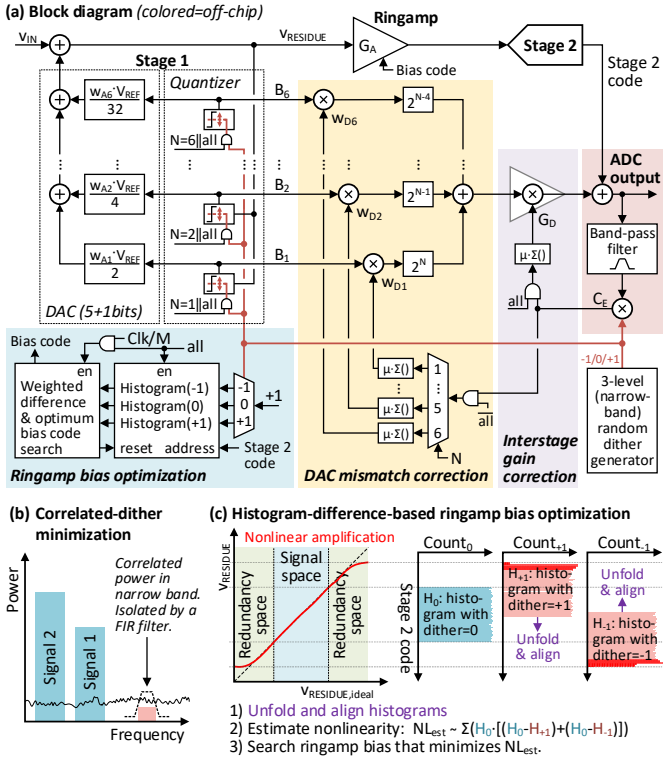


Fig. 3: Narrowband-dither-based background calibration.

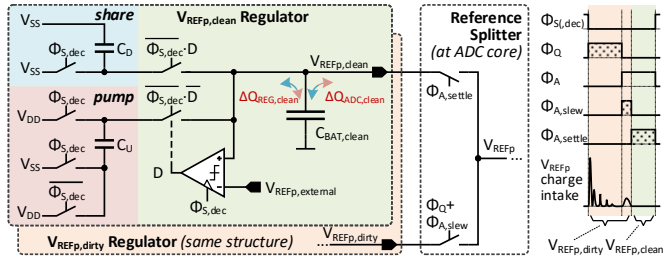


Fig. 4: Charge-pump-based dynamic reference regulation.

Practical implementation involves obtaining backend-code histograms for each dither level, aligning them taking folding effects into account, and computing a weighted difference to generate an estimate of ringamp nonlinearity that can be used to tune the ringamp bias DAC to an S(N)DR maximum.

Fully-dynamic Reference Regulation

The ADC includes an improved split-reference regulation scheme building on [9]. It is adapted for a pipeline-SAR architecture and buffers a reference V_{REFp} with *clean* and *dirty* replicas. As shown in Fig. 4, an analog mux connects the SAR DAC node V_{REFp} first to $V_{REFp,dirty}$ (at Φ_Q+$\Phi_{A,slew}$) and then to $V_{REFp,clean}$ (at $\Phi_{A,settle}$). The charge of the attached reservoirs $C_{BAT,i}$ is *dynamically* replenished and exploits the contrasting charge-pull and precision requirements of the two replicas [9]. To pull a replica *down*, charge from $C_{BAT,i}$ is *shared* with C_D. However, to pull a replica *up,* a charge *pump* is used instead. This allows for V_{REFp} values up to and even beyond V_{DD}, which was not possible in the previous implementation [9]. Moreover, V_{SS} is exploited as the negative reference, reducing the overall regulator area and power (~3.5x w.r.t. [9]). To compensate potential systematic common-mode (CM) offsets incurred when $V_{REFp} \neq V_{DD}$, independent regulation of both V_{CM} and the *sampling* CM reference V_{CMs} is implemented. Since well-balanced differential structures are resilient to CM noise, V_{CM} and V_{CMs} only require one *dirty* replica each, with very relaxed requirements (small C_{BAT} sizes, down-sampled refresh rates).

Measurement Results

The ADC is fabricated in a 16nm CMOS technology (Fig. 6) and operates entirely from a 0.9-V supply. All data reconstruction and processing for background calibration is performed off-chip and fed back through a serial interface.

Interstage gain calibration measurements are summarized in Fig. 5a. The proposed algorithm converges >100x faster than a wideband dither approach, correcting an initial 5% gain error in ~300k cycles and tracking supply-induced gain variations. Fig. 5b shows the estimated nonlinearity objective function and measured SNDR vs. ringamp bias DAC code, including supply variations. This illustrates the ability to continuously optimize the ringamp biasing in the background w.r.t. PVT variation.

Fig. 6 summarizes the measured ADC performance. At 500 MS/s, it achieves 62.3 dB SNDR and 75.5 dB SFDR with a total power consumption of 3.3 mW, of which 2.8 mW are consumed by the core and 0.5 mW by the reference regulator. With FoM_W and FoM_S values of 6.2 fJ/c.-s. and 171.1 dB, respectively, this work achieves the highest power efficiency reported to date among all single-channel ADCs of any architecture operating above 200 MS/s.

References

[1] Y. Lim, VLSI'17. [2] ElShater, ISSCC'19. [3] T-C. Hung, ISSCC'20. [4] Y-Z. Lin, VLSI'16. [5] Verbruggen, ISSCC'12. [6] Miyahara, ASSCC'08. [7] J. Li, TCAS-II, Sept. 2003. [8] Hershberg, ISSCC'19. [9] Hershberg, VLSI'20.

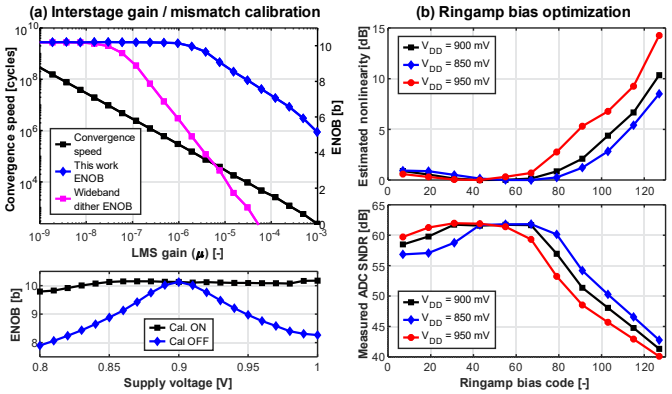
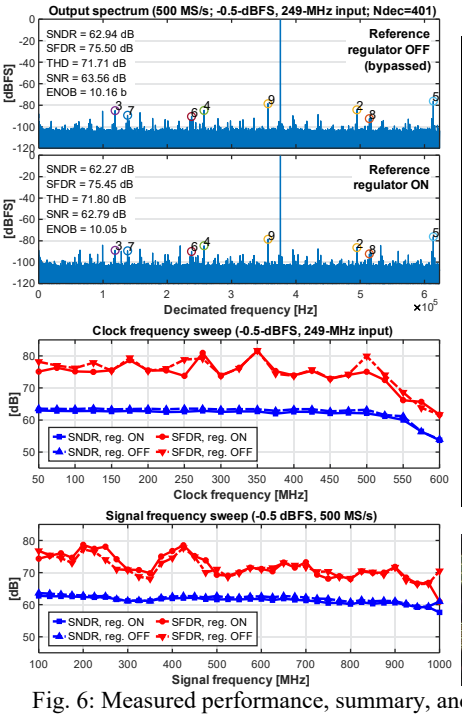


Fig. 5: Background calibration measurements.



Performance Summary

Technology	16nm CMOS	
Supply	0.9 V	
Sampling rate	1–500 MS/s	
Resolution	11.5 b	
Input range	1.8 $V_{pp,d}$	
Performance w/Nyquist input	Reference regulation	
	OFF	ON
ENOB [b]	10.16	10.05
SNDR [dB]	62.9	62.3
SFDR [dB]	75.5	75.5
THD [dB]	-71.7	-71.8
Power [mW]	2.8	3.3
FoM_W [fJ/c.s.]	4.9	6.2
FoM_S [dB]	172.4	171.1
Core area	0.0084mm^2	

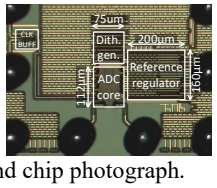


Fig. 6: Measured performance, summary, and chip photograph.