A 950 MHz Clock 47.5 MHz BW 4.7 mW 67 dB SNDR Discrete Time Delta Sigma ADC Leveraging Ring Amplification and Split-Source Comparator Based Quantizer in 28 nm CMOS

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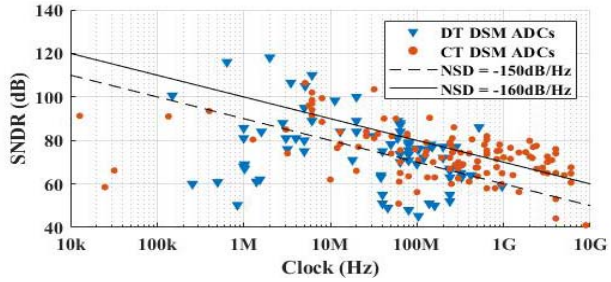
***Abstract*— This article presents a delta sigma modulator (DSM) analog to digital (ADC) that uses ring amplifiers as integrators to relax speed and efficiency bottlenecks in discrete-time (DT) oversampled ADCs. Its multi-bit quantizer is based on split source (SS) comparators, adding flexibility and power efficiency. The complete oversampling ADC is designed as a 3rd-order cascade of integrator with feed forward (CIFF) with a 4-bit quantizer, and it achieves a peak signal-to-noise and distortion ratio (SNDR) of 67 dB and DR of 70.0 dB with 47.5-MHz bandwidth when clocked at 950 MHz. This is the highest bandwidth reported to date among single-channel DT DSM ADCs and demonstrates a viable alternative to continuous-time (CT) DSM ADCs for wideband oversampling applications. With a power consumption of 4.7 mW from a 1-V supply, figure of merit (FoM) Schreier and Walden are 167.0 dB and 27.0 fJ/c.s, respectively, demonstrating efficient DT delta-sigma conversion with high bandwidth.**

***Index Terms*— Cascade of integrators with feed forward (CIFFs), delta-sigma modulation, discrete-time (DT) analog to digital (ADC), oversampling ADC, ring amplification.**

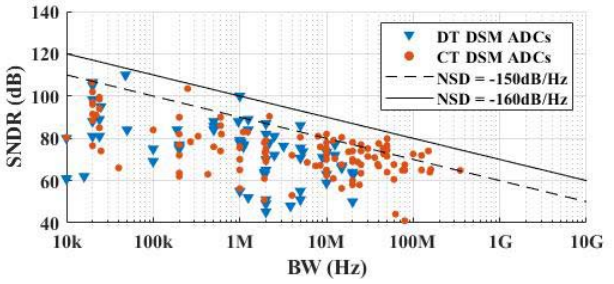
I. Introduction

DISCRETE-TIME (DT) delta sigma modulator (DSM) analog to digital (ADCs) were once the dominant choice in academia and industry to achieve high resolution over a low bandwidth, or even to achieve MHz bandwidth with moderate resolution needed for radio communication due to its easiness of design, component variation robustness and friendly clock scalability [1]. With CMOS scaling, the speed and power efficiency of digital logic increased, while analog transistor parameters did not improve or even degrade. In the long term, this favored the efficiency of ADCs strongly based on digital-like components and digital logic as the successive approximation register (SAR) ADC and its variations. Another architecture that benefited from a faster technology is the continuous time (CT) DSM ADC, which works around a loop filter that does not need to settle within a given amplification time in contrast to discrete-time (DT) DSM, and uses techniques such as component calibration and compensation paths to stabilize the structure at higher clocking speeds. Those architectures were successful enough to push the clock speed and consequently the bandwidth of oversampling converters to the GHz and hundreds of MHz range, respectively, as seen in Fig. 1.

In the meantime, the DT counterpart of oversampling converters has barely increased the clock speed to the GHz



(a)



(b)

Fig. 1. Comparison between state-of-the-art oversampling ADCs. (a) signal-to-noise and distortion ratio (SNDR) versus Clock frequency. (b) SNDR versus bandwidth.

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range, while having the bandwidth at a maximum of 20 MHz. In [2], a clock speed of 1.1 GHz was achieved when heavily relying on integrators calibration to account for the low gain-bandwidth (GBW) product of the operational transconductance amplifiers (OTAs), and even then the decimated bandwidth was only 16.6 MHz. In [3], ringamps were used to push the clock speed to 950 MHz, however, the use of a single-bit quantizer leads to a higher oversampling ratio (OSR) to achieve moderate SNDR in a 10-MHz bandwidth. Despite their slow improvement with CMOS scaling, DT DSM still benefits from robustness in variations dues to their switched capacitor implementation and easiness of design compared to CT DSM. Thus, the effort to improve their performance would bring those advantages to state-of-the-art designs.

Ringamps are known for their high linearity and efficient amplification in state-of-the-art gigasample pipeline ADCs [4], [5]. They benefit from large output voltage swings, efficient slewing, and dynamic bandwidth settling to achieve higher clocking speeds. This work leverages the benefit of ring amplification to push SNDR versus BW achieved by DT DSM ADCs, aiming at power efficiency and FoM regions previously dominated by CT DSM ADCs. It also relies on a multi-bit quantizer designed around dynamic split source (SS) comparators [6] to add power efficiency and flexibility in the threshold generation for the quantizer ladder.

This article is an extension of the work presented in [7]. It shows a simple feasible solution for DT DSM ADCs to achieve higher clock speeds and consequently higher bandwidth than previous DT designs, moving the specification range well within what was previously achieved only by CT DSM ADCs and other types of Nyquist ADCs. Section II presents a system-level overview of the DSM loop filter and the advantages of the use of ring amplification. Section III presents the circuit implementation of the key components in the ADC such as ring amplifiers, comparator, and threshold decision logic. Section IV summarizes the measurements and compares them with other state-of-the-art ADCs. And finally, Section V concludes the article.

II. System Level Overview

A. Effects of Finite DC Gain on Integration Modeling

Integration in a DT structure has two main specifications which are linked but lead to different bottlenecks: 1) the GBW sets the minimum feasible integration time window to achieve the target voltage within a certain accuracy and 2) the dc gain sets the maximum achievable accuracy, even with infinite integration time, due to steady-state errors. For a closed loop one pole dominant system step response, one can see both effects in the following equation, where β is the feedback factor:

$$y(t) = \frac{\mathrm{dc}_{\mathrm{gain}}}{1+\beta \mathrm{dc}_{\mathrm{gain}}}(1-e^{-t\beta \mathrm{GBW}}). \quad (1)$$

Recent work in 28-nm bulk CMOS such as [8] has OTAs in filters consuming 1-mW reaching 46 dB of dc gain, 7 GHz of GBW, and targeting SNR in the range of 60 dB. While on another note, works such as [5] uses ringamp in the MDAC implementation as the amplifier, being able to achieve up

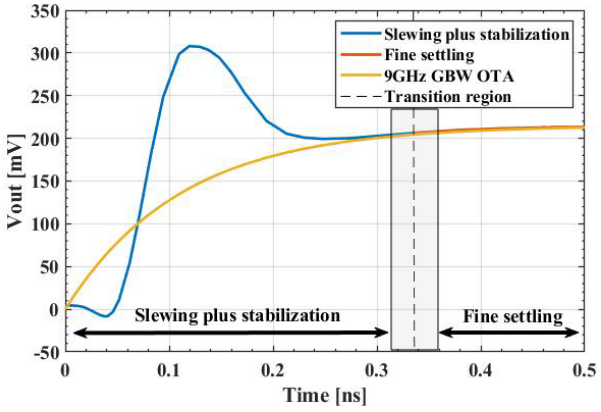


Fig. 2. OTA-based versus Ringamp-based integration.

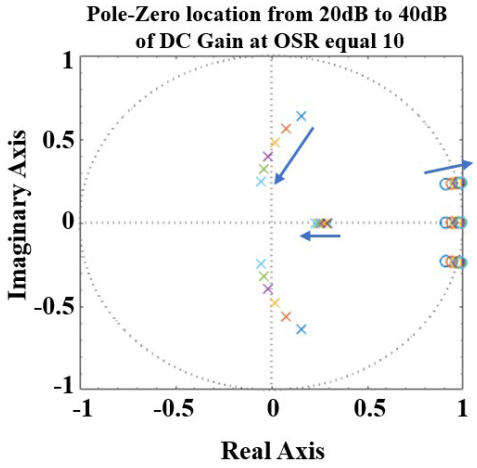


Fig. 3. Effects of finite dc on pole-zero location for a 3rd order CIFF architecture using (2). Arrow direction points to an increasing dc gain.

to 9 GHz of GBW for the same amount of power and target SNR. The high equivalent GBW is possible due to the adaptive bandwidth behavior of ringamps. To demonstrate that, Fig. 2 compares a simulated ringamp-based integrator in 28 nm with an ideal one pole 9-GHz GBW OTA settling with unity-gain feedback. Since the fine settling phases coincide, the ringamp-based integrator has an equivalent GBW of 9 GHz. The explanation to this high equivalent GBW can be better seen if we divide the ringamp behavior in two phases: 1) a slewing plus stabilization phase, where the output stage drives with the maximum slew rate the output load and 2) a fine settling phase, where the ringamp is locked to its deadzone, thus putting the output stage in weak inversion and accurately approaching the final value. The transition moment between the phases is modulated with the deadzone sizing, which has an optimal value for a given clock speed since the right balance between the fast but inaccurate first phase and slow and accurate second phase can lead to an equivalent GBW of 9 GHz as simulated.

B. Loop Filter and Ringamp Co-Design

A simple first-order approximation of the dc gain effects on the settling of a DT structure leads to the modified integrator

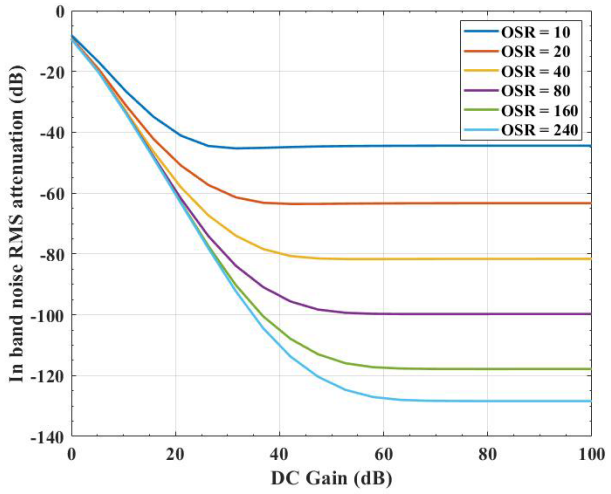


Fig. 4. Effects of finite dc on in-band quantization noise attenuation for a 3rd order CIFF architecture using (2).

transfer function of the following equation:

$$H(z) = a_1 \frac{\mathrm{dc}_{\mathrm{gain}}}{1+\mathrm{dc}_{\mathrm{gain}}} \times \frac{z^{-1}}{1-\frac{\mathrm{dc}_{\mathrm{gain}}}{\mathrm{dc}_{\mathrm{gain}}+1} z^{-1}} \tag{2}$$

where a_1 denotes the scaling coefficient of the closed loop gain of the integrator. This equation, albeit simplified, is going to help in the process of architecture optimization by creating a link between the circuit performance of ringamp-based integrators and the system-level model. From the system level part, a sweep across increasing equivalent dc gains will modify the NTF, moving the zeros toward the border of the unit circle as seen in Fig. 3, which will improve the NTF up to a maximum. The curves in Fig. 4 show this degradation for a 3rd-order loop filter with a 16 level quantizer optimized for a given OSR. Note that while low OSR structures achieve smaller in band noise rejection, they benefit from a smaller equivalent dc gain requirement to achieve their maximum SQNR.

From the circuit simulation side, a 1-GHz test bench integrator around a differential ringamp (see Section III-A for circuit implementation) is simulated to extract the equivalent dc gain to fit (2). To simplify the multidimensional characterization of an integrator (input voltage versus stored voltage), we use a two-point extraction approach. First, we excite with a differential input the integrator with an uncharged integration capacitor and measure the gain error with respect to the ideal value leading to the equivalent dc gain from the closed loop gain (which modifies the coefficient a_1). Second, we excite with zero differential signal the integrator with a pre-charged integration capacitor and measure the attenuation of the capacitor charge leading to the equivalent dc gain from attenuation (which multiplies z^{-1} in the denominator).

From our system level analysis, a maximum in band noise rejection can be achieved for an OSR of 10 when the equivalent dc gain is higher than 30 dB. From the plot in Fig. 5, it is seen that the ringamp can achieve that threshold for both closed loop gain and attenuation across 80% of V_{DD} of output range when optimally biased. The dc gain variations

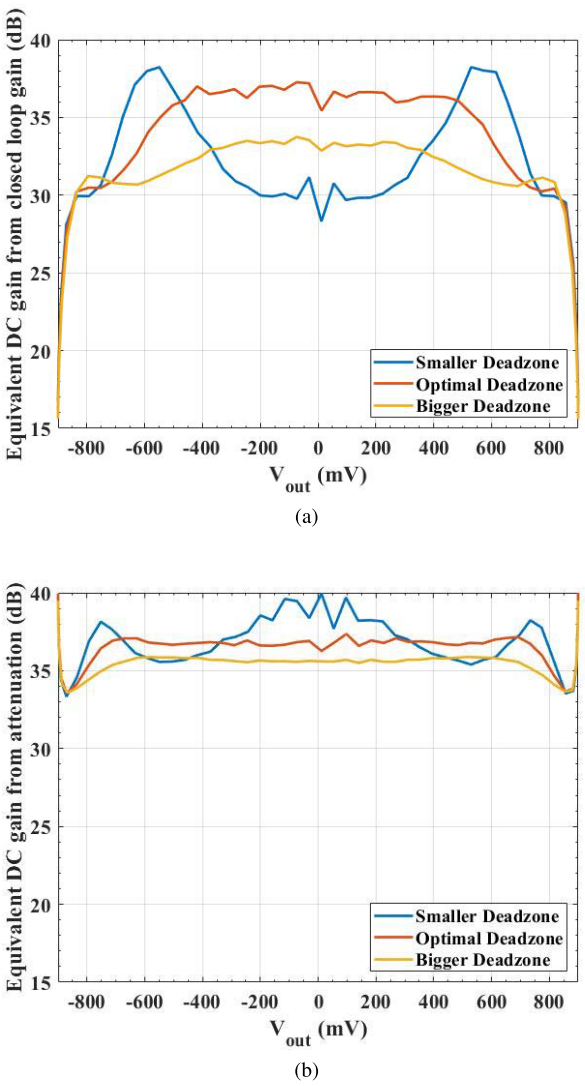


Fig. 5. Simulation of ringamp-based integrator to extract the equivalent dc gain versus output voltages from the (a) closed loop gain and (b) attenuation.

concerning biasing variations can be seen in the following way: a smaller deadzone leads to an under-damped settling (longer slewing phase) which leads to higher uncertainty in the output value due to settling errors. On the other hand, a bigger deadzone leads to an over-damped settling, which leads to a slower settling to the final state, thus also degrading the equivalent dc gain at higher clocks.

The conclusion of this first analysis guides us to set the OSR at 10 since the equivalent dc gain to provide −45-dB rms in band noise attenuation can be achieved when clocking the integrators at around 1 GHz.

C. Third Order CIFF

The DSM architecture of choice for this work was the cascade of integrators with feed forward (CIFFs) with a bypass of the input signal to the quantizer. This architecture decouples the input signal from the loop filter processing chain, we enable higher coefficients after dynamic scaling, thus smaller input-referred contribution of amplifiers non-idealities.

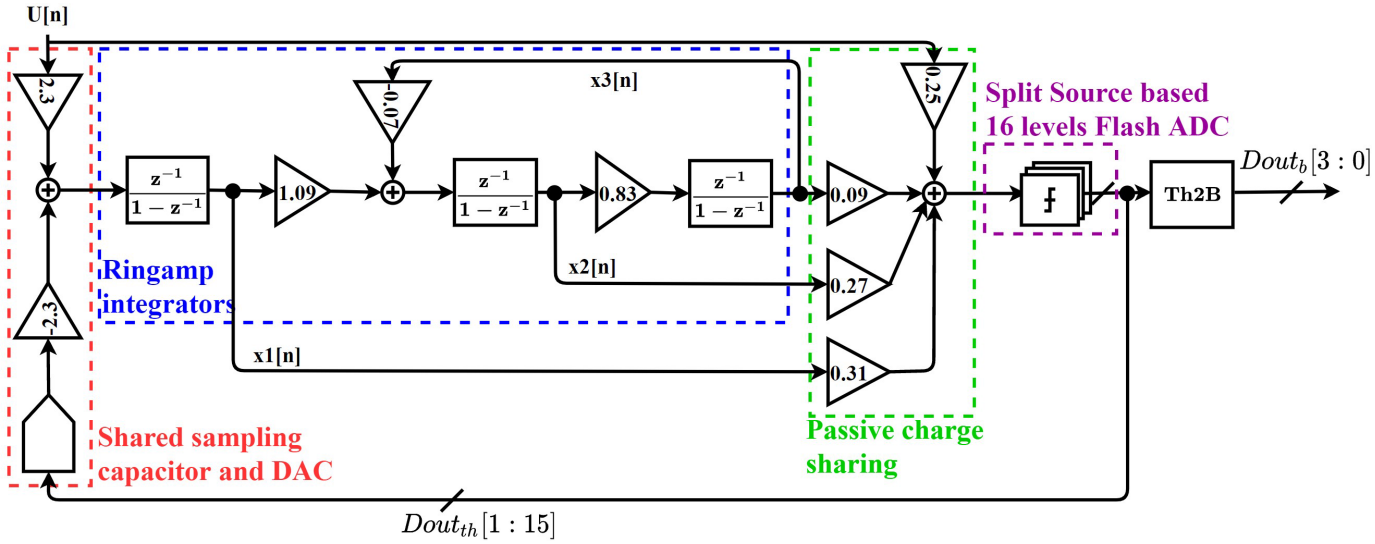


Fig. 6. Top level model of the CIFF DSM ADC with highlight to the techniques of the core parts.

The absence of digital to analog converter (DAC) loading in every stage besides the first also leads to an easier ringamp characterization and design.

With the loop filter order and the number of quantization levels decided in the previous section, the architecture could be optimized for a given OSR using a CLANS synthesis [9]. Followed by a step of dynamic scaling to ensure the full output range of the ringamps is being used, the final ABCD matrix is:

$$ABCD = \begin{bmatrix} 1 & 0 & 0 & 2.38 & -2.38 \\ 1.08 & 1 & -0.07 & 0 & 0 \\ 0 & 0.82 & 1 & 0 & 0 \\ 0.31 & 0.27 & 0.09 & 0.25 & 0 \end{bmatrix}. \quad (3)$$

To save power the summation node is implemented as a charge sharing summation and to account for its corresponding attenuation, the quantizer LSB is scaled accordingly. The final architecture is shown in Fig. 6 highlighting the main techniques used in this work. A single-ended schematic for the ringamp based loop filter is presented in Fig. 7. To enable the charge sharing summation, the time scheduling of Fig. 8 was proposed, where the integration processes, which happen all in the same phase, are the bottleneck of the clocking speed. Extra capacitors are used at the output of the integrators to align the phases of the integration processes by resampling the output of the integrators. The attenuation of 2 caused in this process is accounted for in the design of the integrator coefficients. Quantization happens in the same phase as sampling.

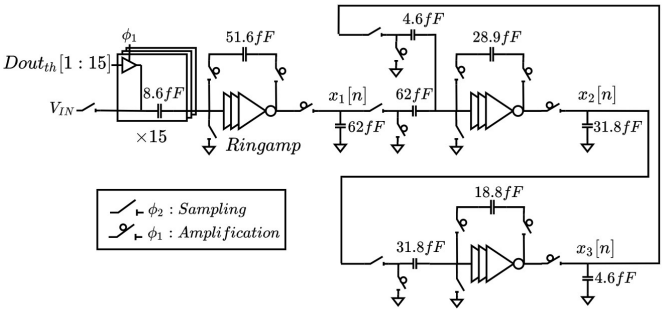


Fig. 7. Single-ended model of the loop filter with switches phases.

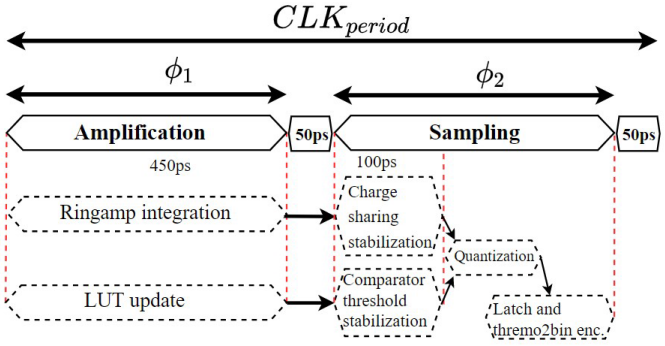


Fig. 8. Time scheduling to enable the power saving techniques of the architecture.

III. Circuit Implementation

A. Ring Amplifier and Integrators

The schematic of the ringamps used in this design is depicted in Fig. 9 [4]. They have a differential input stage with a CMOS resistor implementing the dead-zone voltage in the second stage. Controlling the dead-zone voltage allows achieving better noise shaping by setting the settling performance to an optimal value. This ringamp improves its power efficiency by having a power-down capability when all the CMOS switches are put in a high impedance mode, cutting down the static current. Another advantage is regarding the local feedback between the second stage input and the first stage current source, enabling a fast path for common-mode feedback. At the same time, an external capacitive division between the outputs gives rise to another slower CMFB signal, which is also fed to the ringamp 1st stage.

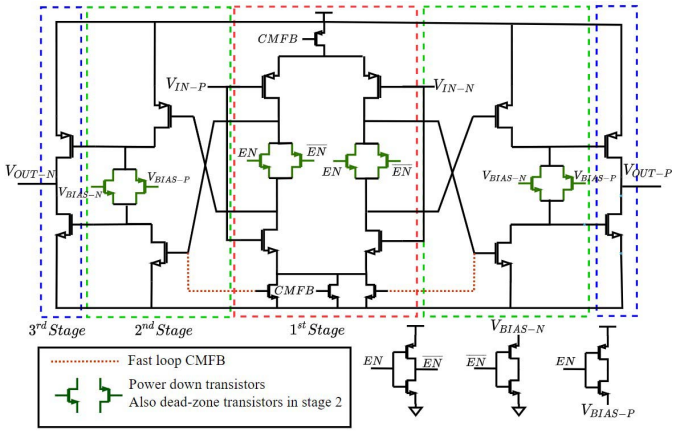


Fig. 9. Differential ringamp schematic.

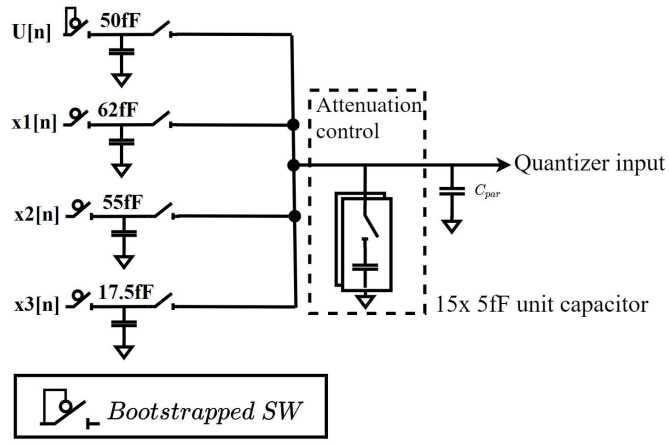


Fig. 10. Top plate charge sharing summation with depicted gain calibration.

The ringamp-based integrator does not differ a lot from the regular OTA-based integrator. Care must be taken when powering down the ringamp so that the charge in the integration capacitor is not lost. This is done by isolating the top and bottom plates of the capacitor using CMOS switches when not integrating.

The input capacitor of the first integrator is sized to set the sampled thermal noise 6 dB higher than the in band quantization noise, thus limiting the overall SNDR of the ADC. For the other stages, the input capacitors are sized considering that each integrator will add 15 dB of gain for the loop filter. Thus, a scaling factor of 2 was chosen between stages to prevent the noise from stages 2 and 3 to be significant when referred to the input. A higher scaling factor would be possible from a noise budget perspective but does not make sense as capacitors would become too small, and the design would be dominated by parasitics.

B. Quantizer and Summing Node

The summation node of the integrators' output and the quantizer were also co-designed in this work. The reason for that decision was to increase power efficiency at the same time

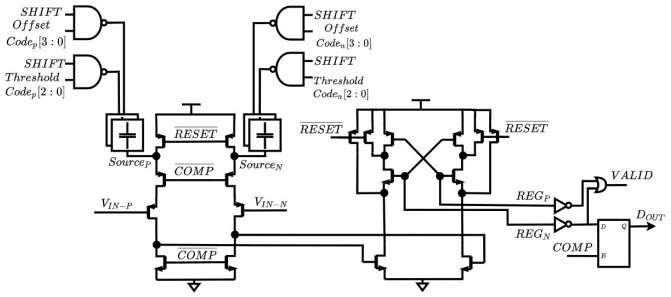


Fig. 11. SS comparator schematic showing threshold level programmability and offset correction via the DAC at the sources of the input pair.

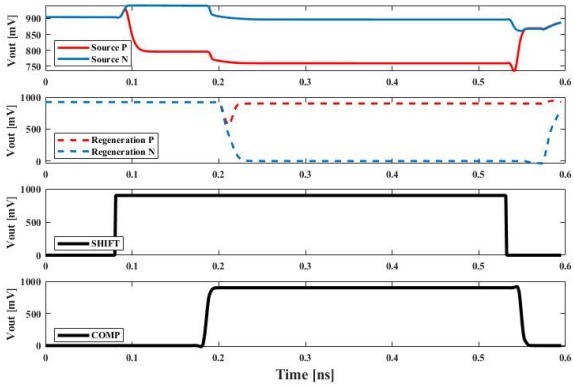


Fig. 12. SS Comparator voltages over time, showing the source shift to create the threshold voltage.

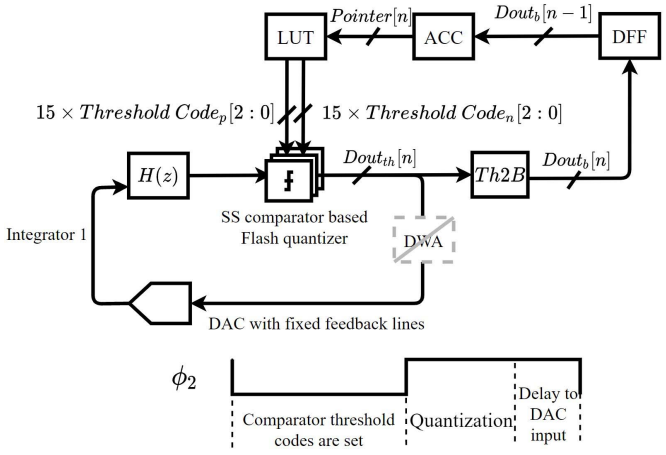


Fig. 13. LUT-based threshold decision model.

enabling a fully dynamic power consumption and flexibility with the use of the SS comparators.

The scheduling of the amplification process enables the sampling in the summation node to occur at the same clock phase. In that case, the most power-efficient solution to sum the sampled voltages is to share the top plate of the sampling capacitors. Top plate capacitor sharing comes at the cost of signal attenuation proportional to the sum of the required coefficients. That attenuation can be accounted for in the quantizer design, thus creating a summation plus quantization process

which is transparent to attenuation from the architecture point of view.

The design follows then to implement a Flash quantizer with a fixed gain of G_Q by design, and a summation node with an attenuation of $1/G_Q$(cal). This attenuation can be easily calibrated to match the quantizer gain by adding extra capacitors to the summation node as shown in Fig. 10.

The flash quantizer ladder is built around SS comparators. Such comparators consist of a pMOS input pair with different voltages across their sources, which translates to an equivalent threshold voltage when referred back to the input. The source voltages are pre-charged to VDD and the voltage difference is created by the capacitive DAC (CDAC) shifting the p and n side to the corresponding voltages set by the threshold code. To increase the conversion speed, they have a common mode step up together with the threshold settling. The comparator schematic is depicted in Fig. 11 and the source voltage behavior can be evaluated in the voltage waveforms in Fig. 12.

The use of this comparator comes with the need for extra settling time for the input sources to the required voltages. In our design, that process happens concurrently with the loop filter output summation, thus adding no delay to the quantization process. A 100-ps time window is scheduled for that settling. The following quantization process is done in a flash ADC manner, thus being in the worst case as slow as the slowest comparison (differential signal close to the threshold voltage). In our simulations, that led to a quantization time of at most 100 ps. Thus, the whole process of summation plus quantization fits well within the allocated 450-ps time frame, leaving the ring amplification time as a bottleneck for clock scaling. Extra capacitors are added in parallel with the threshold code capacitors to enable input pair offset correction capability, covering a range of ± 30 mV which corresponds to a 3σ spread.

C. LUT-Based Threshold Code Generation

The capability of easily programming the thresholds per comparator is the feature that enables a per conversion rotation of the quantizer ladder. This rotation of comparators with fixed feedback lines can be used to implement the dynamic element matching (DEM) of the input DAC. This structure also moves the DEM calculation out of the critical timing path. In our design, the correspondent threshold code for each comparator is controlled by a lookup table (LUT) and an accumulator to implement Data Weighted Averaging, as shown in Fig. 13. This technique is an improvement of [10] and [11], where besides using a switching matrix, the shuffling is implemented fully digitally and provided to the comparator DACs for reference generation.

Despite the DEM capability, the fabricated IC was measured with the rotation off (fixed codes every cycle) since the input capacitors matching was within the technology parameters, and it was not the main source of performance degradation. Rather, the LUT size, switching activity, and proximity to the comparators led to supply bounce on the reference used to generate the comparators thresholds, thus creating mismatch in the thresholds that degraded the system performance by some dBs when turned on. With a careful layout and dedicated supply, those problems could be overcome in a following implementation.

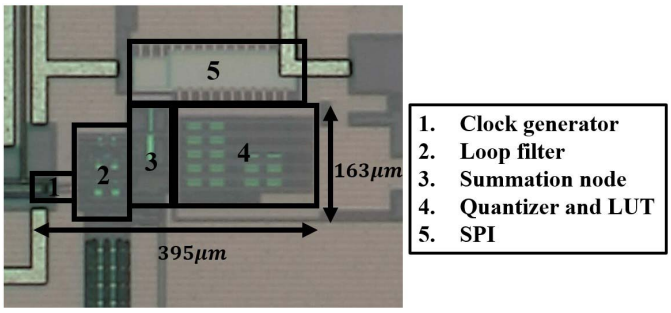


Fig. 14. Die photograph with description of components and dimensions for the core area of the ADC.

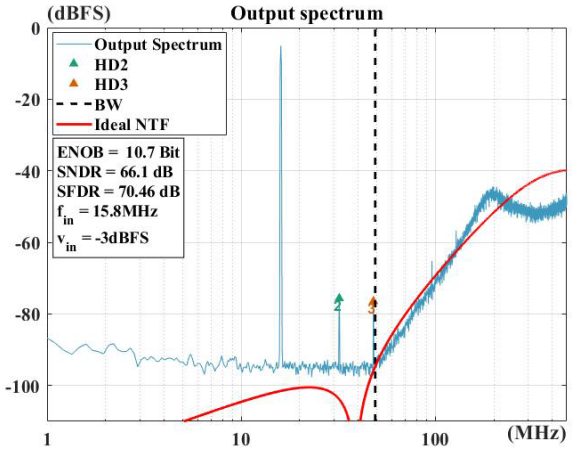


Fig. 15. 8k-points FFT with PSD averaging at 950-MHz clocking frequency and near maximum stable amplitude (MSA) input.

IV. Measurement Results

The ADC is fabricated in a 1P9M 28-nm CMOS process with a core area of only 0.064 mm^2 as shown in Fig. 14. An SPI circuitry was foreseen to control the calibration bits of the core ADC and the IO drivers. Fig. 15 shows a sample FFT from the output signal with 66-dB SNDR over a 47.5-MHz bandwidth. When clocked at 950 MHz (decimated bandwidth of 47.5 MHz) it consumes 4.7 mW. The biggest source of power consumption in this design is the quantizer (50%) due to its flash architecture, while the amplifiers are responsible for only 25% of the total power (see Fig. 16). In Fig. 17 the input power is swept across the full scale of the ADC and the DR is found to be 70 dB.

The foreground calibration of the ADC was performed off-chip using MATLAB, namely the comparator offset, the charge sharing node attenuation, and the ringamp deadzone bias voltage. From a sensitivity point of view, the first integrator deadzone biasing is the one affecting the most the overall peak SNDR as it would be expected, since the settling errors of the other integrators have 30 and 45 dB of rms attenuation when referred to the input. In Fig. 18, one can see the peak SNDR variation versus the first integrator bias. Even though

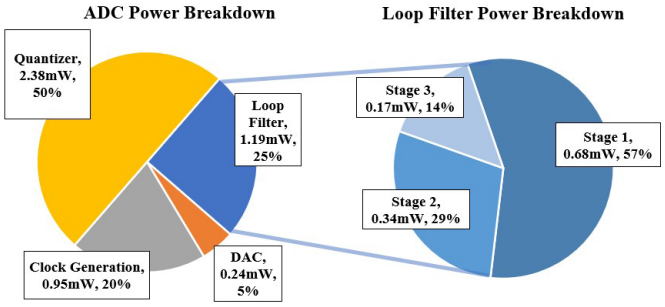


Fig. 16. Power breakdown when clocked at 950 MHz with input power close to MSA. DEM code generation consumes an extra 1.6 mW when clocking at 950 MHz.

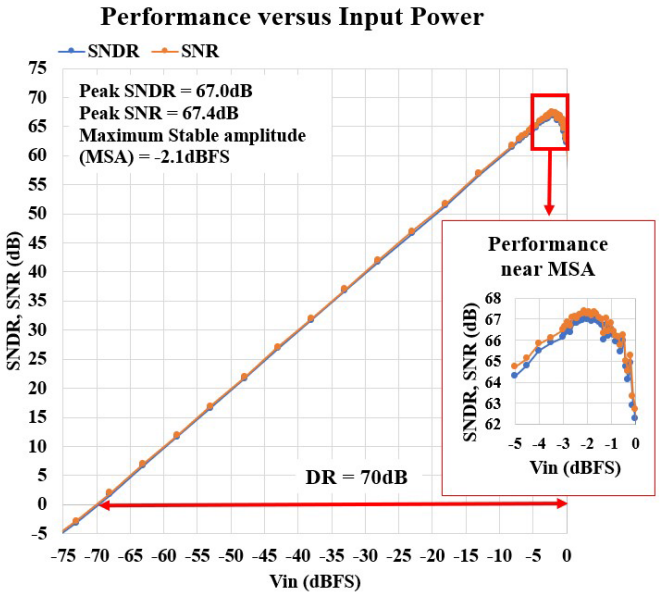


Fig. 17. Input power sweep when clocking at 950-MHz showing the peak SNDR and the Dynamic Range of the ADC.

TABLE I
ADC PERFORMANCE ACROSS CLOCK FREQUENCIES

$Clock\ (MHz)$	500	700	900	**950**	1000
$BW\ (MHz)$	25	35	45	**47.5**	50
$SNDR\ (dB)$	67.5	67	67	**67**	65.7
$ENOB\ (bits)$	10.9	10.8	10.8	**10.8**	10.6
$Power(mW)$	3.0	3.8	4.6	**4.7**	4.9
$FoM_S\ (dB)$	166.7	166.6	166.9	**167.2**	165.8
$FoM_W\ (fJ/c.s.)$	31	29.7	27.9	**27.0**	31.1

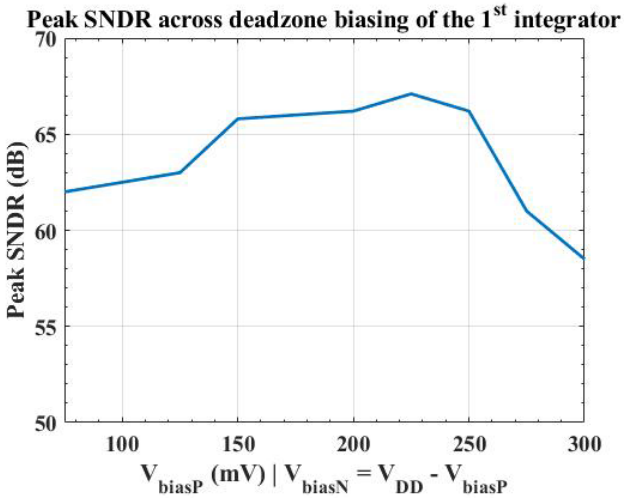


Fig. 18. SNDR dependency on bias voltage of the first integrator.

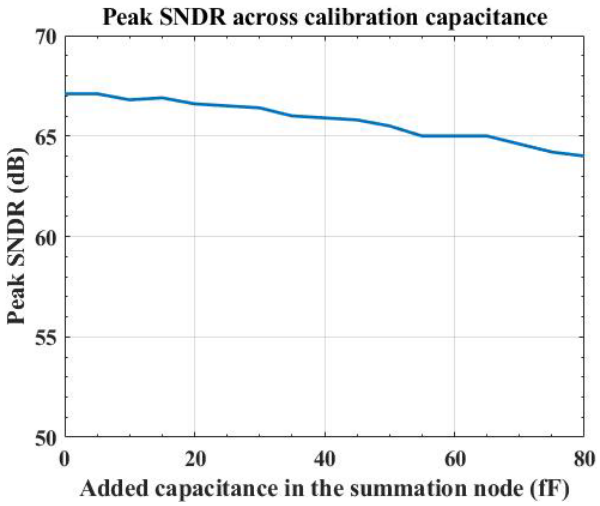


Fig. 19. SNDR dependency on added capacitance to the summation node.

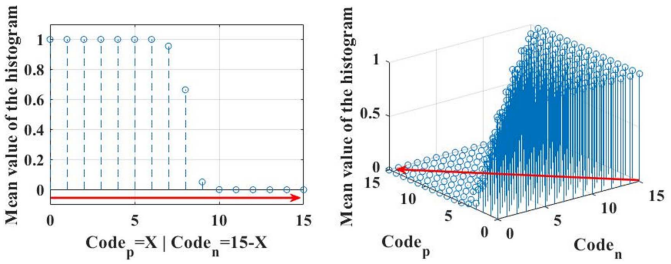


Fig. 20. Sample of calibration plane and line for offset correction. The red arrow indicates the same code direction among the two plots.

an optimal single point can be found using the best SNDR, one may note that there is a 100-mV bias range where the achieved SNDR degradation is less than 1 dB from its peak value. For the second and third integrators, the variation is even smaller for a wider range, so their bias points are chosen to be the same as the first integrator. Although we separated all the bias lines in this works, this shows that they could safely be connected with enough decoupling to save space on the number of required bias generators.

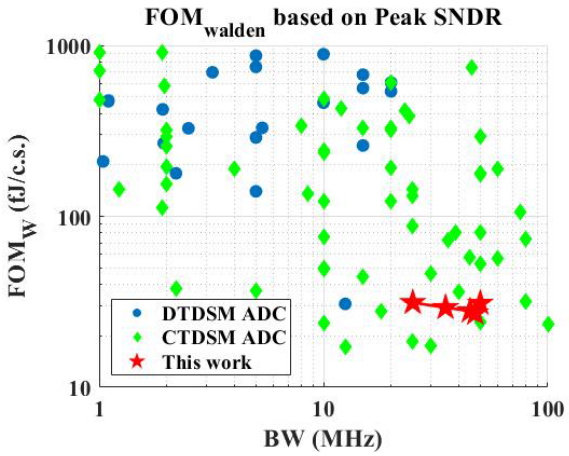
As for the calibration of the summation node, Fig. 19 shows the peak SNDR profile when sweeping across the added capacitance. The global peak SNDR is achieved close to the lower bound of the calibration range, indicating that there was more parasitic in that node than it was estimated, but still within the designed range. Finally, to calibrate the comparator offsets, a zero differential signal was sampled at the quantizer input and one comparator was enabled at a time. The output data readout would give rise to a 0/1 balance which can be plotted as a mean value for a long simulation as in Fig. 20.

After calibration, the converter achieved a peak SNDR around 67 dB (ENOB of 10.8b) with the clocking frequency varying from 500 to 950 MHz with a slight degradation of 1.3 dB when clocked at 1 GHz as summarized in Table I. In this frequency region, the power consumption also scales

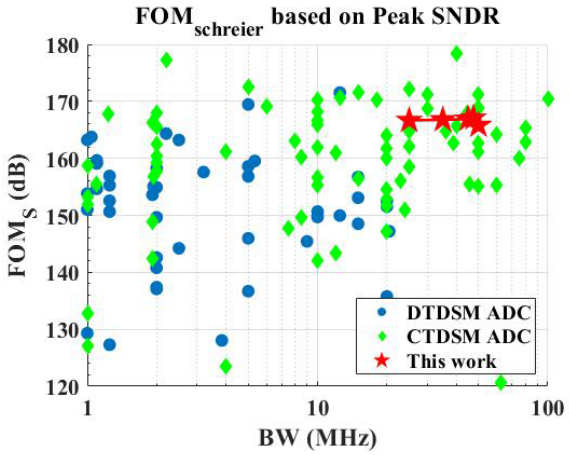
TABLE II
COMPARISON WITH STATE-OF-THE-ART ADCS TARGETING SIMILAR BANDWIDTHS

	This work	Y. Song VLSI 18 [12]	S. Wu JSSC 13 [2]	C. Lee VLSI 13 [13]	B. Carlton VLSI 11 [14]	T. He ISSCC 18 [15]	C. Wang ISSCC 19 [16]	W. Wang ISSCC 19 [17]	P. Cenci VLSI 19 [18]
Architecture	*DT*	*DT*	*DT*	*DT*	*DT*	*CT*	*CT*	*CT*	*CT*
Node	$28nm$	$65nm$	$65nm$	$22nm$	$32nm$	$28nm$	$28nm$	$28nm$	$28nm$
Power (mW)	4.7	4.5	94	12.7	28	64.3	7.3	16.3	3.2
Clock (MHz)	950	200	1100	240	400	2000	960	2000	2400
OSR	10	8	32	8	10	20	6	10	30
Bandwidth (MHz)	47.5	12.5	16.6	15	20	50	80	100	40
SNDR (dB)	67	77.1	74.3	66	63	79.8	64.9	72.6	77.5
DR (dB)	70	78.5	81	–	66	82.8	68	76.3	78.2
FoM_{S-SNDR} (dB)	167.0	171	156	156	151	168.7	165.3	170.5	178.5
FoM_{S-DR} (dB)	170.0	172	163	–	154	171	168	174	179
FoM_W $(fJ/c.s.)$	27	31	667	259	606	80	32	23	6

FoM_S = (SNDR or DR) – 10*log10(Power/BW); FoM_W = Power/((2*BW)*2^(ENOB))



(a)



(b)

Fig. 21. Comparison of this work at different clocking frequencies from Table I with the state-of-the-art using (a) Walden figure of merit and (b) Schreier figure of merit.

accordingly, leading to a Walden FoM between 27 and 31 fJ/c · s; all the decimated bandwidths are taken using an OSR of 10 with respect to the clocking speed, thus ranging the Schreier FoM from 165.8 to 167.2 dB. When taking the peak performance at 950 MHz and comparing with it the state-of-the-art DT and CT DSM ADCs (see Table II), one can see that this work achieves at least 2× more bandwidth than any other single-channel DT design with a power efficiency on par with CT DSM ADCs aiming similar application bandwidth.

V. CONCLUSION

This work successfully showed that ringamp-based integrators can achieve high clocking speeds in DT DSM ADCs, pushing the bandwidths to regions previously only achieved by the CT counterparts while keeping the power efficiency on par with the state-of-the-art. The achievable performance was mainly possible due to: 1) the ringamp fast and efficient amplification; 2) a careful but simple system-level and circuit-level co-design optimization; and 3) SS comparators adding flexibility with dynamic power consumption. It was shown that ringamps could achieve the required dc gain and GBW for the proposed architecture targeting moderate SNDR at GHz range clocking speed in a very efficient manner.

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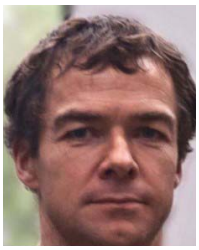

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