A 4.6K to 400K Functional PVT-Robust Ringamp-Based 250MS/s 12b Pipelined ADC with Pole-Aware Bias Calibration

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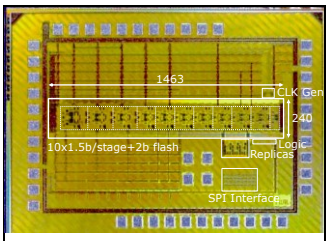
Ring amplifiers (ringamps) have been shown to improve pipelined ADC performance by relaxing the traditional bottleneck imposed by power-hungry class-A residue amplifiers [1,2]. However, the operation of several high-performance ringamp structures is heavily dependent on device parameters and supply voltage, and thus, often sensitive to PVT variation. This creates challenges for applications in extreme environments, such as cryogenic quantum computing, space, and automotive. To overcome this issue, this work introduces a PVT-robust ringamp with pole-aware bias calibration and a bias-enhancement technique. Furthermore, to deal with insufficient gain in advanced CMOS, we also propose a cascode Correlated Level Shifting (cascode-CLS) technique. These three techniques enable a prototype 12b 250MS/s pipelined ADC that achieves SNDR higher than 55dB across 4.6K to 400K operating temperature range without requiring gain calibration. To the best of our knowledge, this work is the first pipelined ADC reported to operate at less than 40K.

There are several approaches to realizing a PVT-robust ringamp. The most common way is to control the 3rd stage deadzone voltage size [1], but this leaves the 1st and 2nd stages uncontrolled, resulting in remaining PVT sensitivity. This is addressed in [2] by controlling all three stages with class-AB biasing and AC-coupling capacitors. However, coupling capacitors between stages add parasitics to critical internal nodes of the ringamp, reducing speed and power efficiency, and the use of a constant current source as a reference leads to excessive mobility and transconductance variation in extreme (cryogenic) environments. This is especially critical when operating in the near sub-threshold region [3], which is the case for the 3rd stage of a ringamp. The resulting variability requires a design with very large stability safety margins, which limits the ringamp bandwidth.

Fig. 1 shows the basic concept of the proposed pole-aware bias calibration. The idea is to 1) fix the amplifier bandwidth by tuning a dominant 3rd stage pole (P3), and then 2) adjust non-dominant 1st and 2nd stage poles (P1, P2) to create optimal phase margin. To realize this, we utilize a constant-gm circuit with poly-resistor (not shown) whose sensitivity to temperature is much smaller than transistors [3] as a reference of the 3rd stage current (I_3). Since P3 is the dominant pole, constant 3rd stage transconductance (Gm_3) ensures constant amplifier bandwidth throughout extreme PVT conditions. After the 3rd stage is biased in this PVT-insensitive manner, 1st and 2nd stage currents (I_1, I_2) are adjusted to the minimum value that can stabilize the ringamp by measuring the stability of the ringamp with a settling detector.

Fig. 2 shows the pole-aware bias calibration implemented by utilizing a replica ringamp, whose transistors are sized identical to the main ringamp. The use of the replica is beneficial in terms of performance; we can avoid adding additional components to the main ringamp. Additionally, we implement a background settling detector in the main CLS circuit to directly detect the ringamp stability to tune P1 and P2. The replica ringamp controls I_3 to match the reference current (I_{CGM}) generated by the constant-gm circuit, by comparing I_3 and I_{CGM}. In this way, Gm_3, i.e., the bandwidth, is kept constant. I_2 is also controlled to lock at a specific ratio against I_1 (0.5 in this design), to set P1 and P2 at a similar frequency. Meanwhile, the settling detector measures whether the biasing values of I_1 and I_2 are sufficient to stabilize the main ringamp by monitoring the internal node of the level shifting capacitor (V_{CLSi}) after the 2nd amplification phase (ϕ_2) of CLS. The principle here is that any incomplete settling due to sub-optimal biasing during the 1st amplification phase (ϕ_1) will increase the error amplitude that must be corrected by CLS in ϕ_2. With more optimal biasing, we achieve smaller average error amplitude of V_{CLSi} at the end of ϕ_2. In this prototype, this is sensed using a peak detection comparator with a predetermined built-in threshold. Even if CLS is not used, the general concept of pole-aware bias calibration can be applied with other form of settling monitoring (e.g., stochastic ADC [1]).



Die micrograph.

The full calibration procedure is depicted in the right part of Fig. 2. First, I_1 is initialized to a minimum value. Then on each iteration, the replica circuit uses I_1 and the constant-gm circuit to set I_2 and I_3, respectively. The number of incomplete settling events, which is well correlated with SNDR and SFDR as shown in the top left of Fig.5, is counted for a fixed number of clock cycles. If this count exceeds a certain threshold, I_1 is increased, and the procedure is repeated.

CLS is often used to deal with insufficient gain in advanced CMOS [4]. However, it suffers from speed degradation, and the resulting gain is sometimes still not sufficient. We introduce a cascode-CLS technique that further enhances accuracy and speed without performance overhead. As shown in Fig. 3, the ringamp output is shorted directly to V_{OUT} during ϕ_1 and then connected to V_{CLSi} through cascode transistors during ϕ_2. Since required output swing is small in ϕ_2, the cascode transistors do not decrease the output voltage range. Also, since large driving power is only required in ϕ_1, the static biasing of the cascode transistors during ϕ_2 does not encumber the ringamp speed. The obtained extra gain via cascode-CLS can be utilized either for more accuracy or speed by allowing larger errors to occur in ϕ_1 and/or reducing the size of C_{CLS}, or combination of both.

Fig. 4 shows the schematic of the proposed fully differential ringamp. Bias voltages for a tail current source and CMOS resistors are generated by trapped charge bias control [1] and controlled by the pole-aware bias calibration. Although this topology is beneficial in terms of common-mode stability, the 1st stage suffers from reduced voltage headroom due to dual PMOS and NMOS current sources. This is especially critical at low temperature where threshold voltage increases significantly beyond nominal, e.g., >100mV at 4K [3]. To mitigate this effect, we propose a bias-enhancement technique; the input transistor bias is optimized by adding different offsets to PMOS and NMOS, respectively, via separate AC-coupling capacitors. They are refreshed by charge transfer such that the gate voltage of the NMOS is higher than the common-mode voltage and vice versa for PMOS to ensure that all transistors operate in saturation.

A prototype ADC is fabricated in 65nm CMOS. The top-level system architecture is shown in the bottom of Fig. 4. The single channel 12b pipelined ADC consists of ten 1.5b stages followed by a 2b flash. The ringamps in the first three stages use dedicated replicas and settling-detectors, and their bias-codes are determined independently. The ringamps in stage 4 to 10 re-uses the bias-codes of stage 3.

Fig. 5 and 6 summarize the ADC performance. The ADC has been tested at 4.6K, 87K, 300K and 400K. Operating at 250MS/s, it achieves SNDR higher than 55dB for Nyquist input signal across temperature. Furthermore, measured four chips show less than 2dB SNDR variation across 250mV supply voltage deviation at 300K. These results demonstrate the robustness of the proposed ringamp against PVT variation. It also achieves Walden FoM of 183fJ/conv.-step at 4.6K, which is competitive compared with a state-of-the-art cryogenic ADC [5].

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References:

[1] B. Hershberg *et al*., “A 4-GS/s 10-ENOB 75-mW Ringamp ADC in 16-nm CMOS With Background Monitoring of Distortion,” JSSC, Aug. 2021.

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[3] J. van Dijk *et al*., "Cryo-CMOS for Analog/Mixed-Signal Circuits and Systems," CICC, Mar. 2020.

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[5] G. Kiene *et al*., "A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS," ISSCC, Feb. 2021.

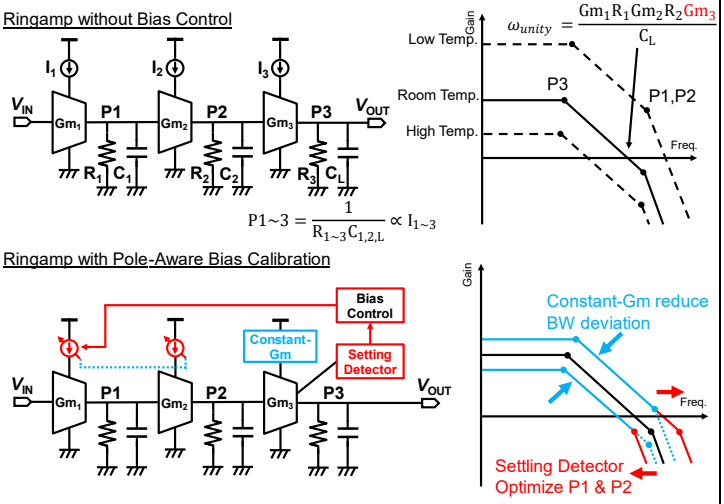

Fig. 1. Small signal model of ringamp with and without proposed pole-aware bias calibration

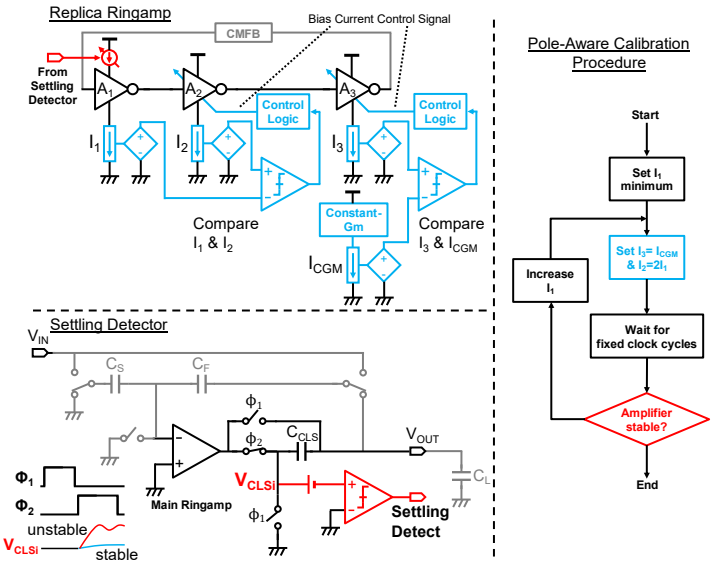

Fig. 2. Implementation of pole-aware bias calibration

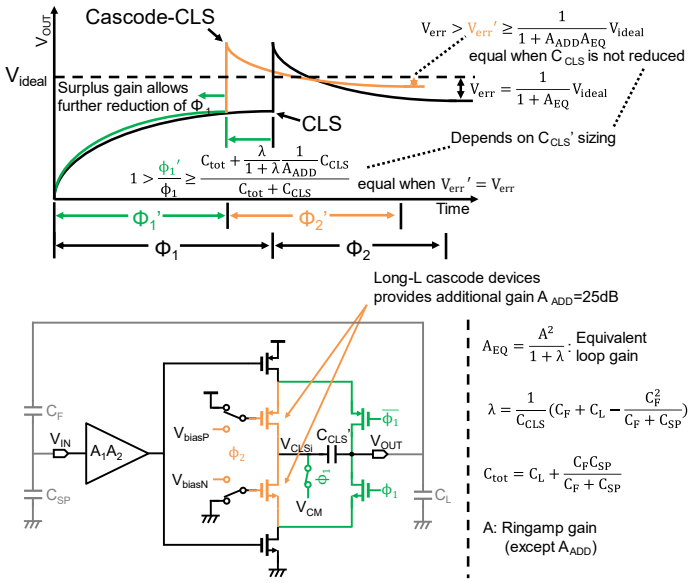

Fig. 3. Operation of cascode-CLS ringamp

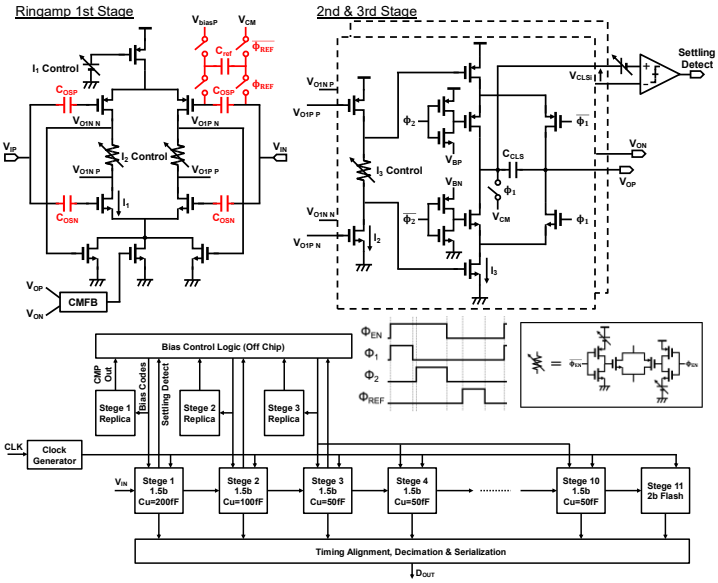

Fig. 4. Ringamp schematic and prototype ADC top-level

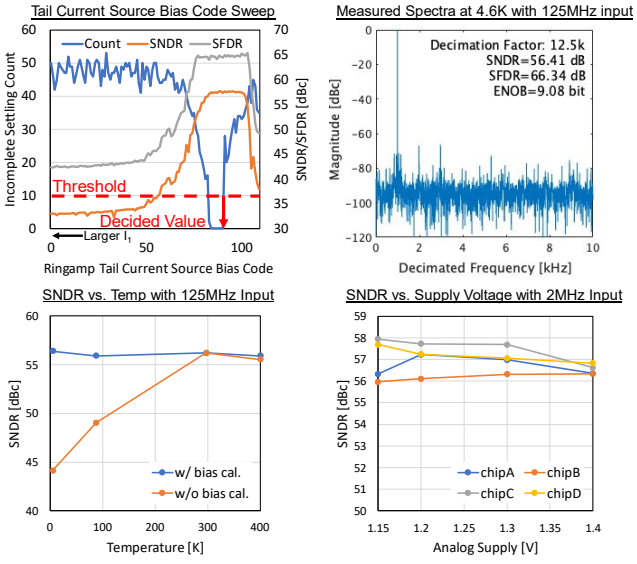

Fig. 5. Tail current source bias code sweep, measured spectra at 4.6K, and SNDR variation across temperature and supply voltage

	This work			Kiene, ISSCC 2021 [5]		Okcan, RSI 2010		Lagos, JSSC 2019
Temperature [K]	4.6	300	400	4.2	300	4.4	300	300
Technology [nm]	65			40		350		28
Architecture	Pipelined			TI-SAR		SAR		Pipelined
Sampling rate [MS/s]	250			900	1000	0.05		600
Resolution [bit]	12			6-8		12		12
Supplies [V]	1.3[1]	1.2		1.1(core), 2.5(clock)		3.3		0.9
Input range [Vpp]	2.0			0.7		-	-	1.6
SNDR@LF [dB]	-[2]	57.7	55.8	-	-	53.1	64.8	59.0
SFDR@LF [dB]	-[2]	65.3	61.1	-	-	-	-	71.9
SNDR@Nyquist [dB]	56.4	56.2	55.9	36.2	33.4	-	-	58.7
SFDR@Nyquist [dB]	66.3	61.4	60.5	48.5	48.4	-	-	72.4
Power [mW]	24.7[1]	28.3	32.4	10.6	10.3	0.297	-	14.5
FoMw [fJ/c.step]	183[1]	215	254	200	260	16100	4188	34.4
FoMs [dB]	153[1]	153	152	143	140	135	147	161.9
Core Area [mm²]	0.484			0.045		2.7[3]		0.621
Gain Calibration Free?	Yes			-		-		No

1: Including 100mV voltage drop in the cryostat 2: Not measured due to increased loss from balun 3: Full chip

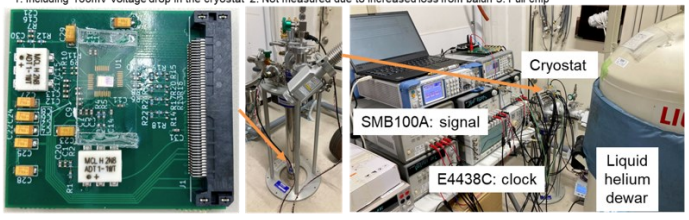

Fig. 6. Comparison table and cryogenic measurement setup