A 4.6–400 K Functional Ringamp-Based 250 MS/s 12 b Pipelined ADC With PVT-Robust Unity-Gain-Frequency-Aware Bias Calibration

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***Abstract*— This article presents a process voltage temperature (PVT) -robust ring amplifier that enables a high speed pipelined analog-to-digital-converter (ADC) without gain calibration, operating across a temperature range of 4.6–400 K. To ensure the stability of the ringamp, given the large variation of MOSFET transconductance, threshold voltage, and drain resistance across temperature, we propose a unity-gain-frequency-aware bias calibration and a 1st-stage bias-enhancement technique. The unity-gain-frequency-aware bias calibration stabilizes the amplifier bandwidth by biasing the 3rd stage of the ringamp using a constant-*Gm* circuit and then optimizing the overall phase margin by tuning the 1st and 2nd stages based on feedback from an amplifier output settling monitor. An additional bias-enhancement technique alleviates the issue of insufficient voltage headroom at cryogenic temperatures (CTs) in the fully differential first stage of the ringamp. This is achieved by separately ac-coupling the NMOS and PMOS of the 1st-stage inverter. Furthermore, to deal with insufficient gain in advanced CMOS process, a cascode correlated-level-shifting (CLS) technique is proposed. This enables gain-calibration-free operation while achieving higher speed than conventional CLS. A 12-bit 250 MS/s pipelined ADC prototype is fabricated with the proposed ringamp in 65 nm CMOS technology. It achieves a signal to noise and distortion ratio (SNDR) above 57.7 dB across the 4.6–400 K temperature range, and Walden figure-of-merit (FoM) of 154 fJ/conv.-step at 4.6 K while operating without any gain calibrations. To the best of our knowledge, the achieved functional temperature range is the widest ever reported for a pipelined ADC.**

***Index Terms*— 4 K, analog-to-digital (A/D), analog-to-digital conversion, analog-to-digital-converter (ADC), cascode correlated level shifting (CLS), cryo-CMOS, cryogenic, data converter, pipeline, pipelined ADC, ring amplifier, ringamp.**

I. Introduction

AS THE fields of quantum computing, aerospace, and automotive technology continue to evolve, the demand for analog-to-digital-converters (ADCs) that can operate under extreme temperatures continues to increase. In the realm of quantum computing, a topic with significant recent activity, there is a need for ADCs capable of operating at more than 100 MS/s. These ADCs must function at very low temperatures, around 3–4 K, to read out quantum bits (qubits) inside the cryogenic cooler. The ADCs need to be highly energy-efficient because the cryogenic cooler's cooling power is limited [1], [2]. In aerospace applications, the preference leans toward ADCs that can function in a wide temperature range, for example, from 43 to 393 K. This wide-range operation removes the need for area and power-consuming warm boxes [3]. Similarly, automotive applications also demand ADCs that can cope with temperature variations from 233 to 393 K. In such applications, a multitude of ADCs are used for sensing and wireless communication purposes. In the quantum computing use-case, ADCs with an effective number of bits (ENOB) greater than 8-bits are preferred since this enables ADCs to read out a large number of frequency-multiplexed qubit signals. Likewise, such high-resolution ADCs are necessary in the analog front-end for wide-bandwidth wireless communication in aerospace and automotive applications.

Despite advances in technology, existing ADCs capable of functioning across a wide temperature range struggle to fulfill both high speed and high-resolution requirements, as depicted in Fig. 1. Achieving both of these objectives typically involves the use of either time-interleaving (TI) or pipelin-

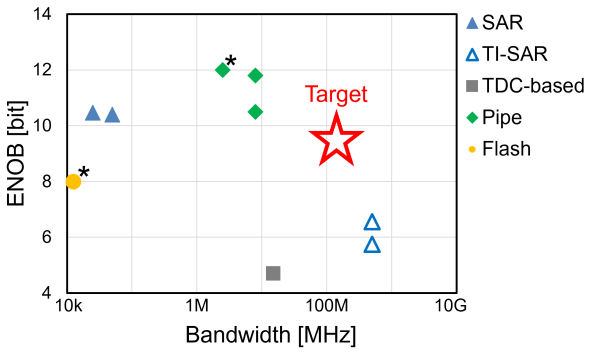

Fig. 1. ENOB versus BW for ADCs with more than 200 K functional temperature range [1], [2], [3], [4], [5], [6], [7], [8], [9]. Those without chip measurement results [10], [11] are excluded. Symbols with * represent resolution instead of ENOB since they do not provide a measured SNDR.

Manuscript received 5 July 2023; revised 1 October 2023; accepted 23 October 2023. Date of publication 9 November 2023; date of current version 27 February 2024. This article was approved by Associate Editor Shaolan Li. This work was supported by the Japan Science and Technology Agency (JST) (Moonshot Research and Devlopment) under Grant JPMJMS2067. *(Corresponding author: Kentaro Yoshioka.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2023.3328385.

Digital Object Identifier 10.1109/JSSC.2023.3328385

ing techniques [12]. TI can overcome the limit imposed by low-speed and high-resolution SAR ADCs, realizing a power-efficient implementation. However, the calibration complexity to correct the TI artifacts (e.g., timing, channel mismatches) grows rapidly as the number of interleaved channels increase. On the other hand, pipelining allows for an increase in the per-channel speed and resolution without a tradeoff between calibration complexity and speed-resolution (often incurring a power tradeoff instead). Consequently, realizing a pipelined ADC operating across an extremely wide operating temperature range not only raises the existing boundary regarding speed and resolution, but also enables further increase in speed of TI.

The main challenge in realizing such a pipelined ADC is the design of the residue amplifier, since it is the most temperature-sensitive component and frequently also the most power hungry. Closed-loop (CL) amplification with a Class-A operational transconductance amplifier (OTA), used in [3], [5] and [6] to achieve operation down to 43 and 77 K, is a promising approach for its robustness arising from negative-feedback and constant current biasing. However, its highly cascoded topology requires a high supply voltage and large power consumption, and it cannot be implemented in scaled CMOS processes.

A variety of amplifier topologies to replace the OTA have been investigated over the years. Notably, open-loop (OL) amplifiers such as *Gm-C* [13] dynamic amplifiers and *Gm-R* [14] amplifiers have attracted attention due to their ability to achieve high speed and low power consumption. However, their accuracy is critically dependent on device parameters such as transconductance and threshold voltage. These parameters are subject to variations across temperatures; they are not suitable for extremely wide-range temperature operation without calibration. Another alternative is the digital amplifier [15], which operates based on successive-approximation-based error correction, allowing the amplifier to exhibit robust performance against process voltage temperature (PVT) variations. However, its serial error correction cycles limit its speed.

Ring amplifier (ringamp) [16] is another OTA alternative that has demonstrated high efficiency, high speed, and high linearity. This CL inverter-based multistage amplifier features a dominant pole at its output stage. As a CL amplifier, provided that its stability is maintained, its final amplification accuracy can be determined by its OL gain and feedback factor. This trait is beneficial in ensuring accurate amplification despite variations in the MOSFET characteristics. However, maintaining the stability of a ringamp across PVT often proves difficult due to its dynamic mechanism of stabilization, which is a function of temperature-dependent parameters such as threshold voltage, output impedance, and device transconductance. Several methods for calibration-free suppression of these parameter variations have been proposed [17], [18], [19], [20], [21], [22], [23], [24], [25], but they lack sufficient degrees of freedom (i.e., tuning knobs) to contain variability across extreme temperature ranges without making unacceptable sacrifices in biasing optimality with regard to bandwidth and power efficiency.

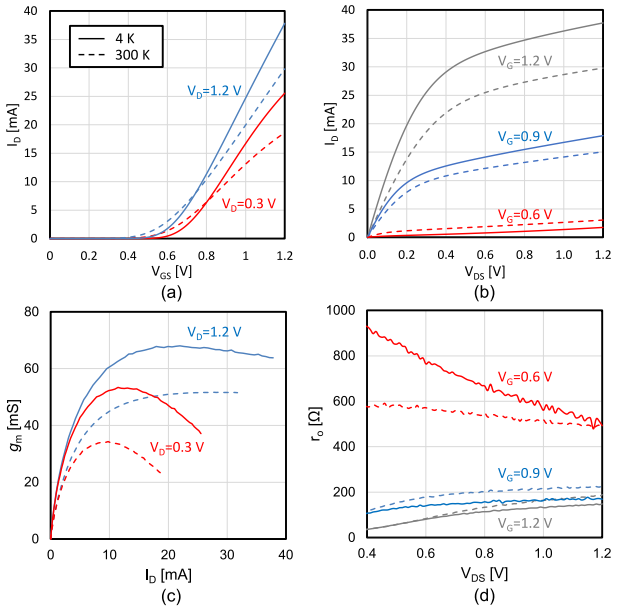

Fig. 2. Measured (a) $I_D - V_{GS}$, (b) $I_D - V_{DS}$, (c) transconductance, and (d) drain resistance of NMOS transistor at 4.2 and 300 K.

To address this, we propose a PVT-robust bias calibration method, named unity-gain-frequency-aware bias calibration, functional from 4.6 to 400 K for a ringamp to realize a 12-bit 250 MS/s pipelined ADC [26]. This calibration method simultaneously stabilizes the ringamp bandwidth and ensures an appropriate phase margin. Furthermore, to deal with the insufficient voltage-margin and intrinsic gain in advanced CMOS technology, we propose a bias-enhancement technique in the first stage of the ringamp and a separate cascode correlated-level-shifting (CLS) technique at the output of the ringamp. This article is constructed as follows. Section II analyzes the operation of the ringamp at extreme temperatures. Based on that analysis, Section III describes the concept of unity-gain-frequency-aware bias calibration. Section IV discusses the circuit-level implementation of the unity-gain-frequency-aware bias calibration and details of the bias-enhancement and cascode-CLS techniques. Section V discloses the implementation of the prototype ADC, and measurement results are reported in Section VI. Finally, Section VII concludes this article.

II. Analysis of Ringamp Operation Under Extreme Temperatures

To initiate the discussion, we first investigate the variation of a MOSFET across temperature and its consequent influence on the operation of a ringamp. Given that the most significant characteristic variation from room temperature (RT) is expected at cryogenic temperature (CT) within our target temperature range, and typical PDKs do not provide accurate device models at CT, we focus on measured CT characteristics of the MOSFET. Fig. 2 shows measured

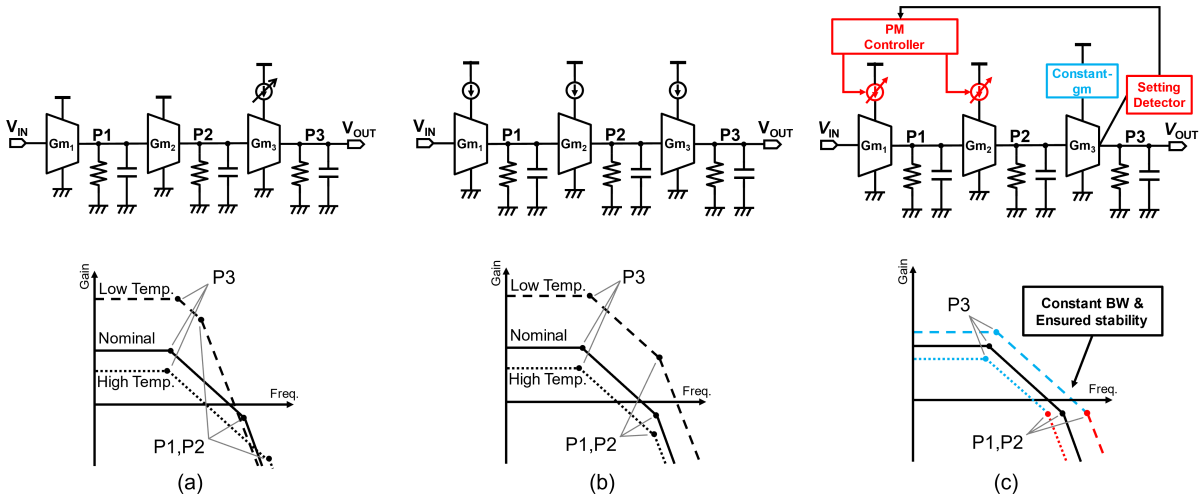

Fig. 3. Small-signal model and frequency response variation across temperature of (a) conventional high-speed ringamp (frequency response assumes that 3rd stage is biased with constant current), (b) prior PVT-robust ringamp [22], and (c) proposed ringamp.

characteristics of an NMOS transistor in a 65 nm CMOS process at 4.2 and 300 K.[1] When going from 300 K down to 4 K, we observe a 1.3 to 2.0 times increase in transconductance, more than 100 mV increase in threshold voltage, and a 0.6 to 0.9 times increase in output resistance for the same drain current.

Such variations at CT can lead to stability issues in conventional ringamps. Fig. 3(a) shows a small-signal model and frequency response of a commonly used topology that only controls the "deadzone voltage" biasing of the 3rd stage, which has the effect of tuning the 3rd stage bias current. Venkatachala et al. [17] and Xavier et al. [18] control the deadzone voltage such that the 3rd stage bias current remains constant by utilizing a replica ringamp, thereby enhancing PVT robustness. However, when the amplifier operates at CT, since the 1st and 2nd stages are not controlled, their bias current decreases in response to the increase in the threshold voltage, leading to a lowering of the 1st and 2nd stage pole frequencies ($P1$ and $P2$). Given that the ringamp is stabilized by placing $P1$ and $P2$ at a sufficiently higher frequency than the unity-gain frequency (ω_{unity}) dominated by $P3$, reduction of $P1$ and $P2$ results in reduced damping and possibly even instability. This problem is further compounded by the increase in mobility at CT and its effect on the large signal behavior of the ringamp. During the initial slewing phase of the ringamp's operation, it biases its 3rd stage with almost rail-to-rail voltage swing resulting in highly dynamic and non-linear behavior. This slewing behavior is affected by the mobility increase at CT, and if $P1$ and $P2$ cannot track with the increased slewing rate, instability can occur. Even if there is a bias point where small-signal stability is possible, it is still possible that the large-signal transient behavior of the ringamp will be such that it never manages to lock into this bias point (see Fig. 4 of [27]). Meanwhile, on the other side of the temperature range, at high temperatures, if $P1$ and $P2$ are unconstrained, they will shift to a relatively higher frequency, resulting in an unnecessarily large phase margin and a non-optimal power/performance tradeoff.

For better PVT robustness, Zhan et al. [22] biases all three stages with a constant current source, as shown in Fig. 3(b). As a result, $P1$, $P2$, and $P3$ are kept relatively stable across temperatures. However, this topology still cannot maintain stability across an extreme temperature range of 4–400 K without incurring an unattractive power/performance penalty in the form of extra design safety margin, due to large variation of ω_{unity}. Furthermore, at CT, the large-signal slewing speed variability problem described above also degrades stability. Therefore, to realize a ringamp operating stably across a wide temperature range from 4.6 to 400 K, the proper amount of bias currents that maintain constant ω_{unity} and stability needs to be actively searched, rather than simply enforcing constant bias currents.

III. Unity-Gain-Frequency-Aware Bias Calibration

To ensure the stability of the ringamp across a wide temperature range, we introduce a new bias calibration technique named unity-gain-frequency-aware bias calibration. As shown in Fig. 3(c), with this bias calibration, the bandwidth, i.e., the speed of the ringamp, is kept stable across temperature, and not only small-signal, but also large-signal stability is ensured while preserving high power efficiency.

As illustrated in Fig. 4, the calibration procedure is divided into two steps.

1) Minimize the bandwidth deviation across temperature by controlling the 3rd stage dominant pole, $P3$, with a constant-Gm circuit.
2) Then, optimize the phase margin by controlling the non-dominant 1st and 2nd stage poles, $P1$ and $P2$, based on information about the amount of amplifier settling error.

The details of these two steps are provided in Sections III-A and III-B. In addition, in order to control the ringamp to have $P1$, $P2$, and $P3$ at the intended frequency, the replica ringamp,

[1]This characterization measurement was obtained with a different 65 nm process than the one used for our ADC prototype, and is thus expected to exhibit similar yet slightly different characteristic curves.

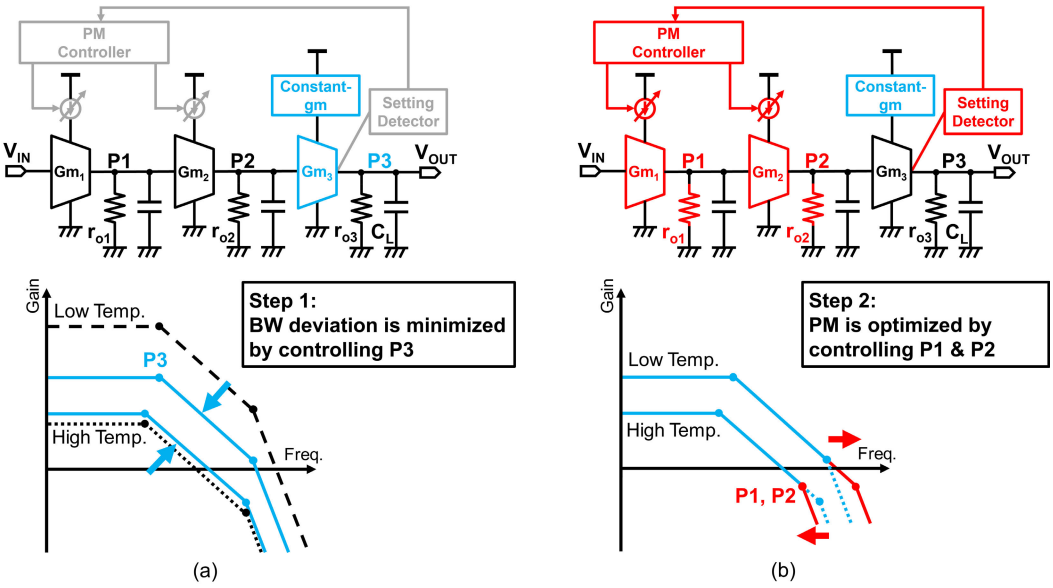

Fig. 4. Two-step operation of unity-gain-frequency-aware bias calibration. (a) Biasing the 3rd stage with a constant-Gm circuit minimizes variation of the amplifier bandwidth across temperature. (b) After the bandwidth is set, phase margin is optimized by controlling $P1$ and $P2$ based on information about the amount of amplifier settling error.

detailed in Section III-C, is utilized. The full calibration procedure is described in Section III-D.

A. Constant Bandwidth With Constant-Gm Circuit

The first step of the calibration minimizes the variation of ω_{unity} across temperature. To achieve this, a constant-Gm circuit [28], shown in 5(a), is used to control the 3rd stage transconductance (Gm_3), which has the largest contribution to ω_{unity}.

Neglecting the finite output resistance, the constant-Gm circuit enforces the transconductance of the transistor operating in a strong-inversion region to be

$$Gm = \frac{1}{R_{\text{ref}}} \tag{1}$$

regardless of MOSFET characteristic variation. R_{ref} is a reference poly-resistor, which is stable (<20% variation at 4 K according to our measurement. van Dijk et al. [29] confirms this result.) across temperature. Assuming $P3 \ll P1$ and $P2$, ω_{unity} of the ringamp can be approximated as

$$\omega_{\text{unity}} \approx \frac{Gm_1 r_{o1} Gm_2 r_{o2} Gm_3}{C_{\text{L}}} \tag{2}$$

where Gm_i and r_{oi} are transconductance and output resistance of ith stage, respectively ($i = 1, 2, 3$). If the 3rd stage of the ringamp is biased with a constant-Gm circuit, the variation of ω_{unity} compared to nominal condition can be written as

$$\frac{\omega_{\text{unity}}}{\omega_{\text{unity,nom}}} = \frac{Gm_1 r_{o1} Gm_2 r_{o2}}{Gm_{1,\text{nom}} r_{o1,\text{nom}} Gm_{2,\text{nom}} r_{o2,\text{nom}}}. \tag{3}$$

Gm_i and r_{oi} have complementary temperature coefficients, as depicted in Fig. 2. Therefore, assuming the 1st and 2nd stages are biased with constant current, the variation in Gm_i and r_{oi} is counteracted by each other, and ω_{unity} is kept relatively constant.

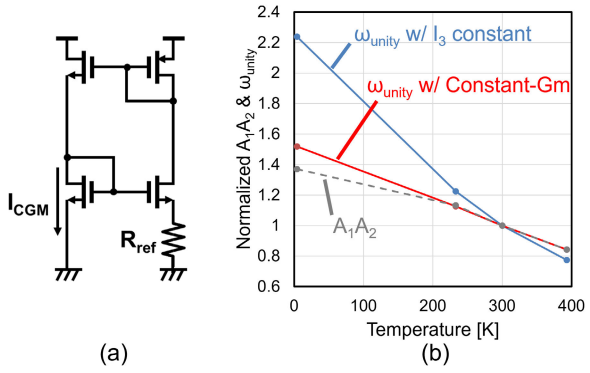

Fig. 5. (a) Constant-Gm circuit and (b) simulation results of the ringamp unity-gain frequency, and first- and second-stage gain. For simulation at 4 K, a custom cryogenic model was used.

The above theory is confirmed via simulation with a custom cryogenic device model.[2] Fig. 5 summarizes the simulated ω_{unity}, and 1st and 2nd stage gain, A_1A_2, with the 3rd stage biased with constant current or constant-Gm circuit, respectively. We keep the 1st and 2nd stage currents constant in this simulation. When the 3rd stage is biased with a constant current, ω_{unity} increases by more than twofolds at 4 K, when compared to 300 K. On the contrary, when the 3rd stage is biased with a constant-Gm circuit, ω_{unity} variation is greatly reduced to $\times 1.5$, which is actually almost equivalent to the increase observed in A_1A_2. While ω_{unity} is not completely flat across temperatures, its variation is effectively mitigated by the output resistance variation, which leads to a proportional variation of $P1$ and $P2$ to ω_{unity}. This serves to maintain the stability of the ringamp despite the changing conditions. Furthermore, the remaining deviations are further adjusted

[2]This model is created utilizing the measurement results shown in Section II.

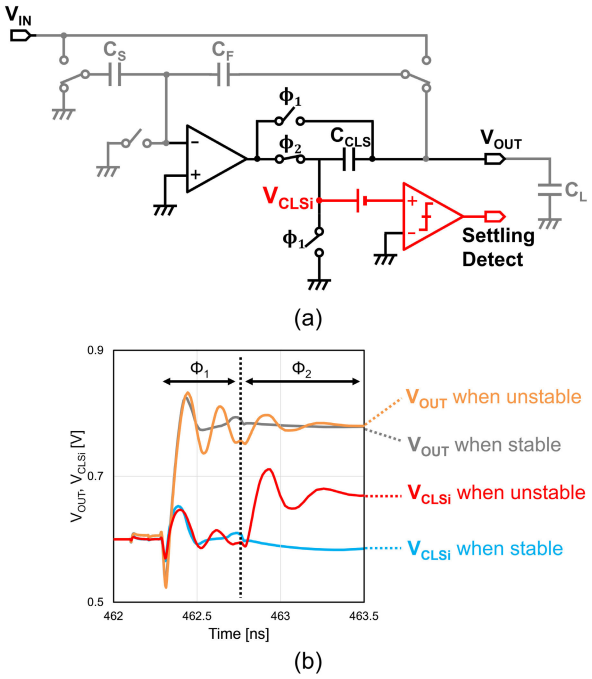

Fig. 6. (a) Settling detector. (b) Waveforms of V_{OUT} and V_{CLSi}.

during the second step of the unity-gain-frequency-aware bias calibration as described in Section III-B.

B. Optimal Phase Margin With Settling Detector

The second step of the unity-gain-frequency-aware bias calibration is to control $P1$ and $P2$ to create an optimal phase margin. This is necessary to ensure the amplifier's small and large-signal stability across different operating conditions. To achieve this, we *directly* monitor the output settling of the ringamp utilizing a settling detector shown in Fig. 6. Here, the term "optimal phase margin" refers to the condition where the transient settling error at the end of the amplification phase is minimized with minimal power consumption, indicating a critically damped condition. If the ringamp has an insufficient phase margin, then poor stability will introduce excess "ringing" errors. If the ringamp has a large phase margin, it becomes stable, but large power is required to put $P1$ and $P2$ at higher frequency than necessary. Therefore, the optimal phase margin condition is the point where the ringing-induced error disappears, that is, the boundary between a stable and unstable operation, and is identified by sweeping $P1$ and $P2$ from low frequency (under-damped condition) and stopping the sweep when the settling error is minimized. In our calibration, the settling detector is used to monitor the settling error; in this way, both large-signal and small-signal stability of the ringamp can be ensured.

To extract the information of the settling error, we exploit a specific feature of CLS [30], which enables an implementation with minimal overhead. A deeper discussion of the CLS scheme is provided later in Section IV-B, but the important aspects for this discussion are shown in Fig. 6. CLS is a two-step amplification technique where the second amplification phase (ϕ_2) compensates for the error voltage of

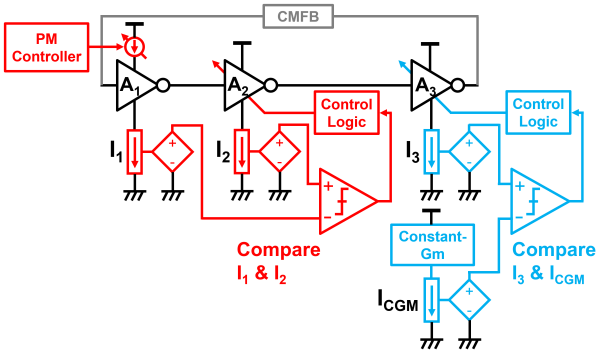

Fig. 7. Simplified model of the replica ringamp.

the first amplification phase (ϕ_1). The key insight is that the voltage amplitude seen at the output of the ringamp during the second phase is a function of the amount of settling error seen in the first phase. Through this, we can monitor the stability based on the amplifier output voltage (V_{CLSi}) during ϕ_2 as shown in Fig. 6(b). A smaller swing suggests stable operation, where only gain-induced errors need to be corrected by the amplifier in ϕ_2. A larger V_{CLSi} swing indicates instability, since it implies that the amplifier, coupled to the output through C_{CLS}, is compensating for some additional source of error encountered in ϕ_1. The size of C_{CLS} also scales the size of the amplifier output swing in ϕ_2, but is constant and set at design time. In this design, C_{CLS} is chosen such that the output swing of the amplifier in ϕ_2 is tens of millivolts when the ringamp is optimally biased, providing a relatively large amplitude that can easily be measured by a monitor circuit.

We implement the settling detector by quantizing V_{CLSi} with a single comparator with a built-in offset voltage. The larger the average error amplitude at the end of ϕ_2, the more often the comparator will trigger. Thus, the average value of the comparator output can be utilized to estimate the settling error. In addition, PVT-induced small variation of the offset voltage does not affect the calibration result because the calibration process searches for the global minimum value of the settling error and does not care its actual value. While CLS-based settling detection is utilized in our design, note that other monitoring approaches, for example, stochastic ADCs [31], [32], can also be applied.

C. Replica Ringamp

Although we have established methods for determining the optimal bias currents to place all poles ($P1$–$P3$) at their desired frequencies, there is still the question of control complexity. To minimize control complexity, the values of $P1$–$P3$ should all be dependent parameters of the constant-Gm reference. To do this, we must know the relative ratios of branch currents I_1:I_2 and I_3:I_{CGM}. This information cannot be easily extracted due to the lack of constant-current class-A-style biasing in the ringamp. For example, in the implemented prototype ADC, the bias current of the 2nd and 3rd stages of the ringamp is controlled with anti-parallel CMOS (AP-CMOS) resistors [33], [34], as shown in Fig. 9. The resistor-bias-to-branch-current conversion factor is highly non-linear and not easily extracted. It may be possible to obtain the branch

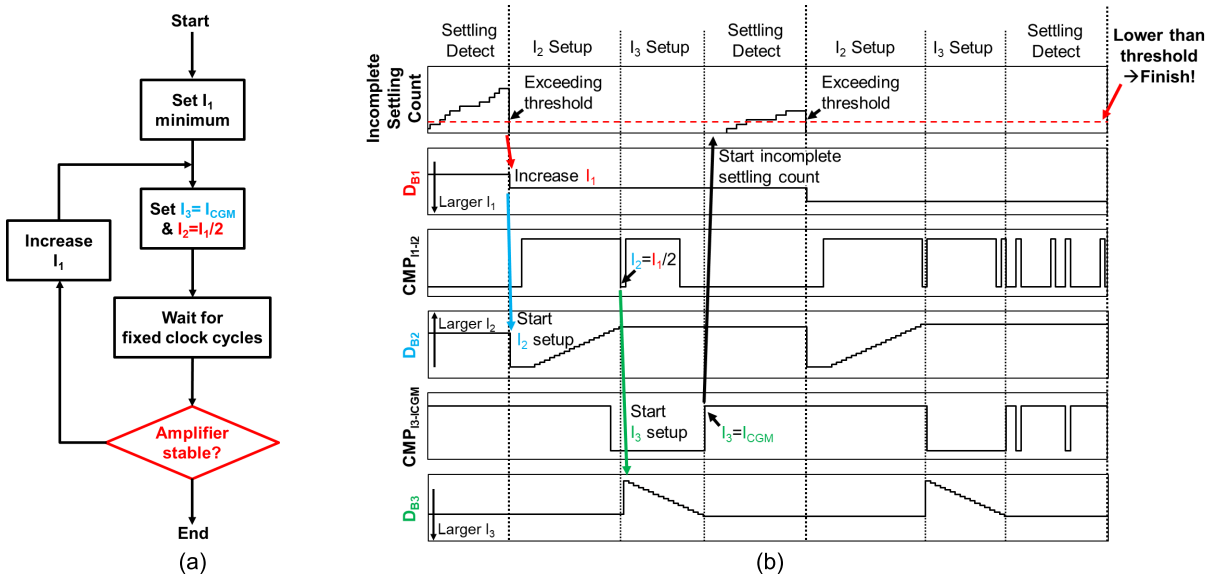

Fig. 8. (a) Flowchart and (b) simulated convergence procedure of unity-gain-frequency-aware bias calibration.

currents with current-mirror read-outs, but this would involve adding extra loading onto the critical, frequency-sensitive internal nodes of the ringamp, incurring performance and efficiency losses.

To bypass these constraints and still minimize control complexity, we introduce the use of a replica ringamp instead. This replica, identical in transistor sizing to the main ringamp in the signal path, helps find the bias voltages that set the ringamp's desired branch currents. Because the replica is outside the signal path and effectively a dc circuit, loading introduced by the components used to monitor the bias currents does not compromise the ADC performance. The simplified model of the replica ringamp is shown in Fig. 7. It has two current comparators, one that compares the 1st and 2nd stage currents (I_1 and I_2) and the other that compares the 3rd stage current (I_3) against the current through the constant-Gm circuit (I_{CGM}). With these current comparators, we can digitally search for the bias voltages that set the currents I_3, I_2, and I_1 appropriately. This process enables us to achieve a constant bandwidth (Gm_3) and track $P2$ and $P1$, intending to enforce the condition where $\omega_{P2} = \omega_{P1}$.

An unavoidable limitation on a use of the replica is a mismatch. Since the 3rd stage of the ringamp uses relatively small-sized transistors, there can be I_3 mismatches between the main and the replica ringamp and between the ringamps sharing the same bias codes. Such mismatches are tolerated by $P1$ and $P2$ calibration with the settling detector. However, if not all of the ringamps sharing the bias codes have the settling detector, ringamps without the settling detector can go into instability, which is undetectable. To mitigate this issue, in this work, the ringamps are designed to have slightly smaller ω_{unity} during ϕ_2 of CLS than during ϕ_1. This enables the ringamp to settle within a tolerable error range during ϕ_2 even if increased I_3 due to mismatch makes it unstable during ϕ_1.

D. Calibration Procedure

The entire bias calibration procedure is summarized in Fig. 8. Initially, I_1 is set to its minimum value. Subsequently, the replica ringamp and its current comparators are utilized to ascertain the bias codes that enforce $I_3 = I_{\mathrm{CGM}}$ and $I_2 = I_1/2$. The condition, $I_2 = I_1/2$, is where the ringamp is designed to have ω_{P2} close to ω_{P1}. This consequently positions the 1st and 2nd stage poles at their lowest frequencies also, while maintaining a constant ω_{unity}. Then, we check for incomplete settling via the settling detector by measuring the average value of the settling detector comparator over many cycles. If this value is below a certain threshold, the calibration is deemed complete. Otherwise, we increase I_1, shifting $P1$ and $P2$ to a higher frequency, and repeat the calibration procedure from the second step.

IV. Ringamp Circuit Implementation

In this section, the circuit-level implementation of the ringamp is described, with the proposed unity-gain-frequency-aware bias calibration included. Furthermore, we will also discuss two additional techniques: bias-enhancement technique and cascode CLS, explained in greater detail in Section IV-A and IV-B.

Fig. 9 shows the schematic of the implemented main ringamp and the replica ringamp. We adopt the fully differential architecture [31] due to the ease it provides in controlling I_1 with a tail current source, alongside offering robust common-mode feedback (CMFB). Both I_2 and I_3 are controlled by AP-CMOS resistors with variable bias voltages. These bias voltages, when adjusted, alter the voltage drop across the resistor, thus influencing the overdrive voltage and the bias current of the next stage. The relative ratio of currents I_1:I_2 is determined by the ratio of current-mirror transistor sizes in the I_1 and I_2 comparator. To enhance the

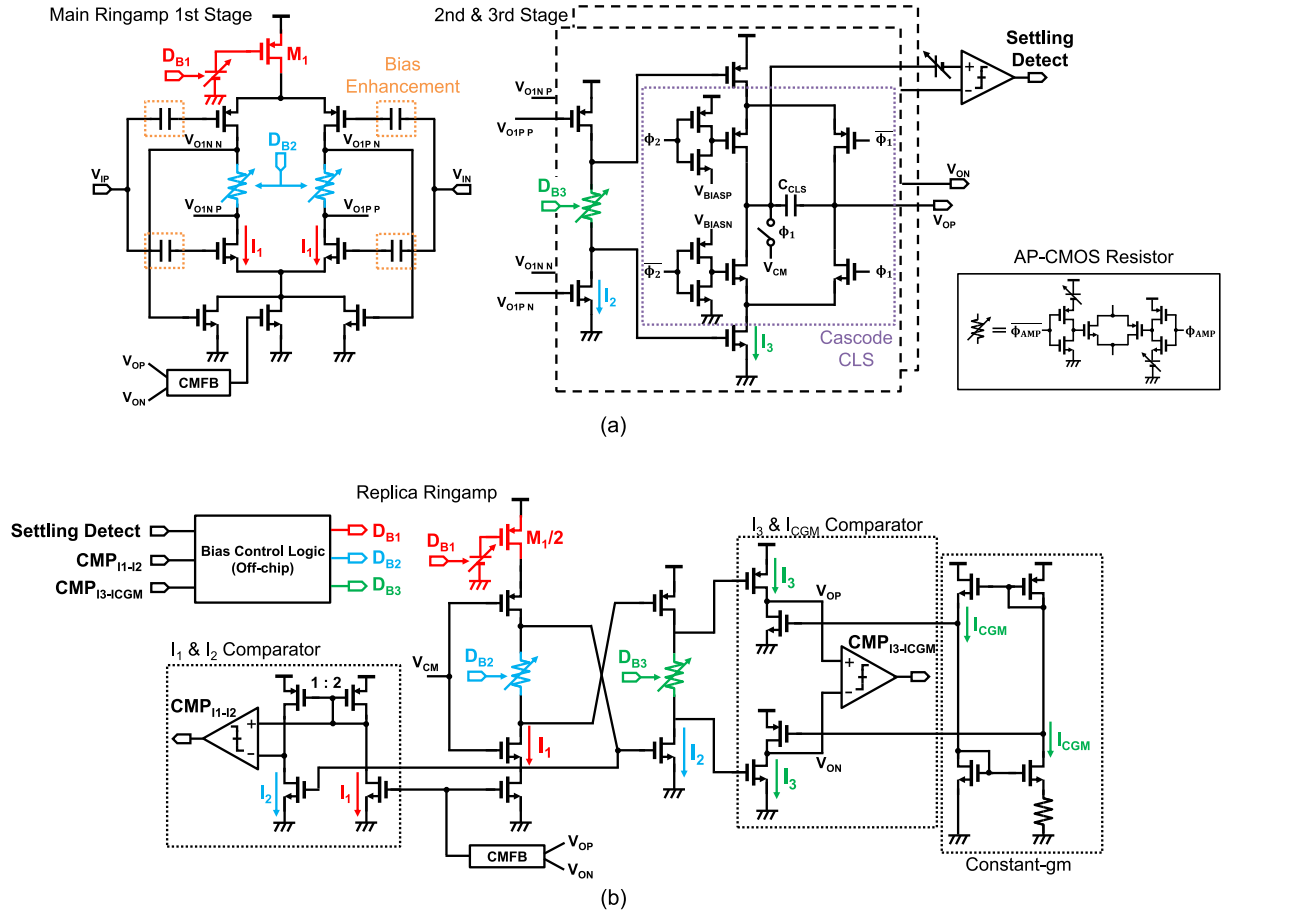

Fig. 9. Implementation of the ringamp with the unity-gain-frequency-aware bias calibration, bias-enhancement technique, and cascode-CLS technique. (a) Main ringamp. (b) Replica ringamp and bias calibration logic.

settling, the bias-enhancement scheme of [33] is used, whereby the 2nd stage PMOS and NMOS gates are cross-connected to the lower and upper side of the stage 1 AP-CMOS resistor, respectively. This enables to keep sufficient amount of I_2 even when threshold voltage increases, at the cost of larger power consumption in a lower threshold voltage corner. The bias voltages for the AP-CMOS resistors are generated with trapped-charge bias control, and trapped-charge CMFB is adopted for CMFB [31]. To save energy, both the main and replica ringamp are turned off when inactive by resetting the gates of NMOS/PMOS of the AP-CMOS resistors to V_{SS}/V_{DD}.

A. Bias-Enhancement Technique

The fully differential architecture of the ringamp is beneficial in terms of easy control over 1st stage current and robust CMFB with a simple circuit. Nonetheless, the 1st stage comprises four stacked transistors and suffers from severe voltage headroom issues at CT where the threshold voltage is >100 mV higher than at RT. Without any intervention, tail current source and CMFB transistors are forced to operate in a linear region, which results in insufficient current and improper common-mode voltage.

In order to solve this issue, we propose applying distinct offset voltages to input NMOS and PMOS transistors through separate ac-coupling capacitors (C_{OSP}, C_{OSN}).[3] As shown in Fig. 10, this configuration ensures that the gate voltage of the NMOS transistor is higher than common-mode voltage (V_{CM}) and vice versa for PMOS. The applied offset voltage (V_{OS}) requires careful consideration, such that input pairs operate in saturation region even with the voltage drop across AP-CMOS resistors, and that the tail CMFB transistors have enough gain. In this design, $V_{OS} = 100$ mV is used.

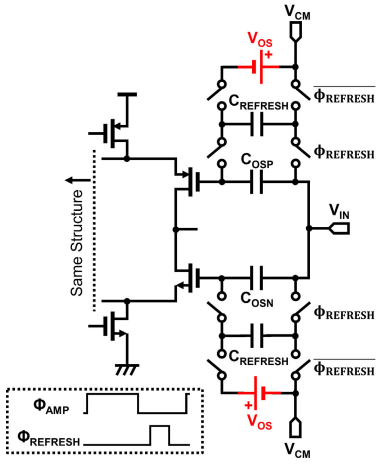

Fig. 10. Simplified fully differential first stage with bias-enhancement technique.

[3]A similar approach reported in [23] was independently proposed.

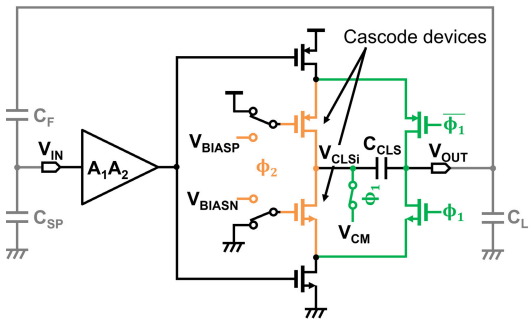

Fig. 11. Simplified ringamp with cascode-CLS technique.

During the time when the amplifier is deactivated (i.e., when ϕ_{AMP} is low), the capacitors are refreshed. The SHA-less first stage of the pipeline sees a continuous fast-moving input signal, and an attenuated version of it also appears at the input of the ringamp due to the IR drop across the bottom-plate sampling switches in the MDAC. To prevent this signal-dependent information from being sampled onto the bias-enhancement ac-coupling capacitors, their offset voltage is programed via charge transfer with a relatively small refresh capacitor C_{REFRESH} [34]. By limiting the total charge that can transfer on any given cycle, this introduces a low-pass filter that helps to attenuate any coupling from the fast-moving input.

B. Cascode CLS

With advanced CMOS processes, it can be difficult to provide sufficiently large gain even with the three-stage amplification of the ringamp. For example, a ringamp designed with minimum gate length (60 nm) transistors in the 65 nm process of this design offers a gain of only 40 dB. Therefore, CLS is often used since it can ideally square the gain with two-time amplification [30] and has been applied to ringamps in a multitude of ways [16], [19], [20], [21]. However, the multistep operation of classical CLS degrades speed, and the squared gain is sometimes still not sufficient.

To overcome these issues, we propose a cascode-CLS technique which provides additional gain (A_{ADD}) without performance overhead. As shown in Fig. 11, this technique replaces the switches for the 2nd CLS amplification with cascode devices, biasing them to operate in the saturation region. Since the internal node of CLS (V_{CLSi}) always hovers around the common-mode voltage (V_{CM}), independent of the output voltage V_{OUT}, cascode transistors do not limit the rail-to-rail swing of V_{OUT}, which is an advantage over [35]. In our prototype ADC, to maximize A_{ADD}, we use cascode devices with long channel-lengths ($L = 200$ nm, $W = 1.6$ μm), achieving A_{ADD} of 25 dB.

Fig. 12 shows the operation of the cascode-CLS technique. During the 1st amplification phase (ϕ_1), the ringamp almost fully charges its load capacitance through low ON-resistance switches, providing fast slewing. Then, during the 2nd amplification phase (ϕ_2), the ringamp compensates for the error voltage of the 1st amplification with large gain provided by the cascode devices. Since this error voltage is small, for which

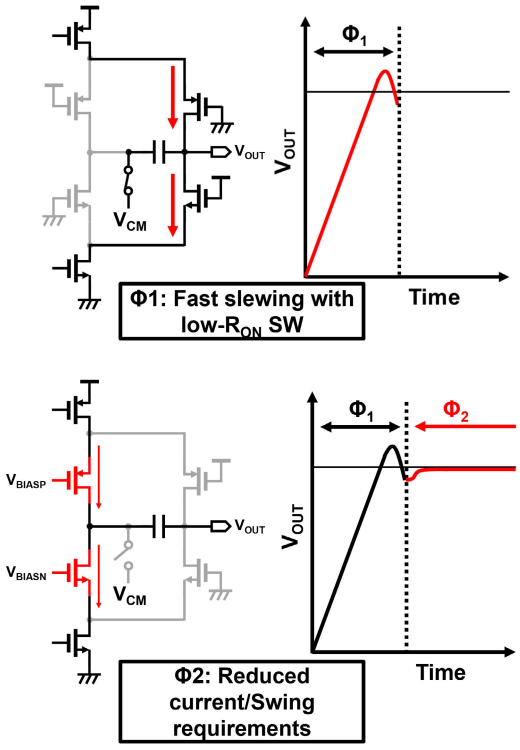

Fig. 12. Operation of cascode CLS.

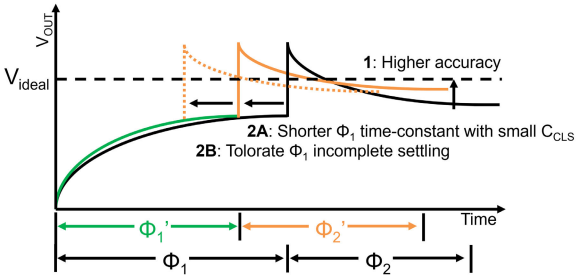

Fig. 13. Three ways to use A_{ADD}, assuming first-order settling of the amplifier.

only a small amount of charge is required to compensate, the static biasing and higher output resistance of the cascode devices do not degrade amplification speed. The additional gain can be used for: 1) higher accuracy and/or 2) shorter amplification time, as shown in Fig. 13, or some combination of both.[4]

1) Higher Accuracy: Additional accuracy can be achieved by simply introducing cascode devices to CLS without changing other parameters, that is, the size of the level-shifting capacitor (C_{CLS}) and amplification time. In this case, compared with CLS, the equivalent loop gain increases by A_{ADD} and is

[4]In the context of other CLS techniques, cascode CLS can be understood as a special case of split-CLS [36]. It capitalizes on the same key insight that the output swing and slewing requirements are relaxed in phase 2 relative to phase 1. Cascode CLS captures all of the benefits of split-CLS and adds the benefit of hardware reuse, re-configuring the phase 1 wide-swing coarse amplifier into a narrow-swing high-gain amplifier in phase 2.

calculated as

$$A_{\mathrm{EQ,Cascode}} = \frac{A_{\mathrm{ADD}} A^2}{1+\lambda}. \tag{4}$$

A is the loop ringamp gain without A_{ADD}, and λ is the effect of finite C_{CLS} [30], which can be expressed as

$$\lambda = \frac{1}{C_{\mathrm{CLS}}}\left(C_{\mathrm{F}} + C_{\mathrm{L}} - \frac{C_{\mathrm{F}}^2}{C_{\mathrm{F}} + C_{\mathrm{SP}}}\right) \tag{5}$$

where C_{F} is the feedback capacitance, C_{L} is the load capacitance, and C_{SP} is the sum of capacitance at the input node (V_{IN}).

2) Shorter Amplification Time: Alternatively, a shorter amplification time can be achieved by using A_{ADD} A) to reduce the size of C_{CLS} and/or B) to tolerate incomplete settling of the 1st amplification. If A_{ADD} is used entirely to reduce C_{CLS}, it can be calculated as

$$C'_{\mathrm{CLS}} = \frac{\lambda}{(1+\lambda)A_{\mathrm{ADD}} - 1} C_{\mathrm{CLS}} \simeq \frac{\lambda}{1+\lambda}\frac{1}{A_{\mathrm{ADD}}} C_{\mathrm{CLS}}. \tag{6}$$

This indicates that C_{CLS} can be reduced by the factor of A_{ADD}, contributing to a smaller area and a shorter time period of ϕ_1 without power overhead.[5] Assuming first-order settling of the amplifier, the reduced time of ϕ_1 can be expressed as

$$\phi'_1 = \frac{C_{\mathrm{tot}} + \frac{\lambda}{1+\lambda}\frac{1}{A_{\mathrm{ADD}}} C_{\mathrm{CLS}}}{C_{\mathrm{tot}} + C_{\mathrm{CLS}}}\phi_1 \simeq \frac{C_{\mathrm{tot}}}{C_{\mathrm{tot}} + C_{\mathrm{CLS}}}\phi_1 \tag{7}$$

where C_{tot} is the total capacitance at the output node that can be expressed as

$$C_{\mathrm{tot}} = C_{\mathrm{L}} + \frac{C_{\mathrm{F}} C_{\mathrm{SP}}}{C_{\mathrm{F}} + C_{\mathrm{SP}}}. \tag{8}$$

The time required for ϕ_2 does not change because the loop ω_{unity} during ϕ_2 is not affected by the size of C_{CLS}.

The time spent on ϕ_1 can also be reduced by utilizing A_{ADD} to tolerate incomplete settling of ϕ_1. For example, if the amplifier needs to finally settle within ± 125 μV($\approx$ 1/8 LSB) of the ideal output voltage (V_{ideal}), assuming a feedback factor of 1/2, $A = 34$ dB, and $\lambda = 1.5$, the amplifier with CLS needs to settle within ± 3 mV of V_{ideal} during ϕ_1. On the other hand, assuming $A_{\mathrm{ADD}} = 25$ dB, the amplifier with cascode CLS only needs to settle within approximately ± 50 mV of V_{ideal}. In the case of the ringamp, this allows it to halt ϕ_1 soon after the slewing finishes, as illustrated in Fig. 12.

Fig. 14 shows the simulated SFDR for a sweep of ϕ_1 time period from 0.2 to 0.8 ns. The ringamp with cascode CLS consistently achieves higher SFDR than the one with ordinary CLS, even with short ϕ_1. The prototype ADC uses A_{ADD} to achieve higher accuracy and to tolerate the incomplete setting of ϕ_1, utilizing ϕ_1 time period of 620 ps. To avoid affecting the result of the settling detector shown in Section III, the period of ϕ_1 is made tunable and configured prior to bias calibration.

[5]Note that as the chosen value of C_{CLS} is decreased, the resulting swing of V_{CLSi} will increase, and at some point this tradeoff will push the cascode output devices in ϕ_2 into their linear region. Therefore, careful simulation is needed to determine the practical extent to which this feature can be exploited.

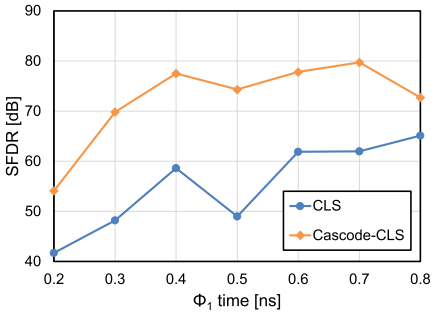

Fig. 14. Simulated SFDR of the ringamp with cascode CLS and CLS.

V. ADC Implementation

A 250 MS/s, 1.5-bit/stage, 12-bit pipelined ADC is implemented to demonstrate the effectiveness of the proposed techniques. Fig. 15 shows the top-level architecture. The ADC adopts a SHA-less architecture and is composed of ten 1.5-bit multiplier-DAC (MDAC) stages; one 2-bit flash backend stage with dummy loading; a global clock buffer/generator; and a digital logic for timing alignment, decimation, and serialization. The first three stages have dedicated replica ringamps, and the digital bias control codes of their ringamps are independently calibrated, while the rest of the stages reuses the bias codes of 3rd stage and contains no replica. Fig. 16 shows the ringamp-based MDAC stage. Boot-strapped switches [37] are heavily used to deal with high ON-resistance of CMOS pass-gate at low temperatures due to increased threshold voltage. The 1st MDAC stage uses the unit capacitance (C_{U}) of 200 fF, which is chosen based on kT/C noise consideration. To enhance power efficiency, it is progressively scaled down by a factor of 2 up to and including stage 3.

VI. Measurement Results

The prototype ADC is fabricated in a single poly nine metal (1P9M) 65 nm CMOS process. As shown in the chip micrograph Fig. 17, the ADC occupies 0.484 mm^2. All the necessary supply and reference voltages, except for the ringamp bias voltages, are generated off-chip. The ADC is measured at 4.6, 87, 300, and 400 K. For measurements at 4.6 and 87 K, a cryostat and liquid helium are used [26]. The 87 K measurements, conducted during the cool down phase, may not have accurate precise temperature values. At 4.6 and 87 K, the ADC core voltage is increased to 1.3 V to compensate for the voltage drop in the cryostat. All digital codes unrelated to the proposed calibration scheme, included for purposes of test and prototyping, are kept constant throughout the measurement, except for the tunable delay parameter affecting the ϕ_1 time period, which is re-tuned at 4.6 and 87 K to compensate for variation of the time delay cells.

Fig. 18(a) shows the measured signal to noise and distortion ratio (SNDR) across temperature with near Nyquist frequency (125 MHz) input. When the proposed unity-gain-frequency-aware bias calibration is executed at each temperature, the SNDR remains above 57.7 dB from 4.6 to 400 K. On the other hand, we see a significant drop at CT when the bias calibration is disabled and the same bias codes as those at 300 K are used.

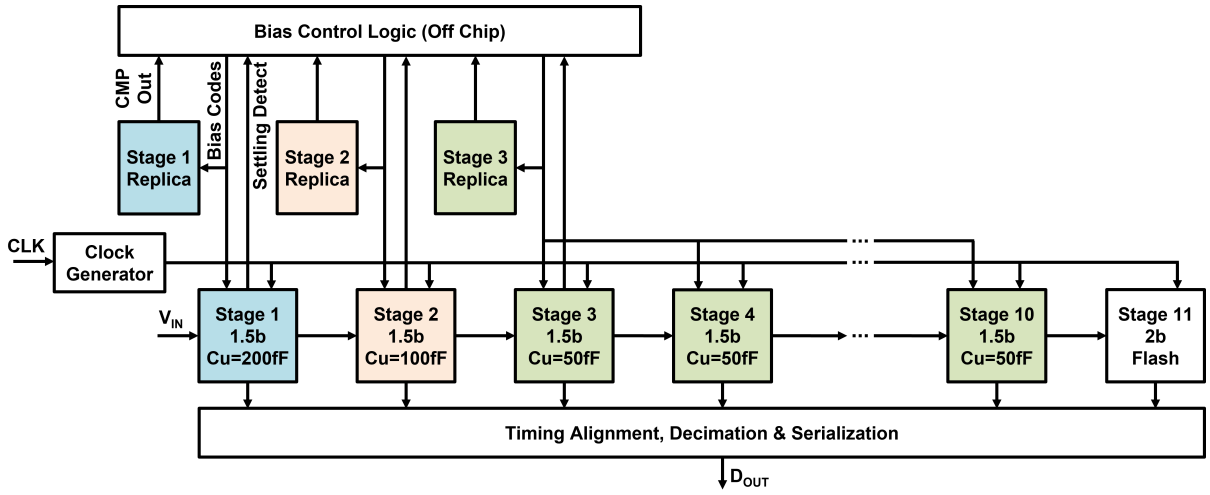

Fig. 15. ADC top-level architecture.

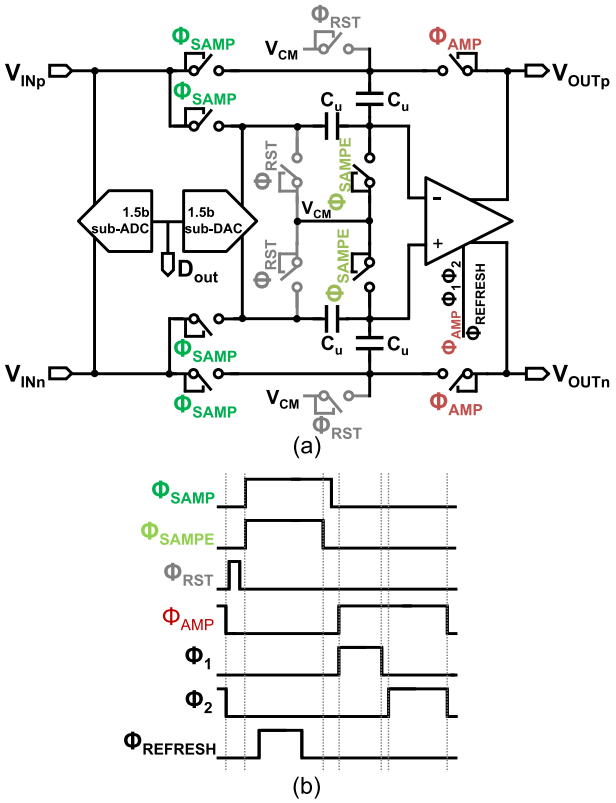

Fig. 16. (a) MDAC gain stage and (b) timing diagram. ϕ_{RST} is only implemented in the 1st stage.

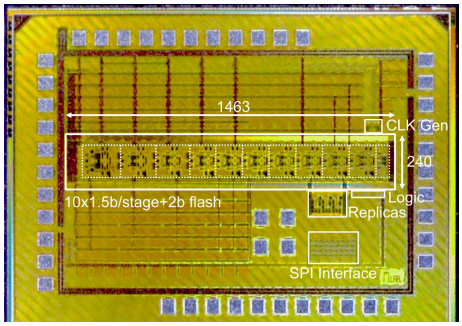

Fig. 17. Chip-micrograph.

Fig. 18(b) exhibits the measured SNDR across 250 mV ADC core supply voltage variation with a low frequency (2 MHz) input. The bias calibration was executed at each measurement point, and the results from four chips showed constant SNDR higher than 58.7 dB. These results confirm the robustness of the ringamp with the proposed bias calibration method against temperature and supply voltage variations.

Fig. 19 shows the number of times the settling detector detects incomplete settling (incomplete settling count), SNDR, and SFDR across the bias code for the ringamp 1st stage tail current source. A large bias code corresponds to a smaller 1st stage current. We can see that the lower count of incomplete settling coincides with higher the SNDR and SFDR, indicating that the settling detector can find the optimal phase margin. The smaller SNDR and SFDR measured with a large bias code (small current) can be attributed to instability caused by insufficient phase margin. On the other hand, SNDR and SFDR also fall with smaller bias codes (large current), which is likely due to the combination of decreased gain, slowed slewing, and inaccurate CMFB.

Fig. 20 shows the FFT spectrum with a near-Nyquist frequency input tone. Due to the narrow bandwidth of the connection between the inside and outside of the cryostat, only a relatively small number of 4096 points could be captured, with a large decimation factor (12.5 k). SNDR/SFDR of 57.9/66.1, 59.0/64.6, and 57.8/62.0 dB is measured at 4.6, 300, and 400 K, respectively. Although, theoretically, the SNR should increase as the temperature decreases, due to the reduced thermal noise, the measured SNR actually declined at 4.6 K. We assume this is attributed to the increase in the reference noise. At 4.6 K, multi-layer ceramic capacitors with a high dielectric constant, which are used as a bypass capacitor for reference voltages, experience a loss of capacitance [38]. Consequently, their filtering capability is compromised, leading to an increase in the reference noise and SNR degradation. The increased spurious at 4.6 K is expected to be a result of

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART EXTREME TEMPERATURE ADCS

	This work			[2] Kiene, ESSCIRC 2022		[1] Kiene, ISSCC 2021		[8] Okcan, RSI 2010		[34] Lagos, JSSC 2019
Temperature [K]	4.6	300	400	4.2	300	4.2	300	4.4	300	300
Technology [nm]	65			40		40		350		28
Architecture	Pipelined			SAR		SAR		SAR		Pipelined
Sampling rate [MS/s]	250			1000		1000	900	0.05		600
Resolution [bit]	12			7		6-8		12		12
Supplies [V]	1.3[1](core), 1.2[1](others)	1.2		1.1		1.1(core), 2.5(clock)		3.3		0.9
Input range [Vpp]	2.0			0.6		0.7		-	-	1.6
SNDR@LF [dB]	-[2]	60.2	57.3	-	-	-	-	53.1	64.8	59.0
SFDR@LF [dB]	-[2]	70.2	64.7	-	-	-	-	-	-	71.9
SNDR@Nyquist [dB]	57.9	59.0	57.8	41.1	38.2	36.2	33.4	-	-	58.7
SFDR@Nyquist [dB]	66.1	64.6	62.0	>50	>50	48.5	48.4	-	-	72.4
Power [mW]	24.7[1]	27.1	31.5	1.94		10.6	10.3	0.297	-	14.5
FoMw [fJ/c.step]	154[1]	149	199	20.9	29.2	200	260	16100	4180[3]	34.4
FoMs [dB]	155[1]	156	154	155	152	143	140	132	144[3]	162
Core area [mm^2]	0.484			0.042		0.045		2.7[4]		0.621
Gain Calibration Free?	Yes			-		-		-		No

[1]Including voltage drop in cryostat [2]Not measured due to increased loss of balun [3]Calculated with power consumption at 4.4 K [4]Full chip

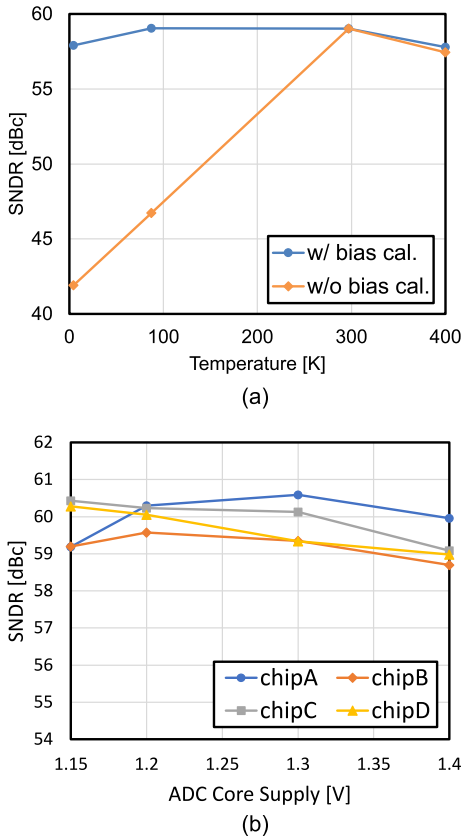

Fig. 18. Measured SNDR variation across (a) temperature and (b) ADC core supply voltage.

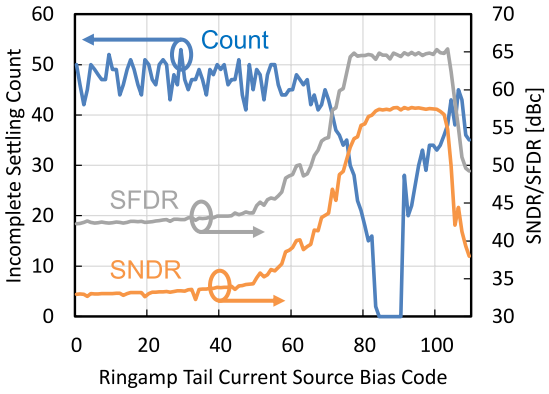

Fig. 19. Measured incomplete settling count, SNDR, and SFDR across the bias code of ringamp tail current source.

pronounced ringing on the reference voltage, due to higher quality factor of on-chip bypass capacitors. This effect can be relieved by inserting a small resistance in series with the bondwire.

Fig. 21 shows the measured differential non-linearities (DNLs) and integral non-linearities (INLs). As analyzed in Section IV-C, the ringamp with proposed cascode CLS can settle within 1/8 LSB of an ideal output voltage, but measured INL shows 4 LSB jump. With further analysis, we found that an insufficient shielding between the input and the output nodes of the ringamp causes gain mismatch, leading to larger DNL/INL and lower SFDR.

The ADC achieves a Walden-figure-of-merit (FoM) of 154, 149, and 199 fJ/conv.-step with power consumption of 24.7, 27.1, and 31.5 mW at 4.6, 300, and 400 K, respectively, which are comparable with state-of-the-art extreme temperature ADCs. At 300 K, the consumed 27.1 mW is comprised of 17.4 mW for the ADC core, 8.8 mW for the clock buffer/generator, and 0.89 mW for the digital correction and decimation logic. The increased power consumption at higher temperatures is dominated by the clock distribution and digital circuits, due to increased crowbar current of CMOS circuits at those temperatures.

A performance summary and comparison with state-of-the-art extreme temperature ADCs is provided in Table I. The proposed ADC achieves both high SNDR (>57 dB) and high sampling rate (250 MS/s) with comparable Walden- and Shreier-FoMs to other ADCs from 4.6 to 400 K. To the best

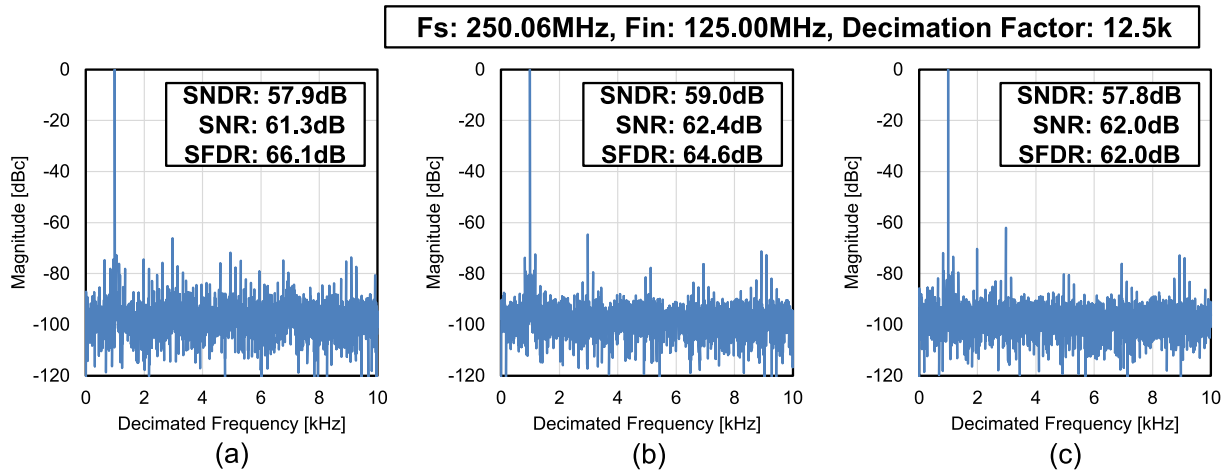

Fig. 20. Measured 4096-point FFT spectrum with near-Nyquist frequency input at (a) 4.6, (b) 300, and (c) 400 K.

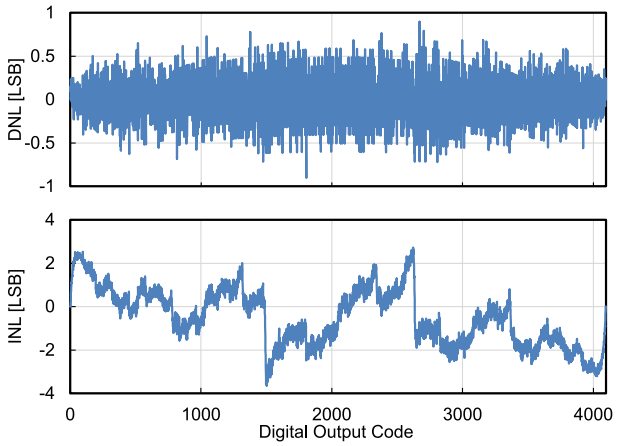

Fig. 21. Measured differential and integral non-linearities at 300 K.

of our knowledge, the achieved operation temperature range of 395 K is the widest ever reported for a pipelined ADC.

VII. Conclusion

This article introduces a ring amplifier with unity-gain-frequency-aware bias calibration, first-stage bias enhancement, and cascode-CLS technique. The ringamp operates across a wide temperature range of 4.6–400 K, by stabilizing the BW, optimizing the PM, and relieving the voltage headroom constraints of the fully differential first stage. The cascode-CLS technique facilitates high accuracy operation without the need for gain calibration.

The prototype ADC, fabricated in 65 nm CMOS technology, achieved an SNDR of over 57.7 dB with Nyquist input across a temperature range of 4.6–400 K. It demonstrates a Walden FoM of 154 fJ/conversion-step at 4.6 K, comparable with state-of-the-art extreme environment ADCs.

Acknowledgment

The authors would like to thank Dr. T. Tanaka, Keio University, Yokohama, Japan, for assisting the cryogenic measurement.

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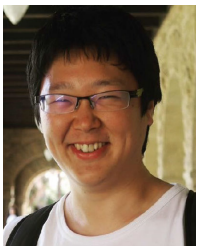

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