# Ring Amplifiers for Switched Capacitor Circuits

Benjamin Hershberg<sup>1</sup>, Skyler Weaver<sup>1</sup>, Kazuki Sobue<sup>2</sup>, Seiji Takeuchi<sup>2</sup>, Koichi Hamashita<sup>2</sup>, Un-Ku Moon<sup>1</sup>

<sup>1</sup>Oregon State University, Corvallis, OR, USA <sup>2</sup>Asahi Kasei Microdevices, Atsugi, Japan

## A/D Scaling Trends: FoM<sub>1</sub>



- Performance continues to scale well with process
- FoM<sub>1</sub> best describes low/medium-resolution A/D performance

#### [Jonsson, NORCHIP 2010]

## A/D Scaling Trends: FoM<sub>2</sub>



- FoM<sub>2</sub> best describes high-resolution A/D performance
- Noise floor degrades faster than power/speed improves.

#### [Jonsson, NORCHIP 2010]

We need amplifiers that are:

- Immune to SNR loss from low-voltage, degrading r<sub>o</sub>
- Exploit digital scaling benefits
- Avoid conventional RC-based settling

### **Beating the Trend**



#### Ring Amplifier (Ring Amp, RAMP)

# **Ring Amplification**

**Basic Theory** 

## **Ring Amplifier: Basic Theory**



Basic MDAC test structure

## **Ring Amplifier: Basic Theory**



- Ring Oscillator
- Unstable...

...but will oscillate around the correct settled value

#### **Ring Oscillator Sample Waveform**



## **Ring Amplifier: Basic Theory**



- Split signal into two separate paths
- Embed offset in each path























## $V_{OV}$ Dynamic Pinch-off



## $V_{OV}$ Dynamic Pinch-off



- Dominant pole  $\rightarrow$  DC

## **Ring Amplifier Core Benefits**

#### Slew-based charging

- Charges with maximally biased, digitally-switched current sources
  - V<sub>OV</sub> = V<sub>DD</sub>
  - Can be very small, even for large  $C_{LOAD}$
  - Decouples internal speed vs. output load requirements

#### Exponential dynamic stabilization

- Very fast
- Well defined tradeoffs

## **Ring Amplifier Core Benefits**

#### Scalability (Speed/Power)

- Internal speed/power (mostly) independent of C<sub>LOAD</sub>
  - Inverter t<sub>d</sub>, crowbar current, parasitic C's
  - Digital power-delay product scaling benefits apply
- Power/speed product scales with digital process trends



## **Ring Amplifier Core Benefits**

#### Scalability (Output Swing / SNR)

- Compression immune: rail-to-rail output swing
  - 50dB: Input-referred dead-zone size will limit accuracy
  - 90dB: dynamic pinch-off effects maintain high accuracy
  - V<sub>OV</sub> pinchoff: decreases V<sub>DSAT</sub>, decreses I<sub>D</sub>, increases r<sub>o</sub>



# **ADC Implementation Details**



• Split-CLS

- Generalized form of Correlated Level Shifting (CLS)

#### [Hershberg, ISSCC 2010]



#### Φ<sub>1</sub>:

- amp charges output directly
- processes full signal

#### **Amplifier Design Requirements**

	Φ <sub>1</sub>	Φ <sub>2</sub>
Output Swing	Large	Small
Slew Rate	Large	Small



#### Φ<sub>2</sub>:

- opamp is level-shifted to mid-rail
- processes error only

#### **Amplifier Design Requirements**

	Φ <sub>1</sub>	Φ <sub>2</sub>
Output Swing	Large	Small
Slew Rate	Large	Small

- Optimized design for each phase
  - Increase overall accuracy & efficiency
- This design:
  - $\Phi_1$ : Ring Amp
  - $-\Phi_2$ : Telescopic opamp
- Finite opamp gain error becomes approx.  $1 / (A_1 * A_2)$

55dB ring amp

- + 65dB opamp
  - 120dB effective gain

#### **Pipelined ADC Overview**



## Pipelined ADC Stage 1 MDAC



## Pipelined ADC Stage 2-4 MDAC



## Pipelined ADC Stage 5-6 MDAC



## **Ring Amplifier Core Structure**



- No need to refresh every cycle.
- Can disable ring amp when not in use

## **Ring Amplifier Power Save Feature**



- Only enable when amplifying or refreshing
- Refresh only once every N cycles (during  $\Phi_S$ )

## **Ring Amplifier CMFB**



### Float-Biased Switched Opamp



### **Float-Biased Switched Opamp**



### Float-Biased Switched Opamp



## **Measurement Results**



#### Input Spectrum



#### Performance vs. Input Frequency



#### SNDR vs. Input Amplitude



#### Ring Amp Dead-Zone Sensitivity



## Ring Amp Supply Sensitivity



## **Opamp Float-Bias Switching**

• Reduces total opamp power by 35%:

1769uA → 1151uA

• Bias network isolation improves accuracy by 0.6dB:

76.2dB → 76.8dB

## **Performance Summary**

Technology	0.18µm 1P4M CMOS
Resolution	15 bits
Analog Supply	1.3 V
Sampling rate	20 Msps
ERBW	10 MHz
Input Range	2.5 V pk-pk diff.
SNDR	76.8 dB
SNR	77.2 dB
SFDR	95.4 dB
ENOB	12.5 bits
Total Power	5.1 mW
FoM	45 fJ/c-step



(nyquist or oversampling)

[B. Murmann, 2011]

## Conclusion

- Ring Amplification
  - High efficiency slew-based charging
  - Rail-to-rail output swing
  - Performance scales with digital process
- Split-CLS
  - Efficient coarse charging
  - Very accurate fine settling
  - High-efficiency, high accuracy amplification

# Thank you for your attention

# **Additional Slides**

Possibly useful in Q&A afterwards

#### Systematic dead-zone offset

#### **1st Stage Deadzone vs SNDR**



## **Ring Amp Accuracy**

- Determined using 2 independent test approaches
- Ring Amps contribute ~55dB to overall accuracy

Test method 1: Increase  $f_s$  until opamps don't have enough time to turn on.

Peak SNDR vs. Sampling

Frequency

Test method 2: Power down opamps, and adjust the time the ring amps are allowed to settle.

> SNDR vs. Ring Amp Timing (with opamps off)



#### Input-cap clearing

• FFT spectrum when the input capacitors aren't cleared before being re-connected to the chip signal input:



## More about Compression Immunity

- Isn't this just a 90dB amplifier that's been limited by the dead-zone size to look like a 60dB amplifier?
  - Answer: No!
- With a well chosen dead-zone value:
  - Current pinches off, increasing r<sub>o</sub>
  - $V_{\rm OV}$  shrinks, decreasing  $V_{\rm DSAT}$
  - High gain preserved, even when  $V_{\text{DS}}$  is very small
- Depends on dead-zone value?
  - Yes, but doesn't actually matter...
  - Small dead-zone: compression immune
  - Large dead-zone: some compression (lower accuracy anyway)

#### Power Breakdown



## DNL - INL



### Supply current vs. Stage 1 DZ



## A/D Scaling Trends: FoM<sub>2</sub>



- FoM<sub>2</sub> best describes high-resolution A/D performance
- Noise floor degrades faster than power/speed improves.

#### [Jonsson, NORCHIP 2010]

## Chip Micrograph



#### Full die micrograph



Stage 1 MDAC





#### **Ring Amp Power-Save Feature**

