A 61.5dB SNDR Pipelined ADC Using Simple Highly-Scalable Ring Amplifiers

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An Incomplete Solution

- Goal: develop truly scalable amplifiers
  - Conventional opamps are fundamentally ill-suited for nanoscale CMOS
  - Efficiency in amplification-based designs is actually getting *worse*

- ADCs
  - Amplifier-less ADCs (i.e. SARs) provide excellent scalability for *some* of the design space
  - Scalable amplifiers are needed to cover the *entire* ADC design space

- The more scalable options we have, the better

Beating the Trend

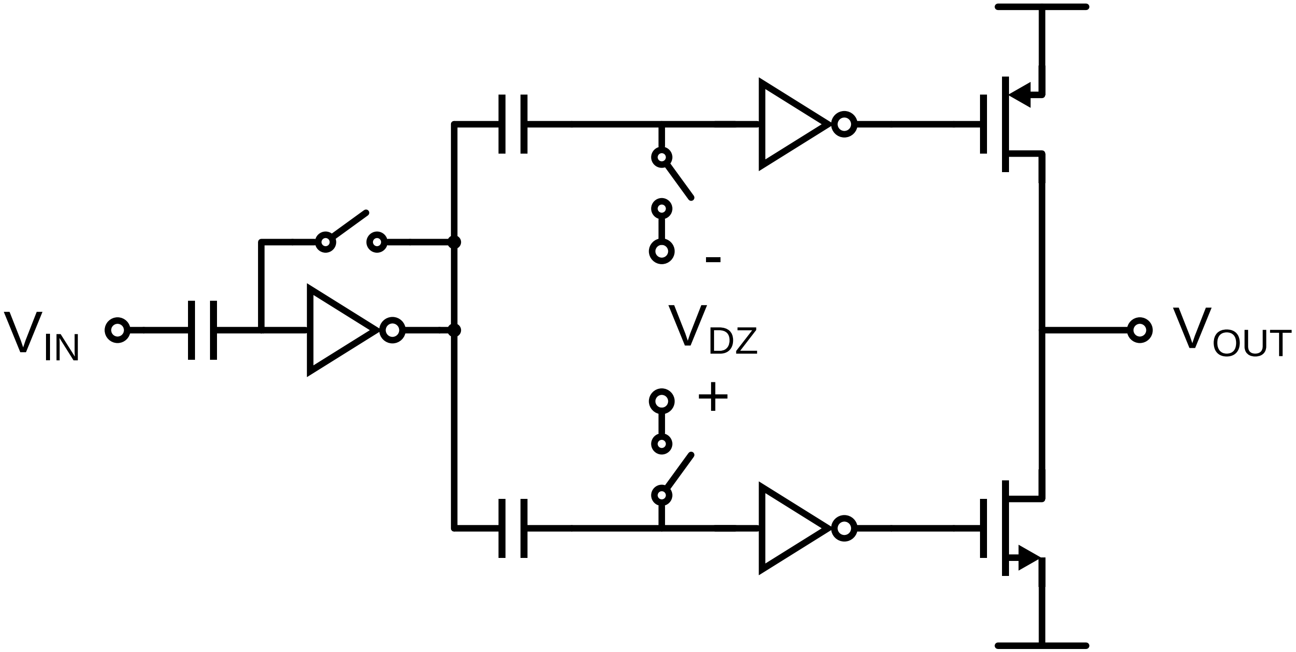
A scalable amplifier must

- Operate well ***in*** nanoscale CMOS
- Improve ***with*** nanoscale CMOS

Circuit level requirements

- Minimize SNR loss from low-voltage, degrading r_o
- Exploit digital scaling benefits
- Avoid conventional RC-based settling

Beating the Trend



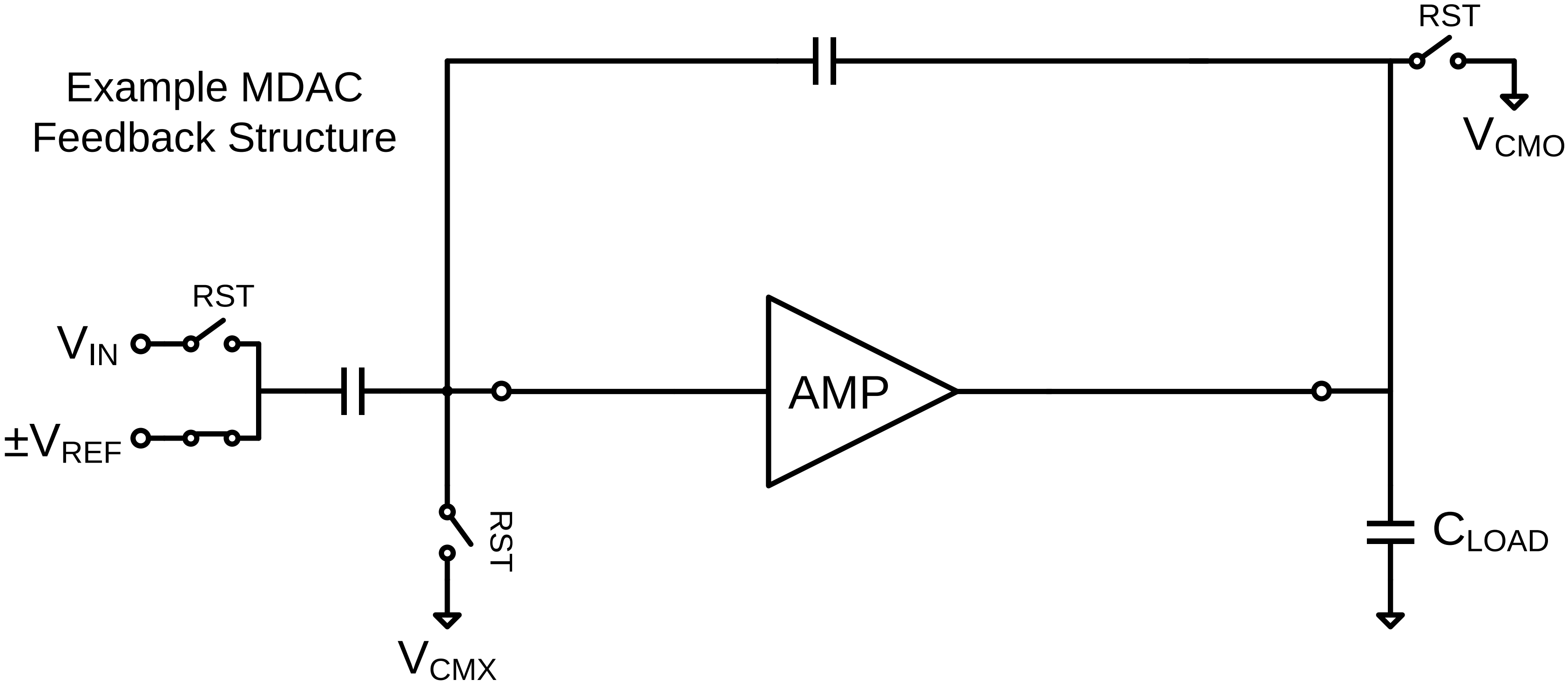
<u>Ring Amplifier</u>

(Ringamp, RAMP)

Ring Amplification

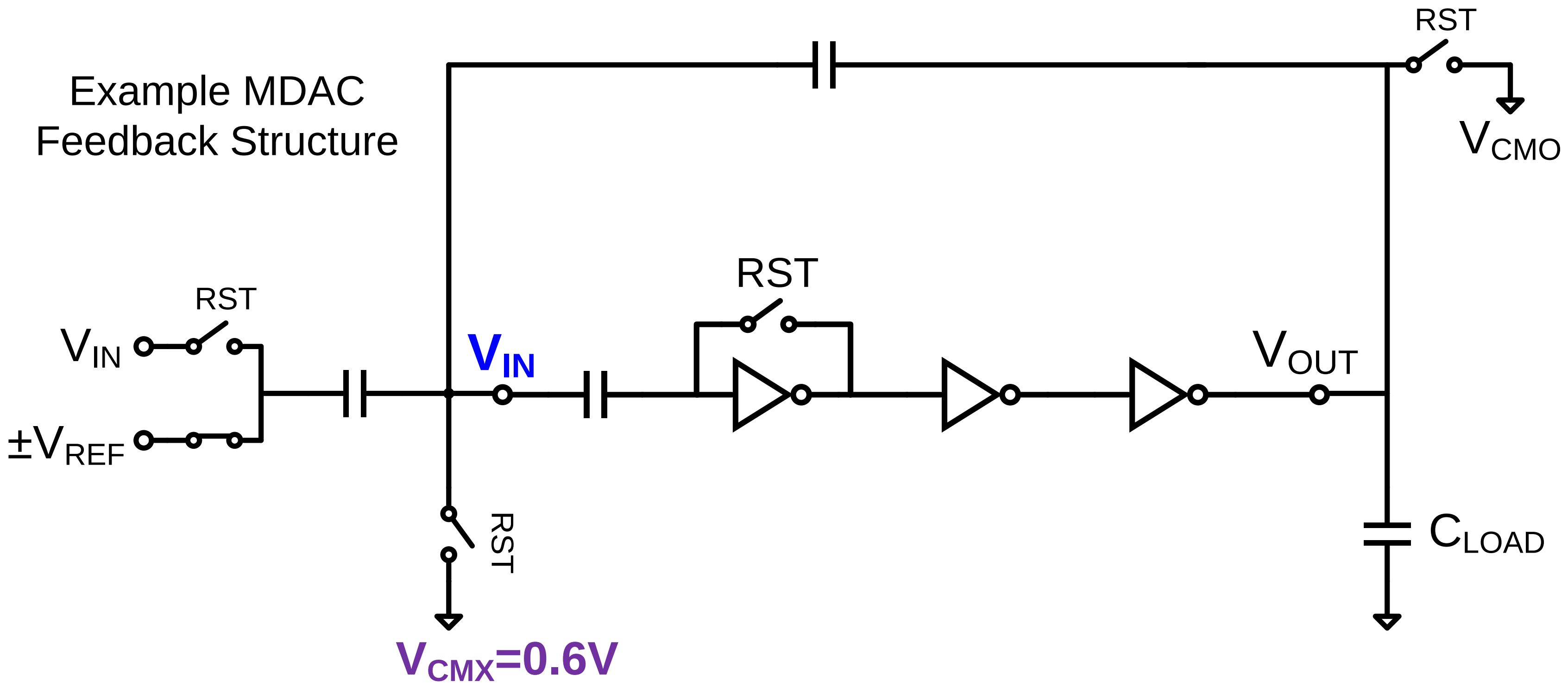
Basic Theory

Ring Amplifier: Basic Theory



- Basic MDAC test structure

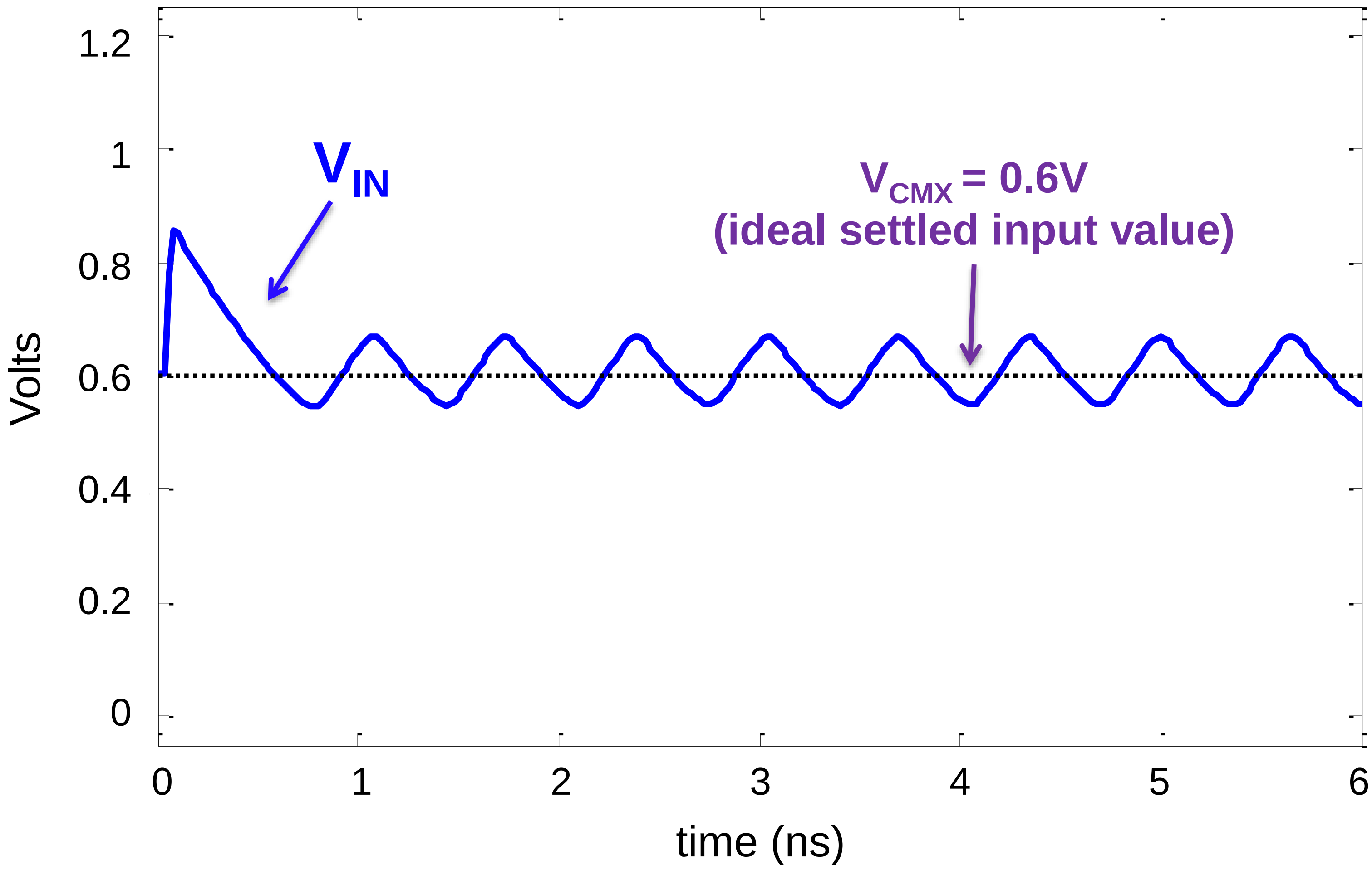
Ring Amplifier: **Basic Theory**



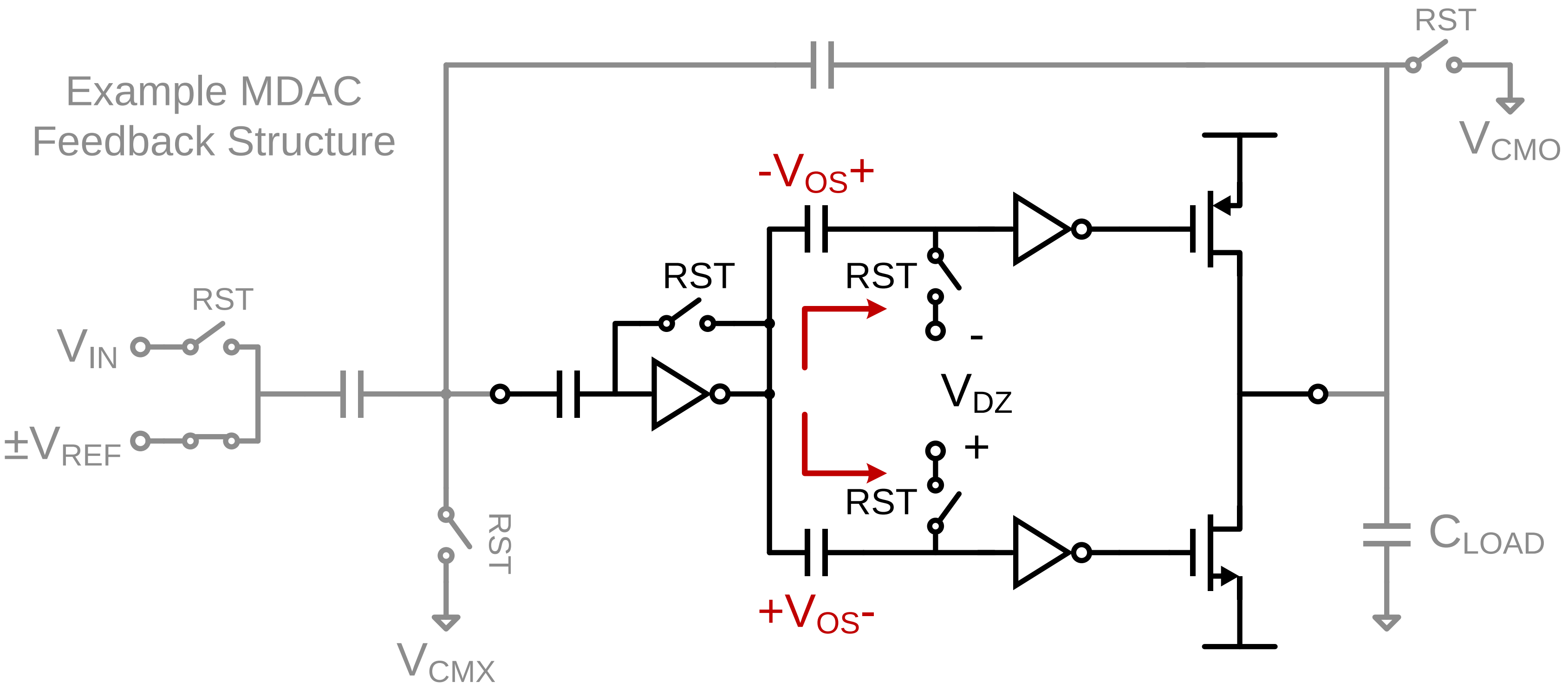
- Ring Oscillator
- Unstable…

…but will oscillate around the correct settled value

Ring Oscillator Sample Waveform

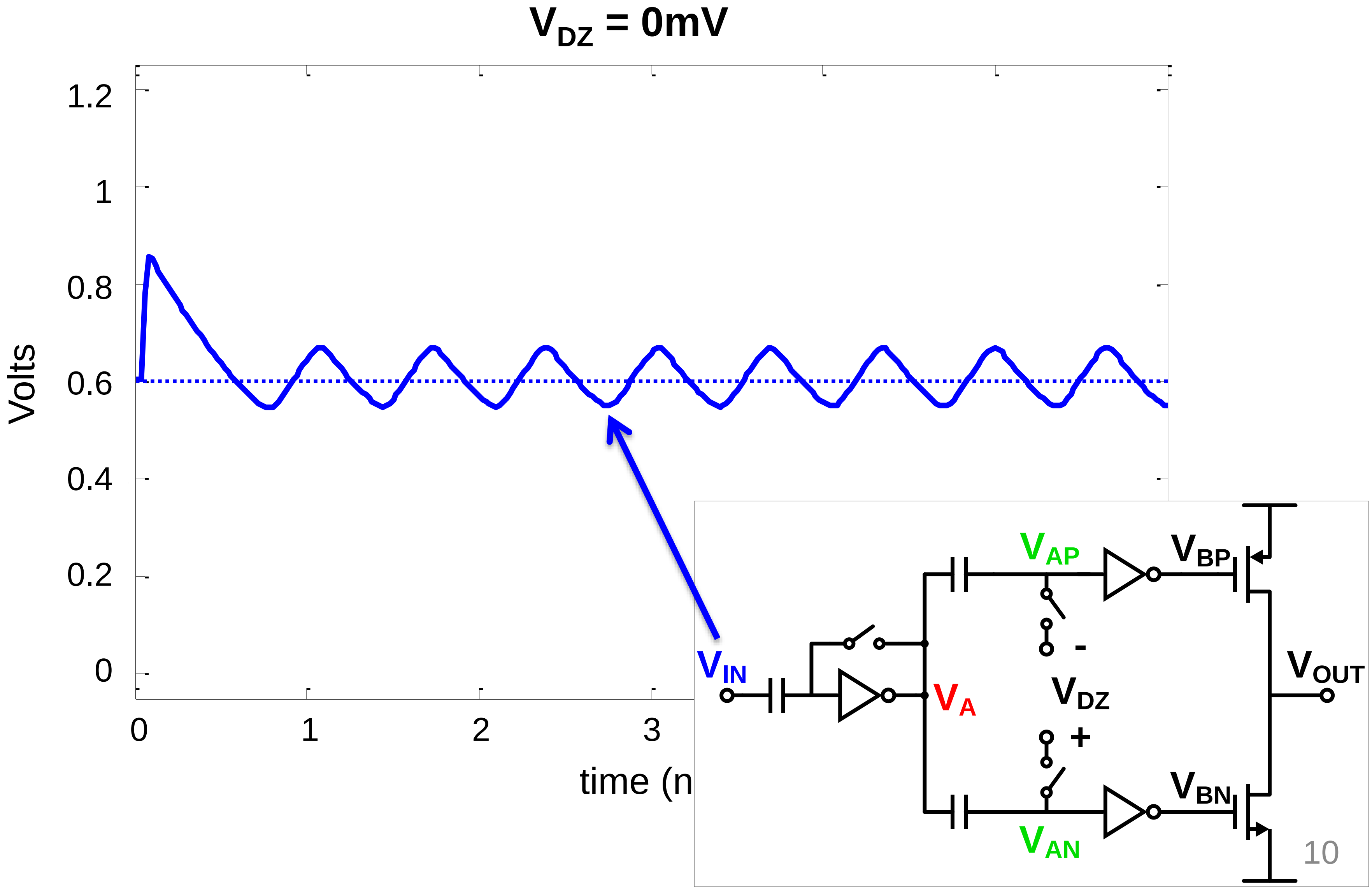


Ring Amplifier: Basic Theory

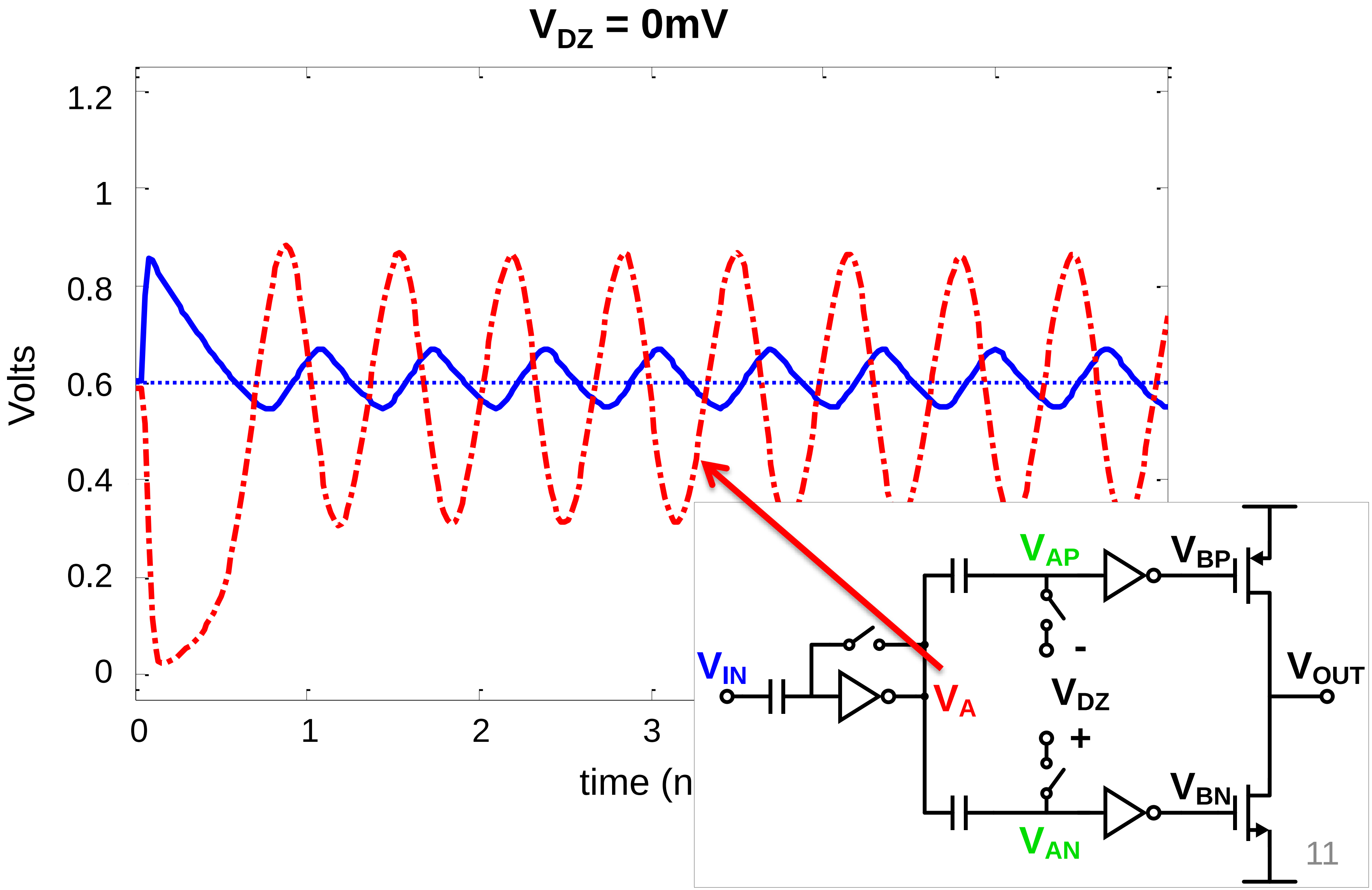


- Split signal into two separate paths
- Embed offset in each path

Ring Amplifier Sample Waveform



Ring Amplifier Sample Waveform



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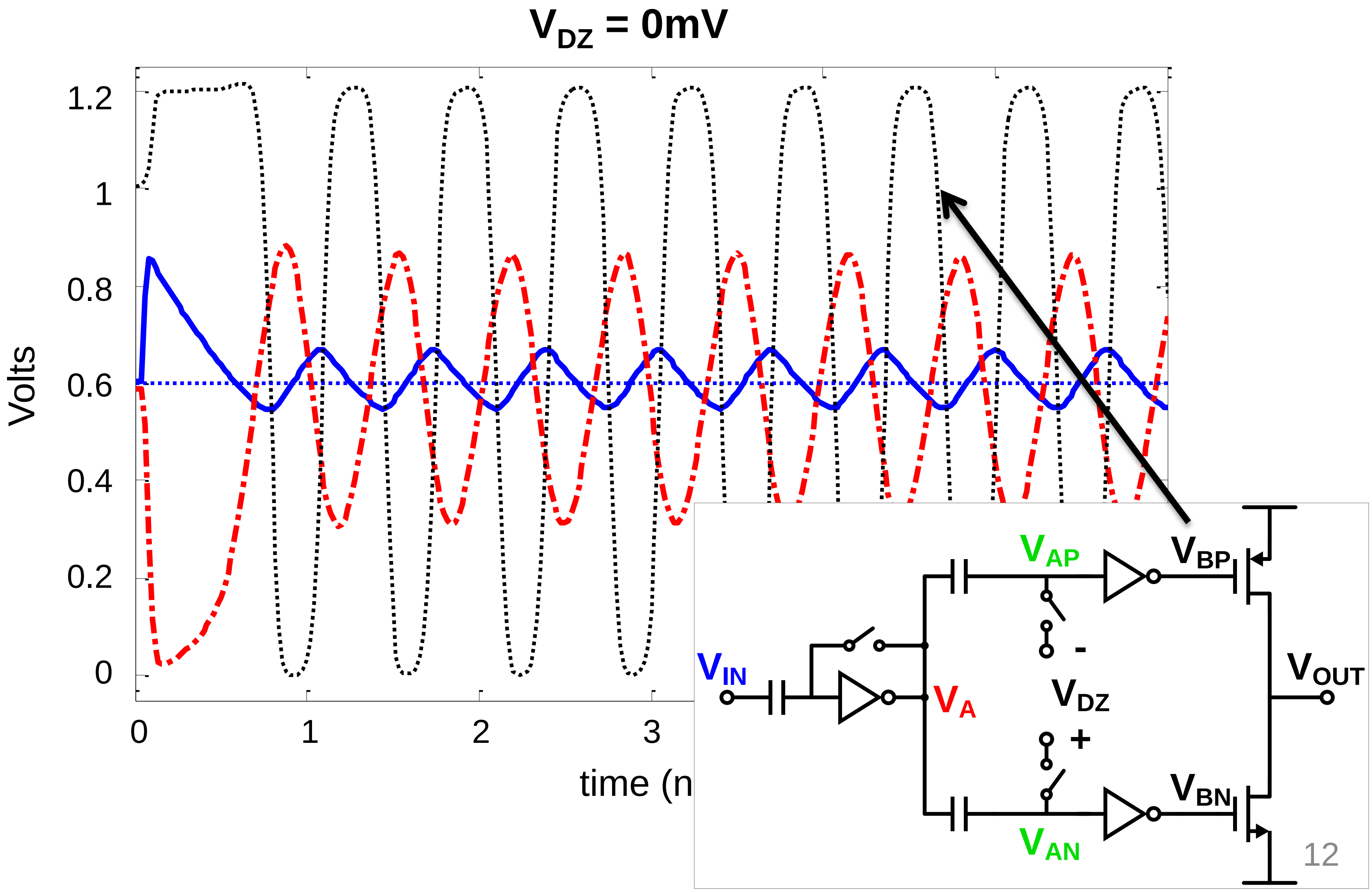

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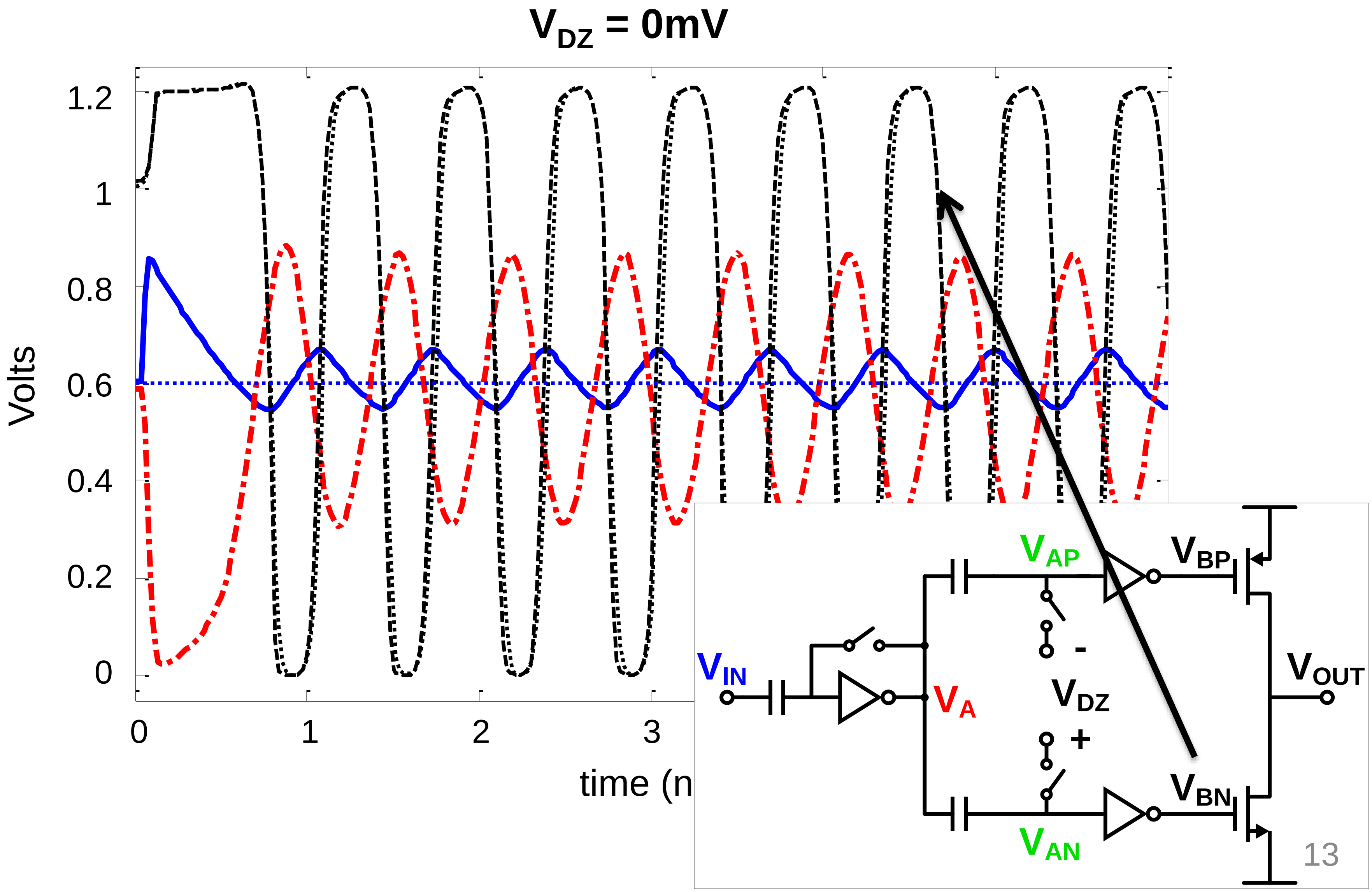
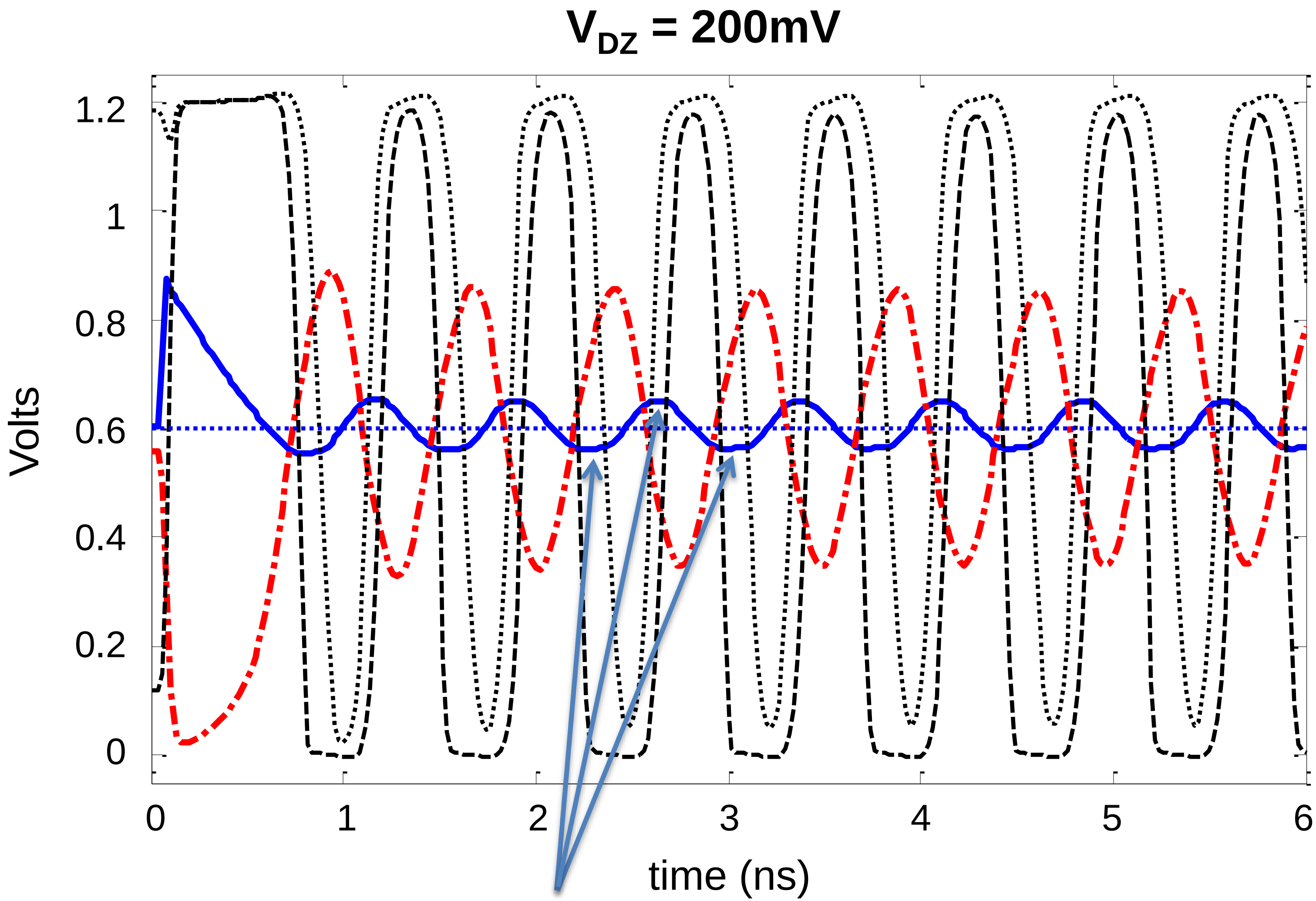
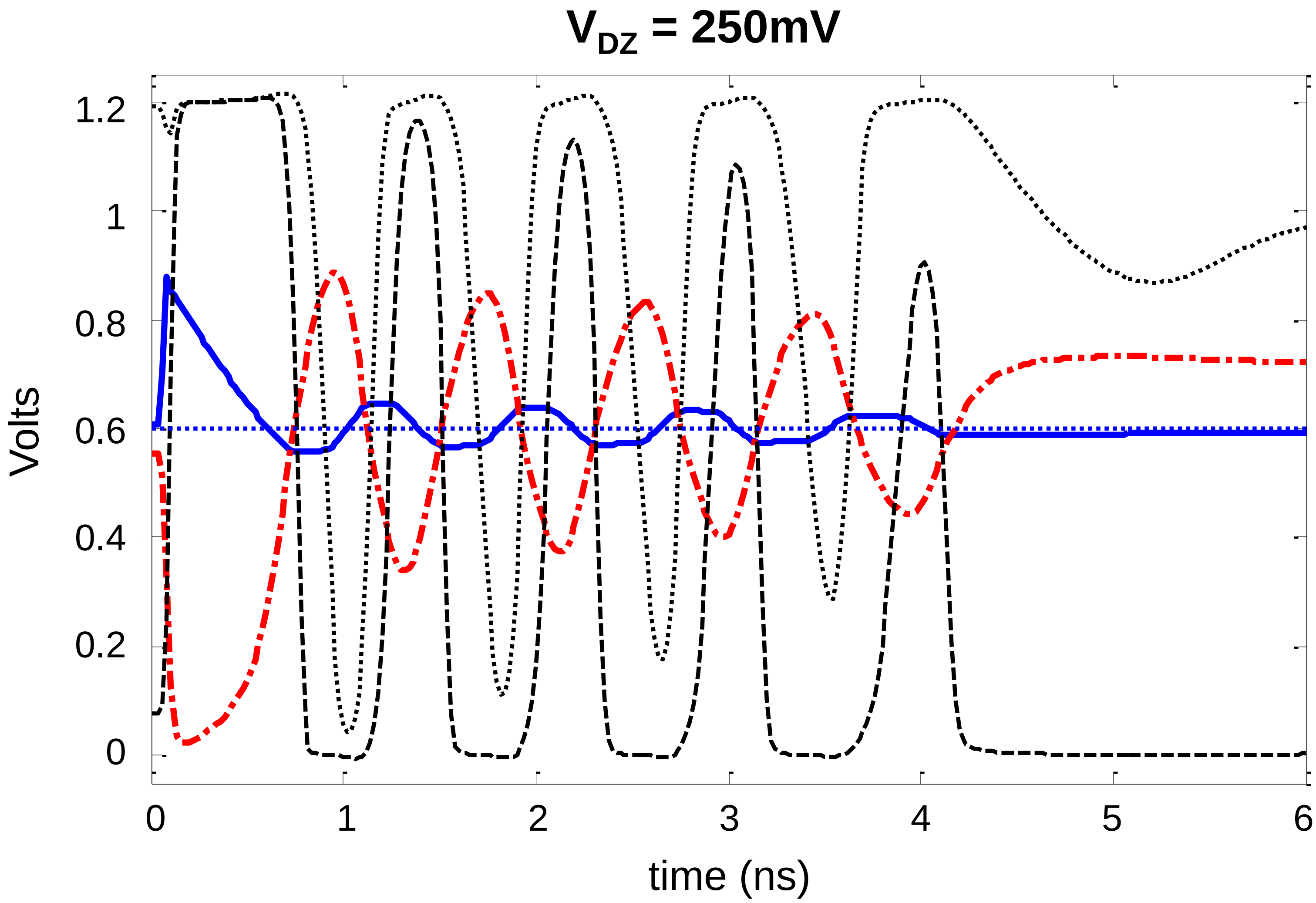


Ring Amplifier Sample Waveform



Plateaus form at dead-zone crossings

Ring Amplifier Sample Waveform



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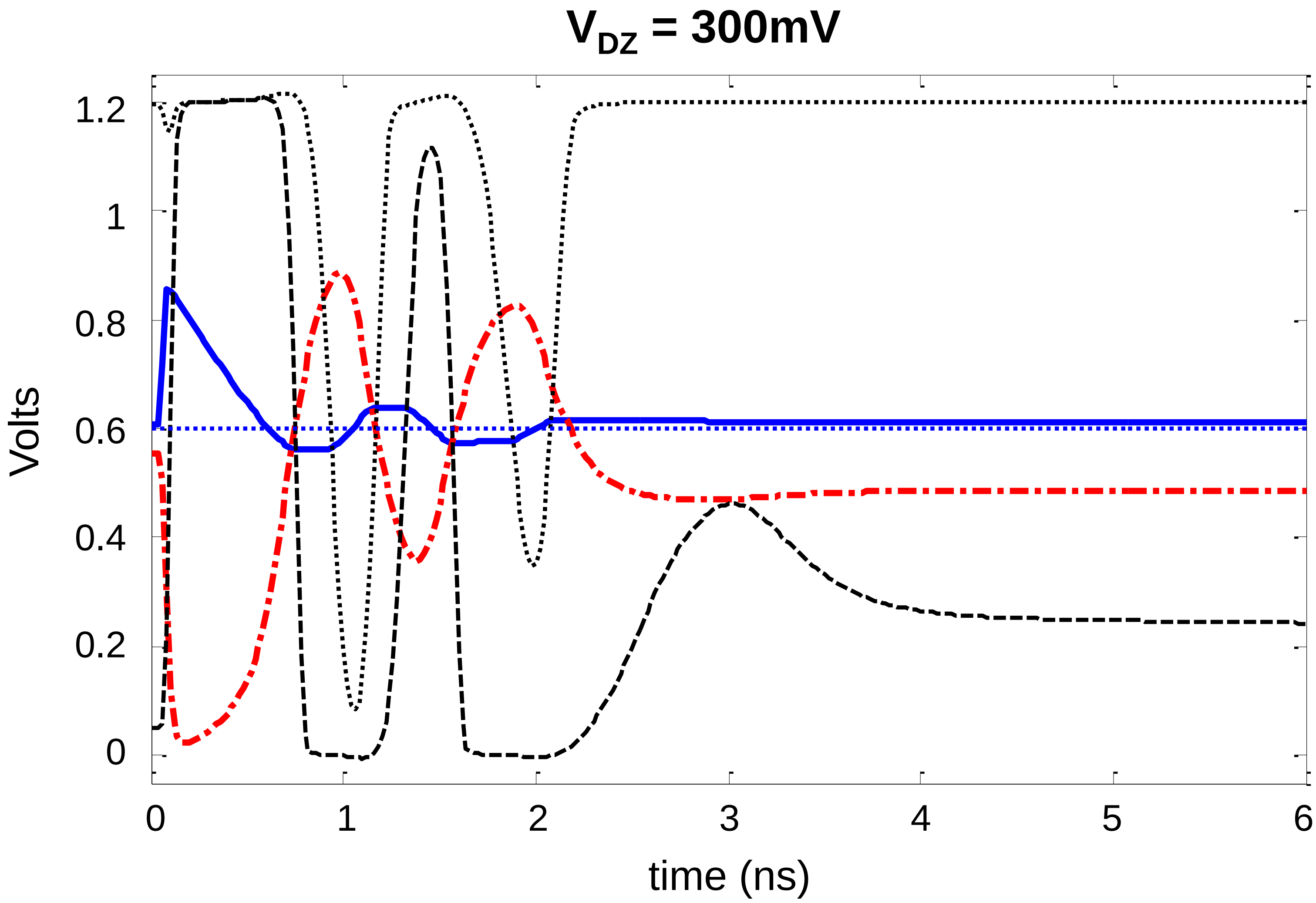
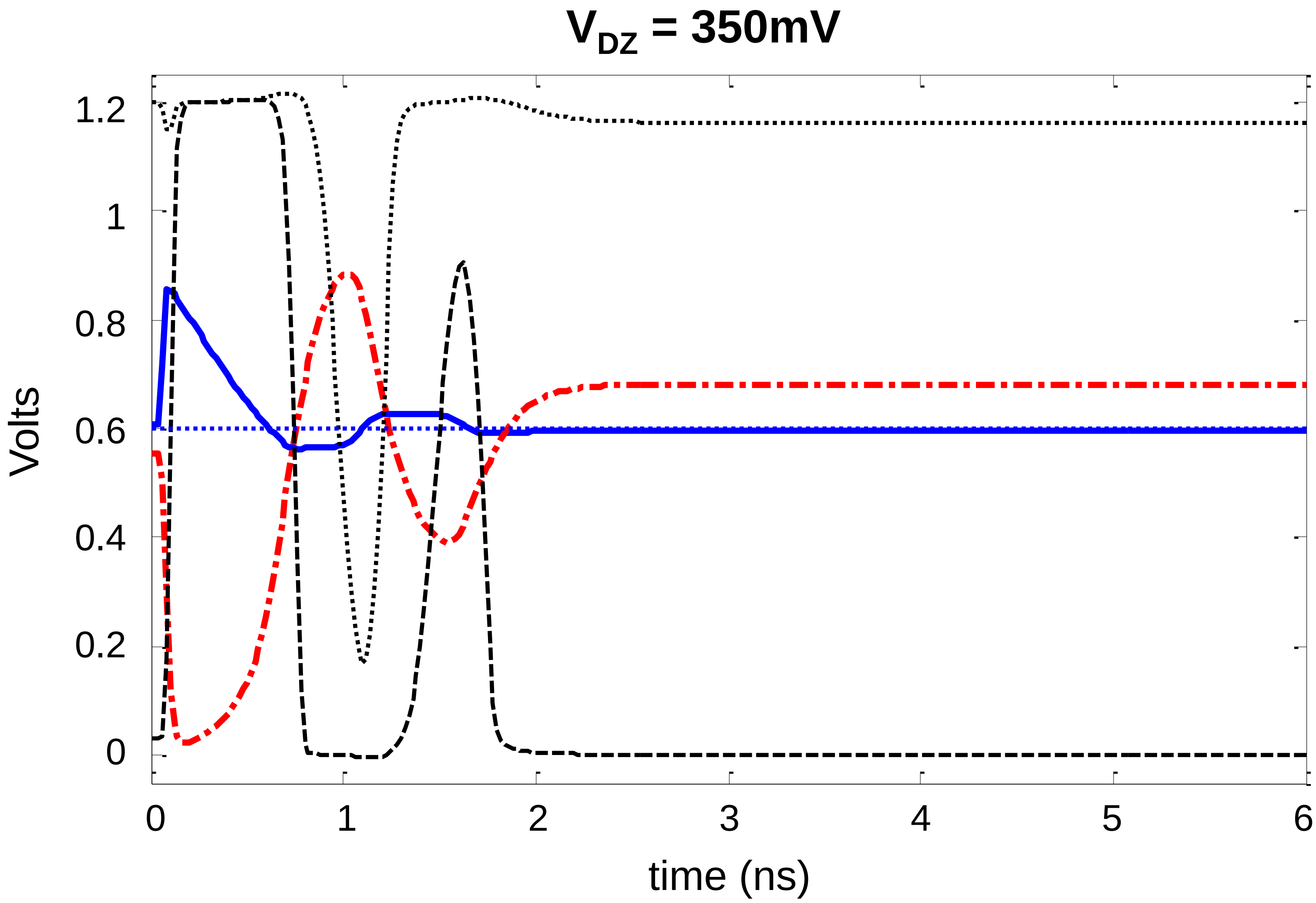


Ring Amplifier Sample Waveform



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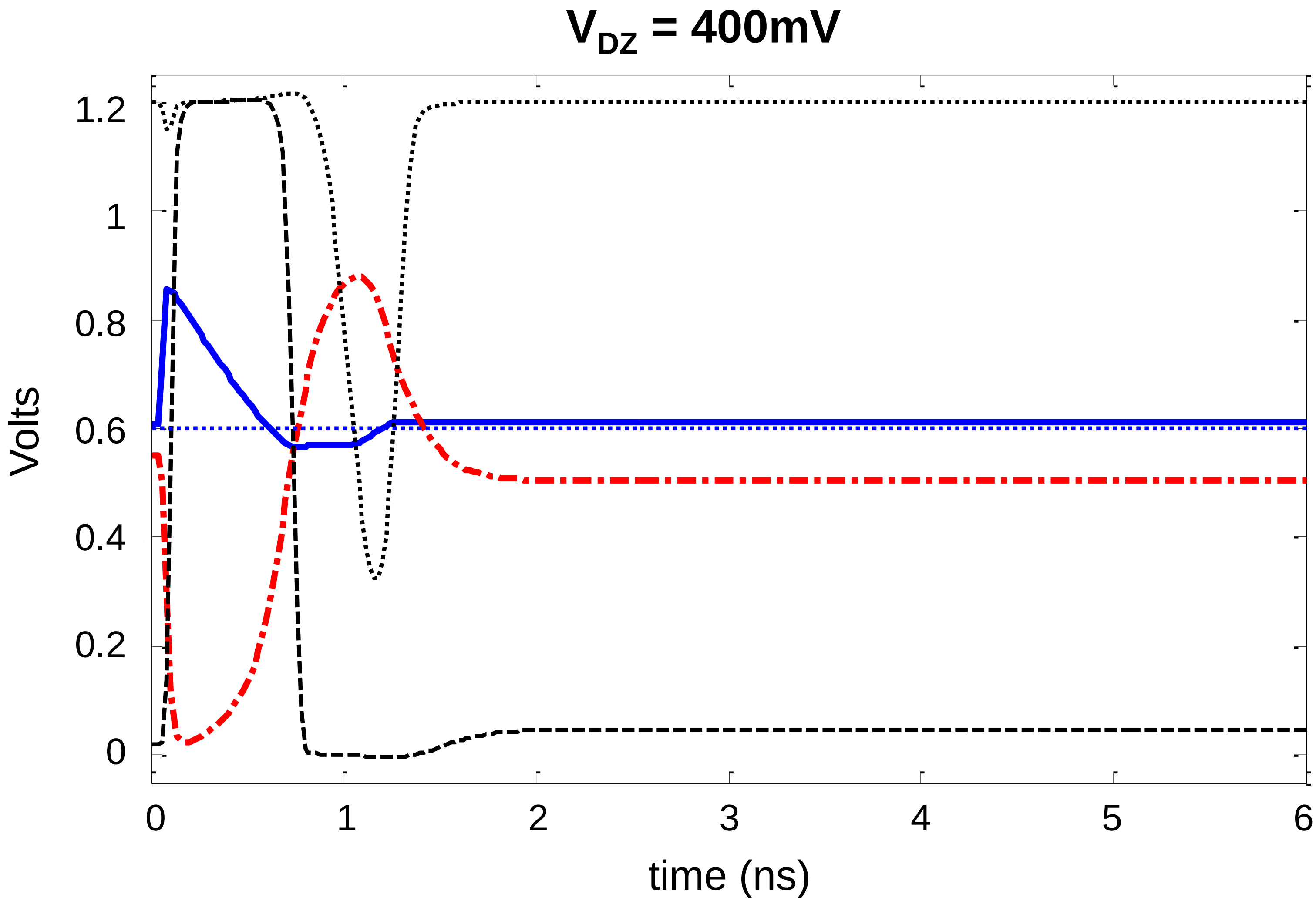
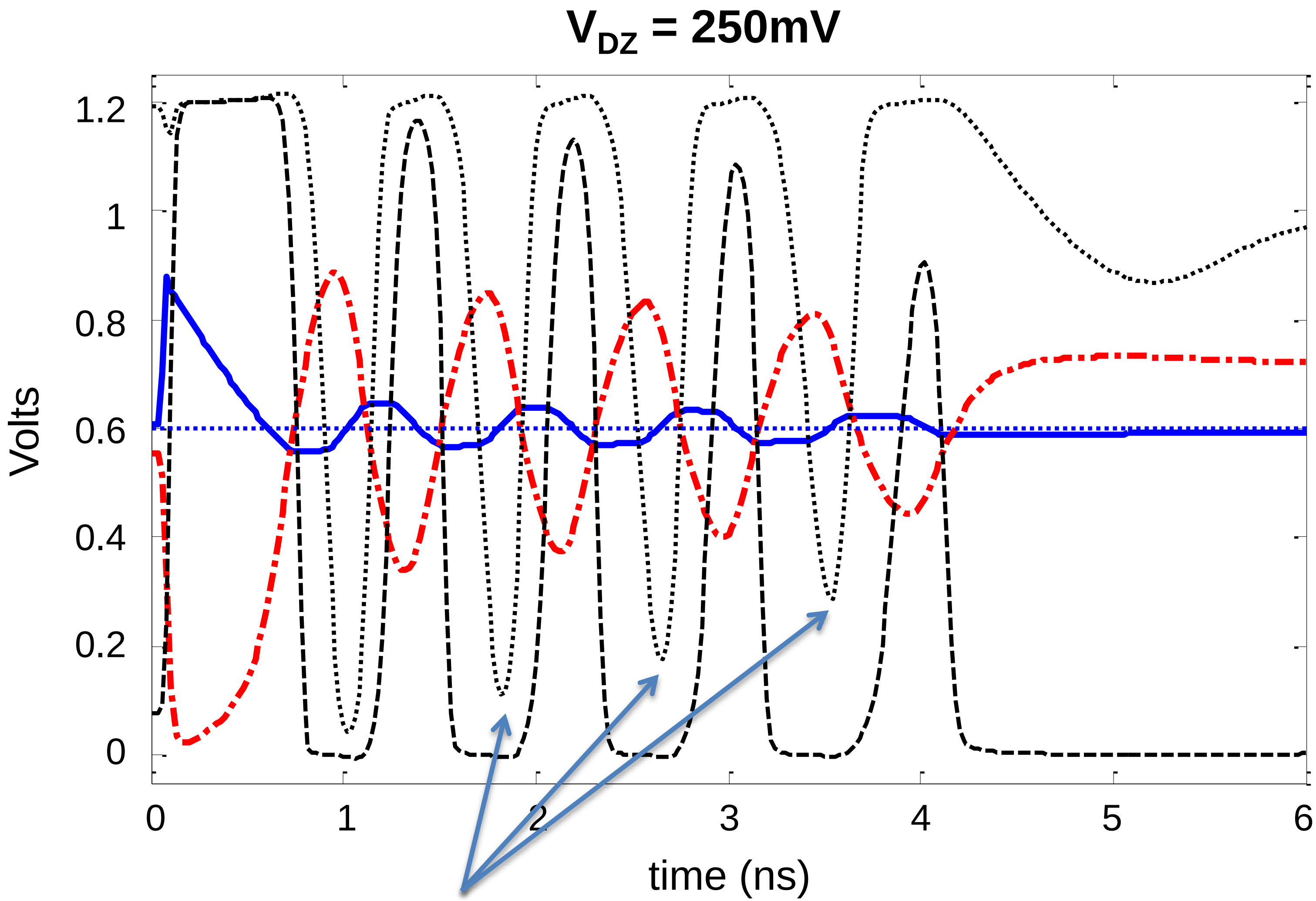
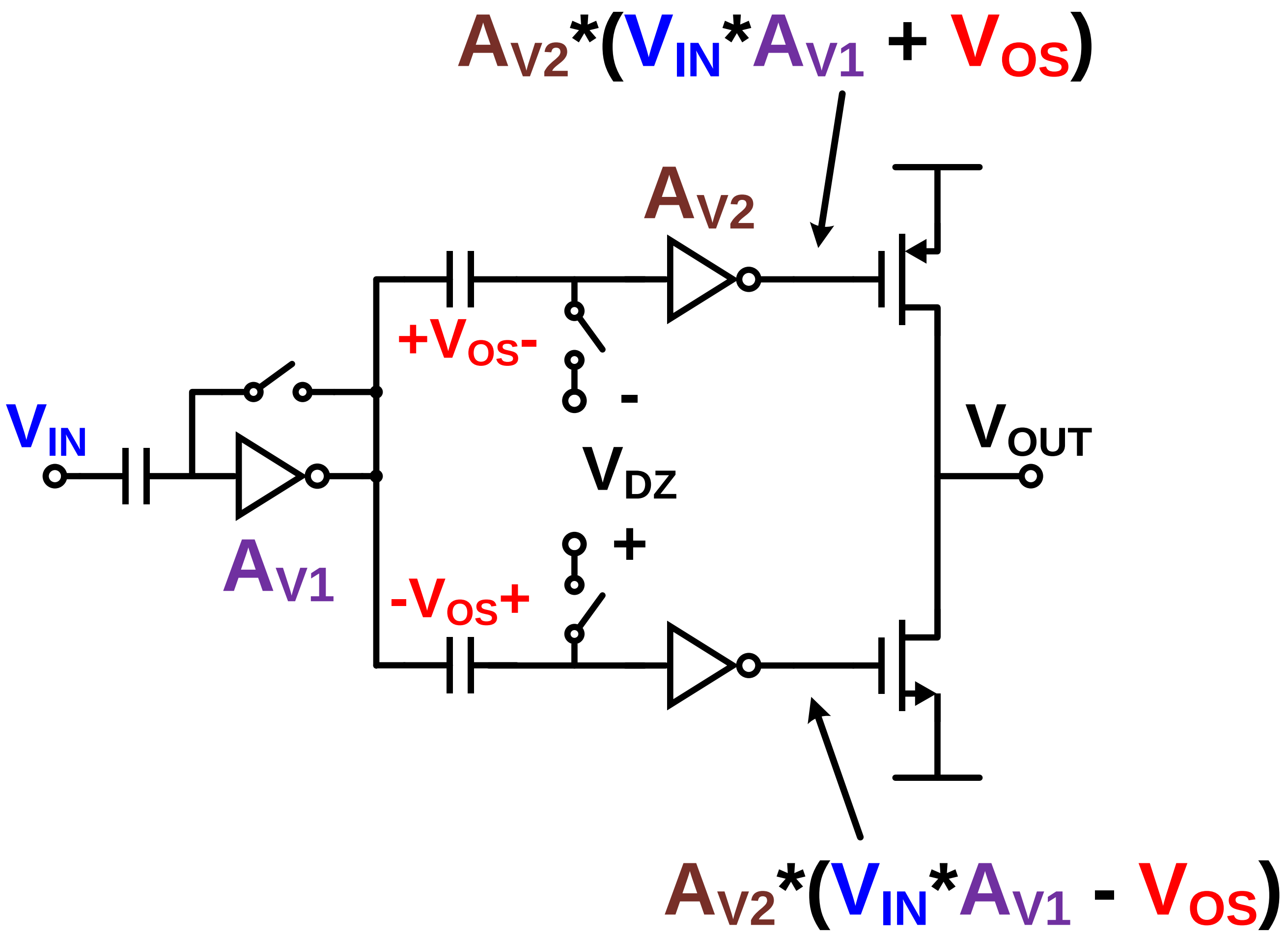


Ring Amplifier Sample Waveform



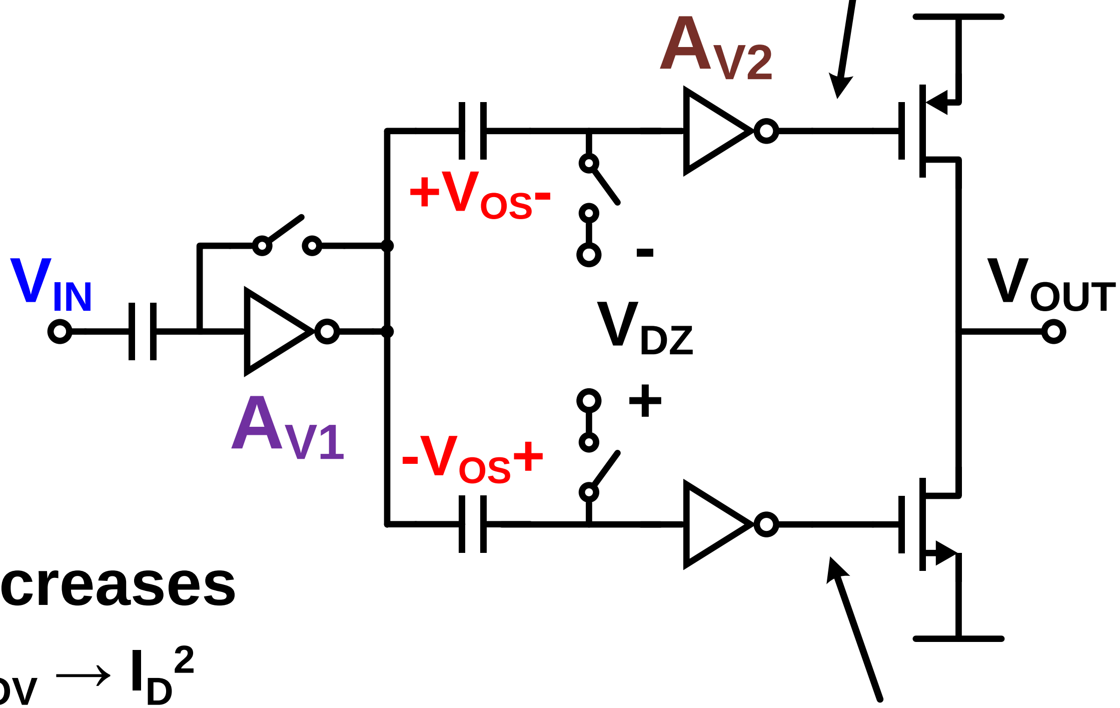
Decreasing V_{OV} reduces slew-rate

V_{OV} Dynamic Pinch-off



V_{OV} Dynamic Pinch-off

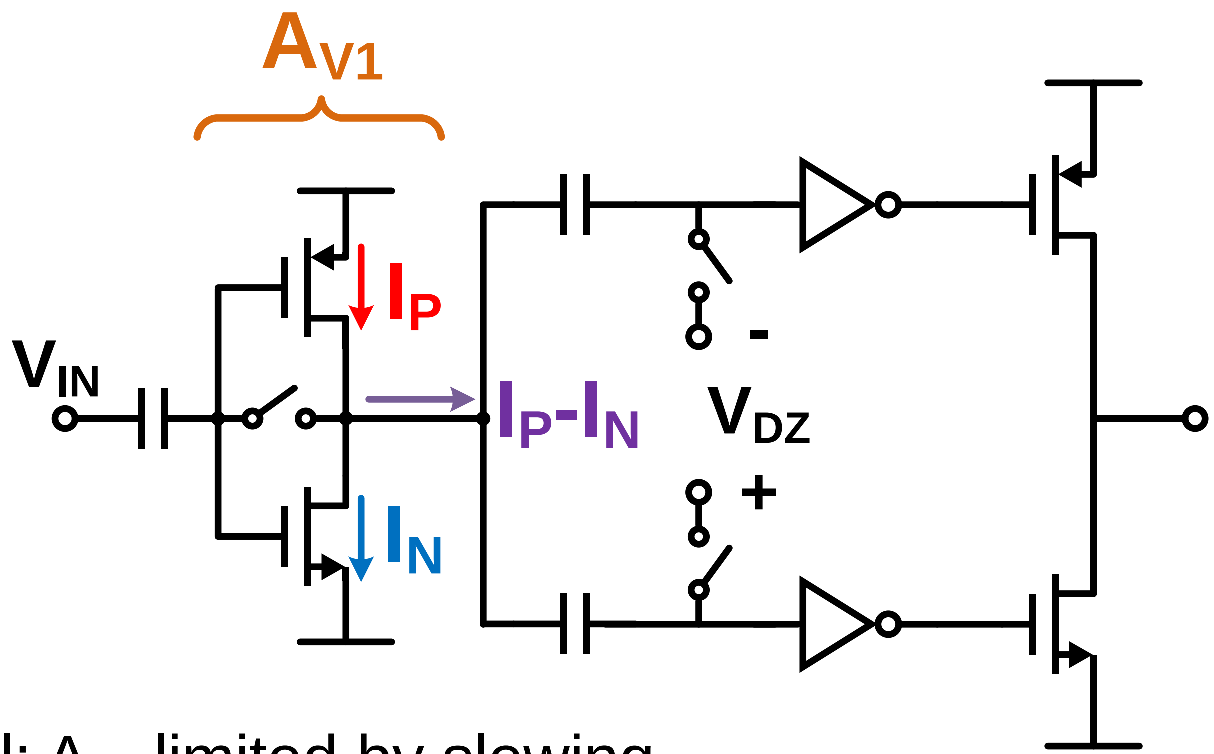
$A_{V2}*(V_{IN}*A_{V1} + V_{OS})$



$A_{V2}*(V_{IN}*A_{V1} - V_{OS})$

- **I_D decreases**
  - **$V_{OV} \rightarrow I_D^2$**
- **R_o increases**
  - **Dominant pole → DC**

Dynamic Dead-zone Adjustment



- Initial: A_{V1} limited by slewing
- Final: A_{V1} set by AC small-signal
- Dynamically adjusts input-referred dead-zone
- Enhances Speed / Accuracy trade-off

Core Benefits

Ring Amplifier Core Benefits

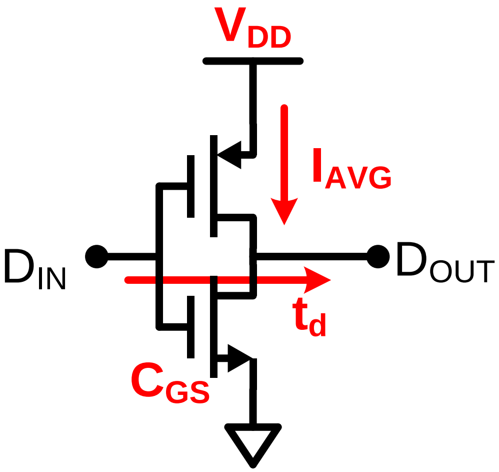
Slew-based charging

- Charges with maximally biased, digitally-switched current sources
  - Can be very small, even for large C_{LOAD}
  - Decouples internal speed vs. output load requirements

Ring Amplifier Core Benefits

Scalability (Speed/Power)

- Internal speed/power (mostly) independent of C_{LOAD}
  - Inverter t_d, crowbar current, parasitic C's
  - Digital power-delay product scaling benefits apply
- Captures the same power/speed trends as digital circuits

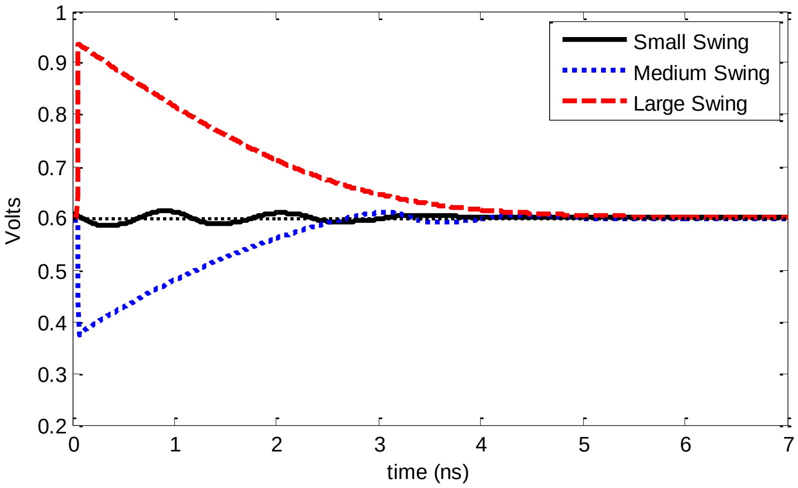


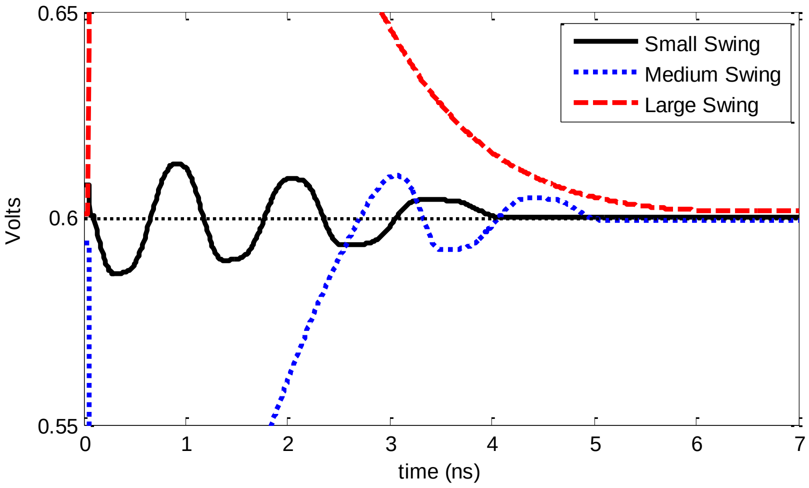
$$PDP = V_{DD} \cdot I_{AVG} \cdot t_d = E_{tot}$$

Ring Amplifier Core Benefits

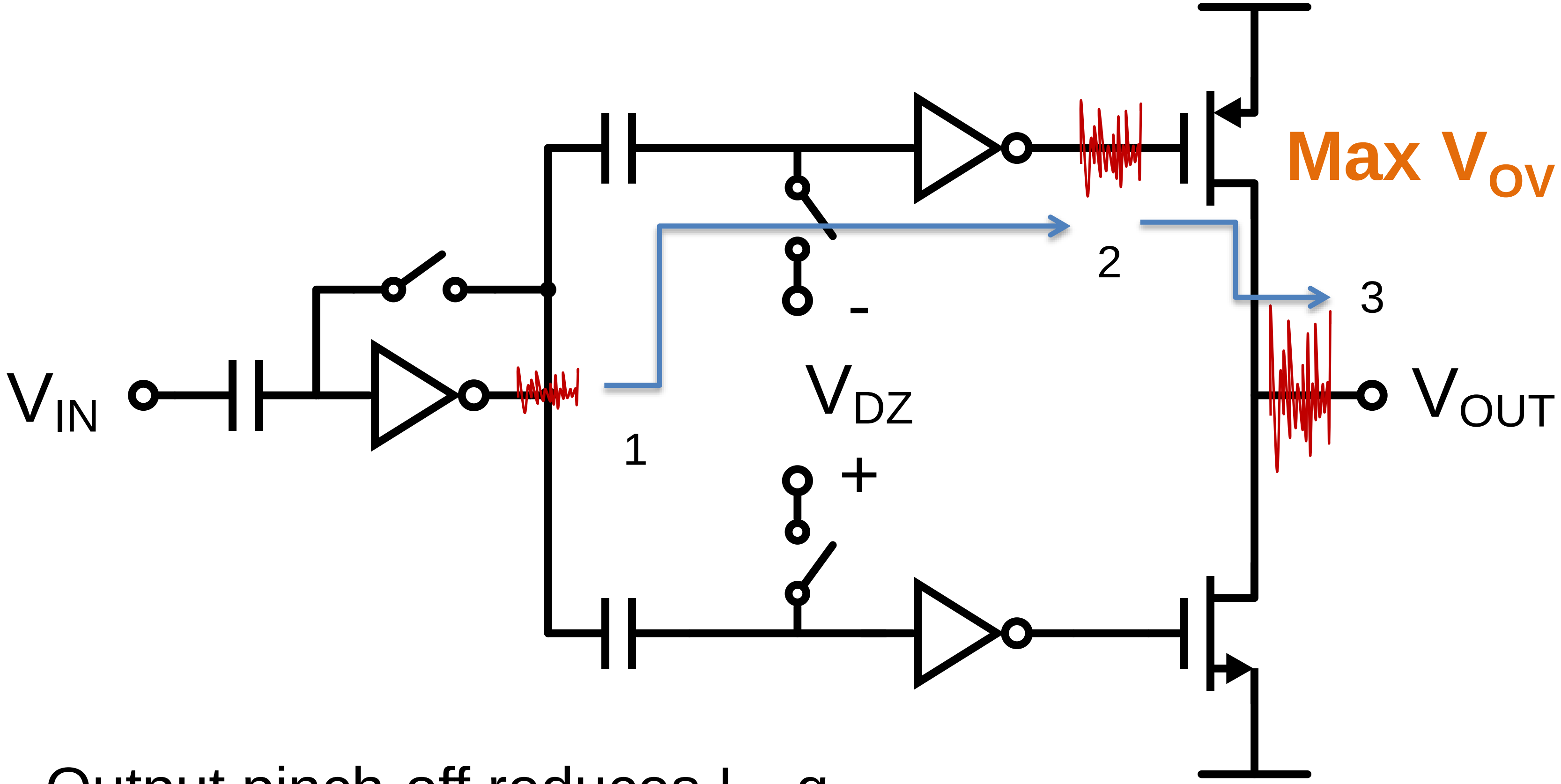
Scalability (Output Swing / SNR)

- Compression immune: rail-to-rail output swing
- 50dB: Input-referred dead-zone size will limit accuracy
- 90dB: dynamic pinch-off effects maintain high accuracy
  - weak inversion
  - saturation even for small V_{DS}
  - gain-boosting from increased r_o



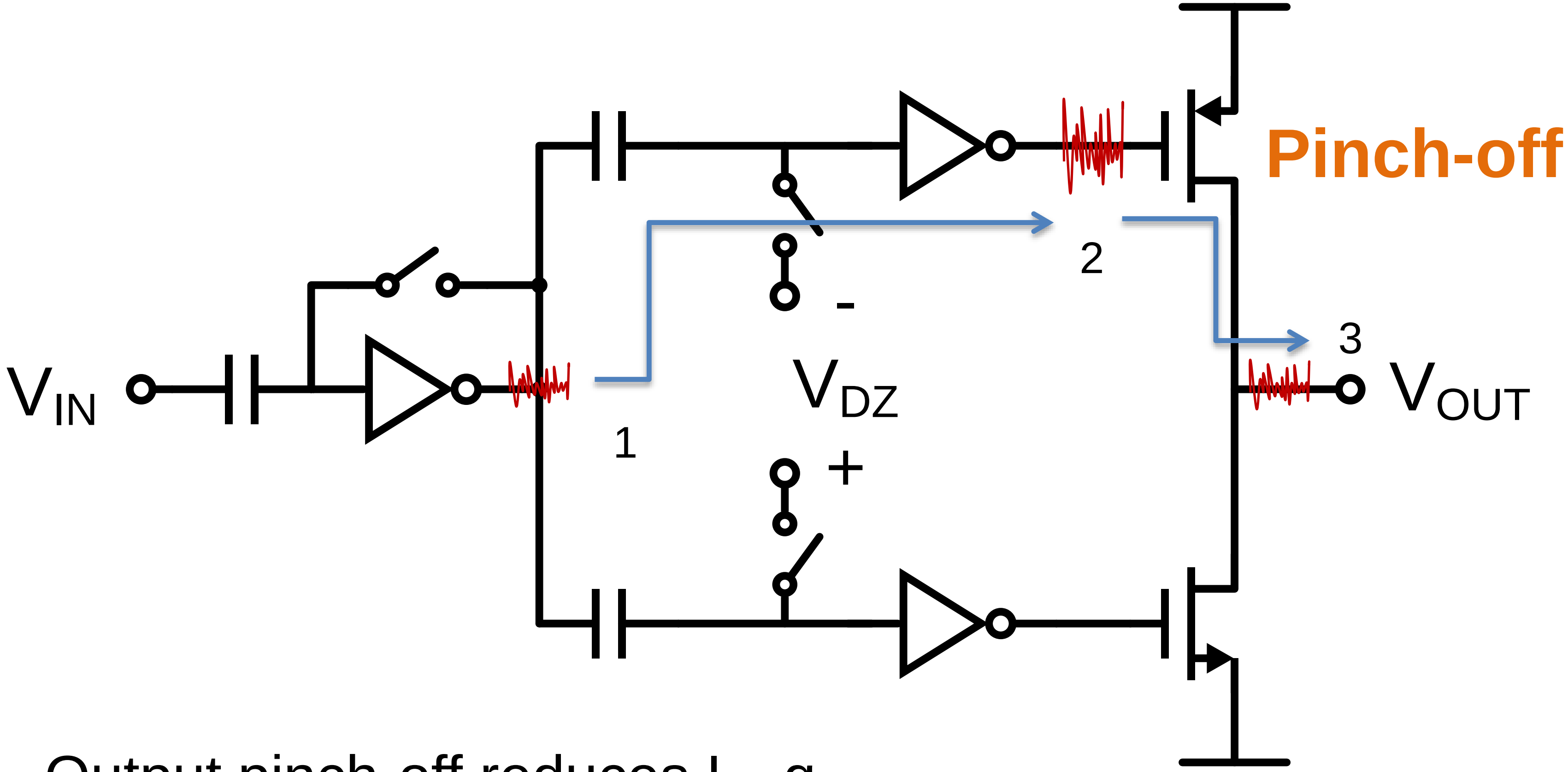


Noise Suppression



- Output pinch-off reduces I_D, g_m
  - Internal noise sources attenuated
- Initial charging noisy → final settling quiet

Noise Suppression



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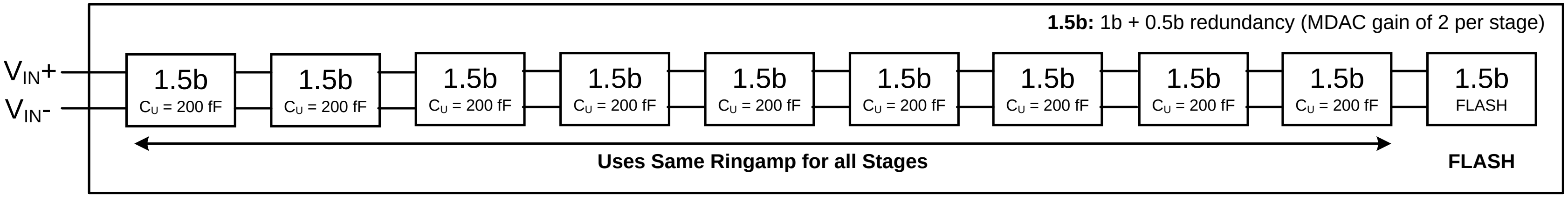
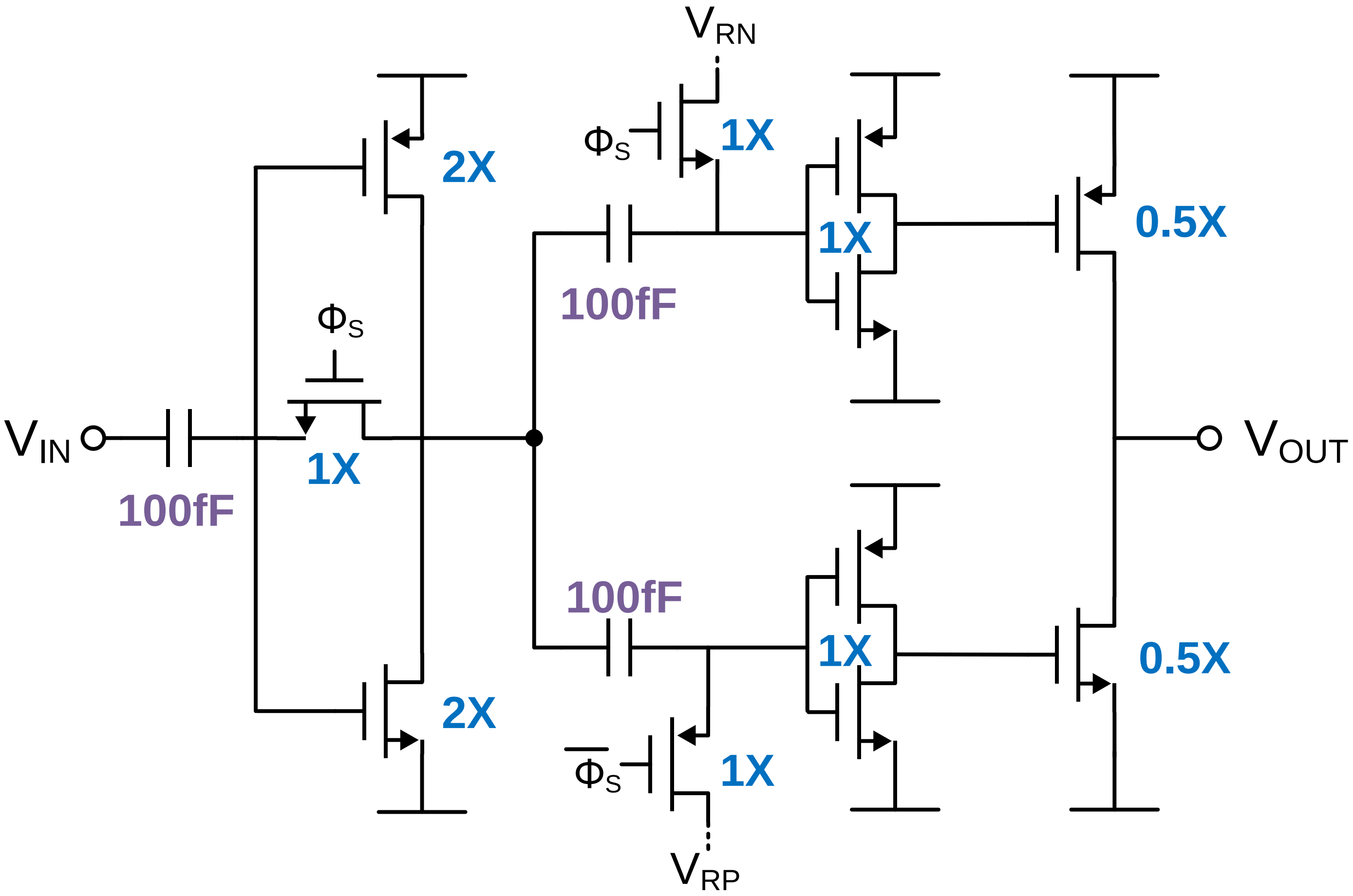
ADC Implementation Details

Structure Overview



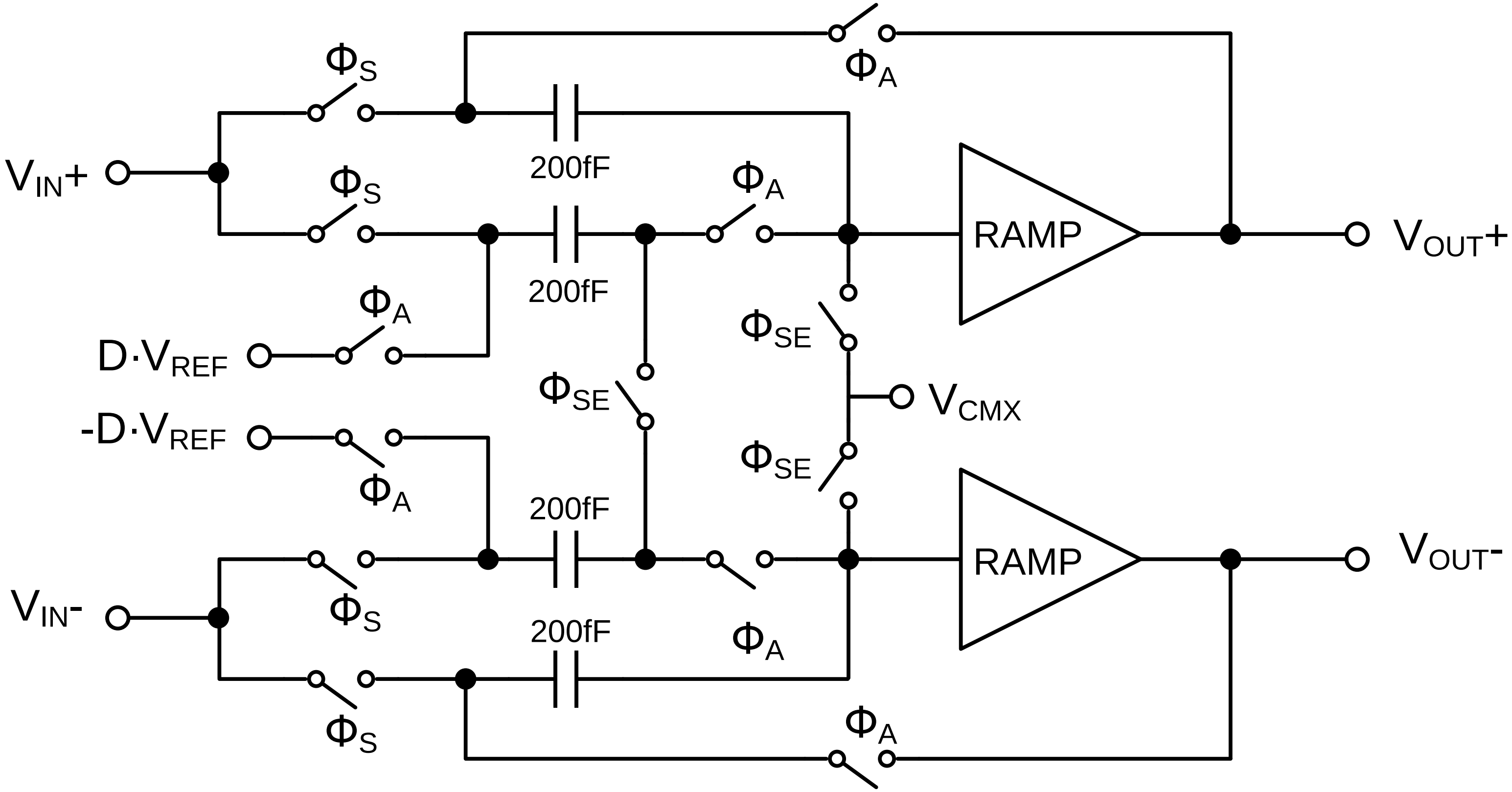
- 10.5b Pipelined ADC
  - 9 identical 1.5b MDAC stages
  - 1.5b Flash
- Simple proof-of-concept built to characterize:
  - Basic functionality
  - Rail-to-rail output swing
  - Noise immunity

Ring amplifier



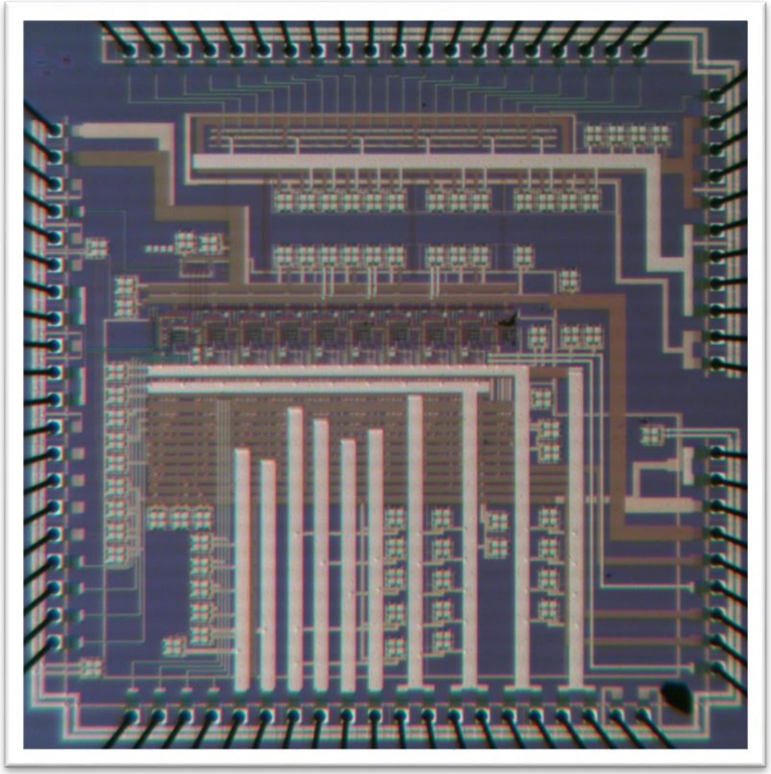
- Very small, very simple, uses minimum size inverters

Float-sampled MDAC

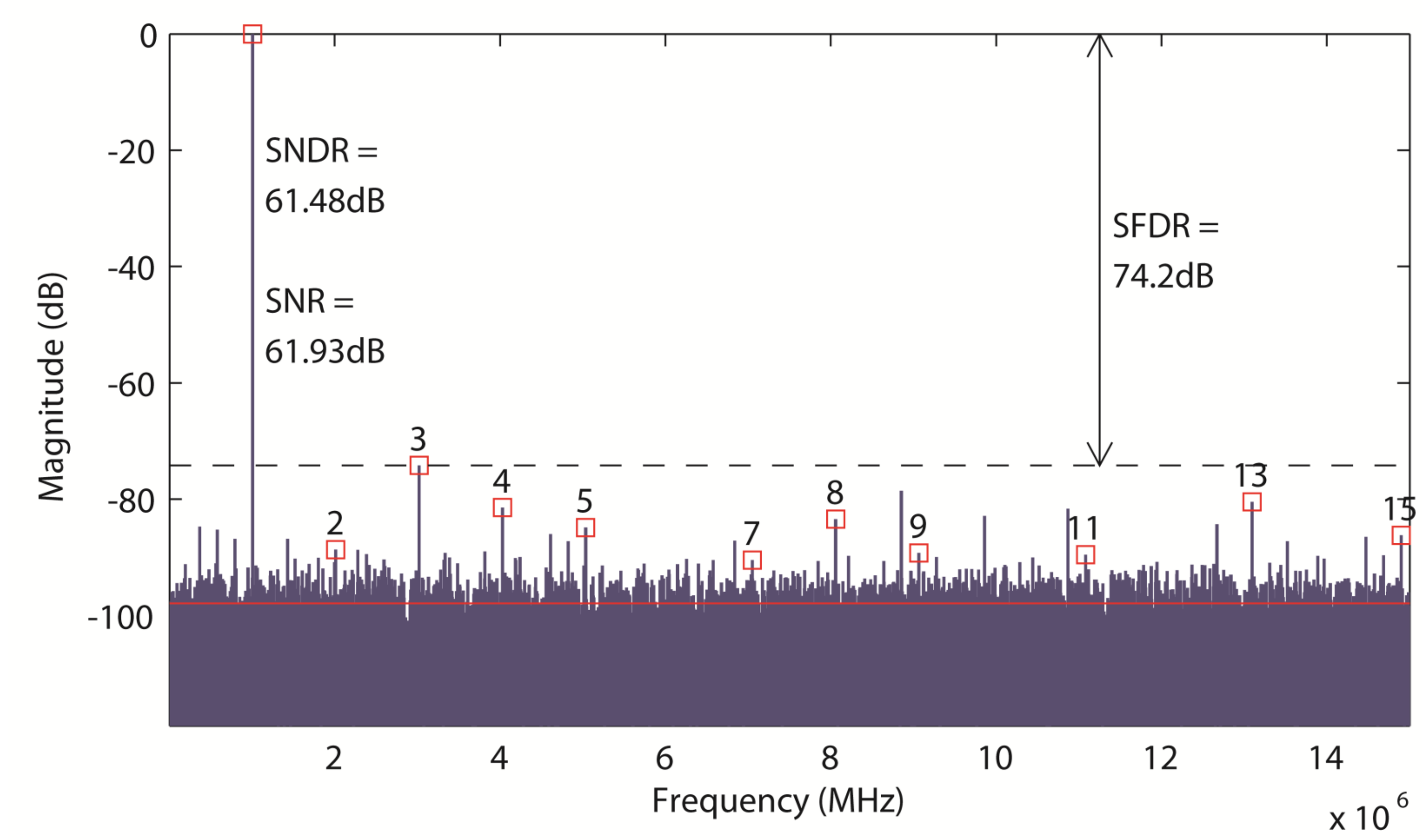


- Differential gain: 2X
- Common-mode gain: 1X

Measurement Results

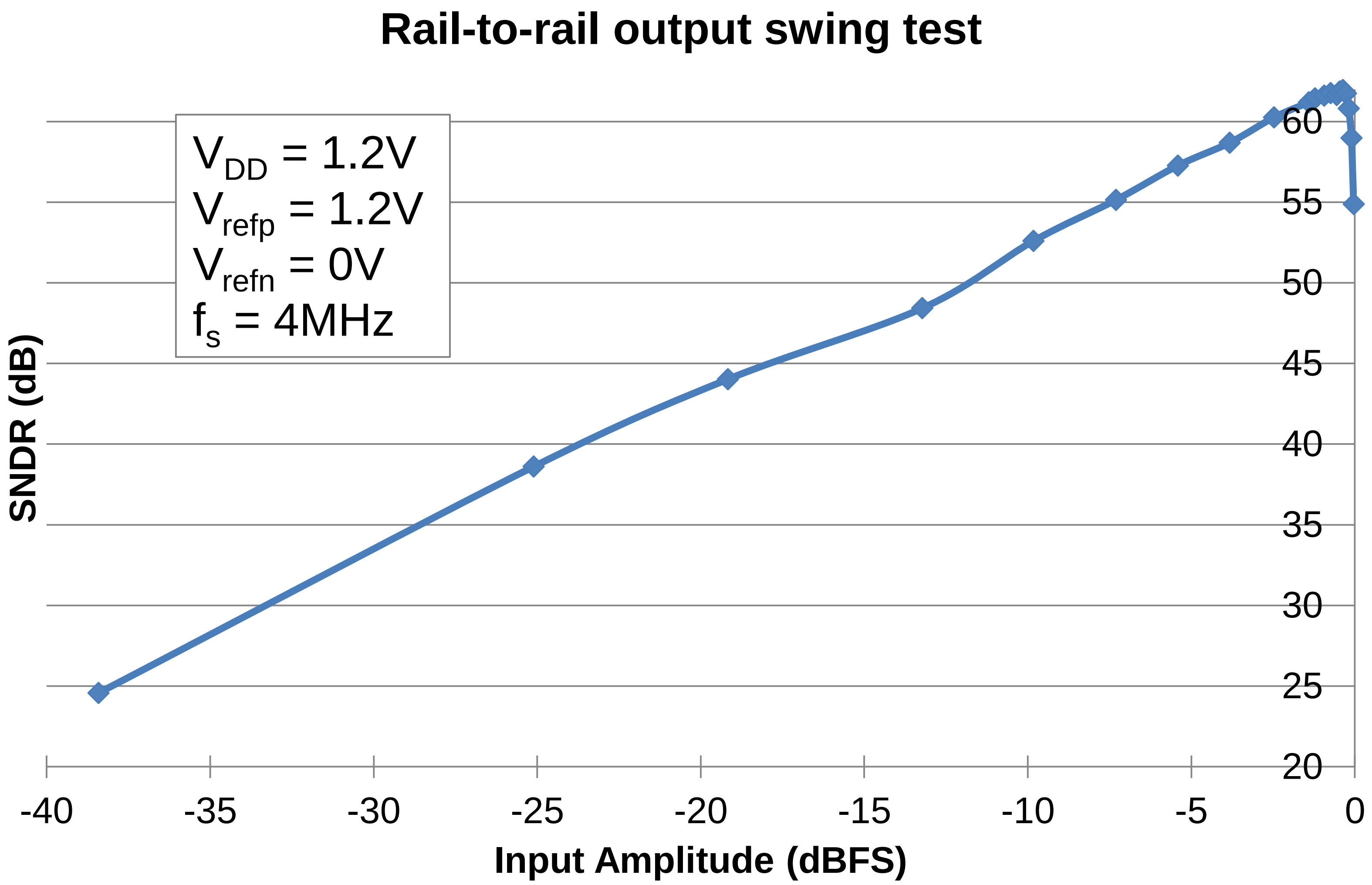


Input Spectrum

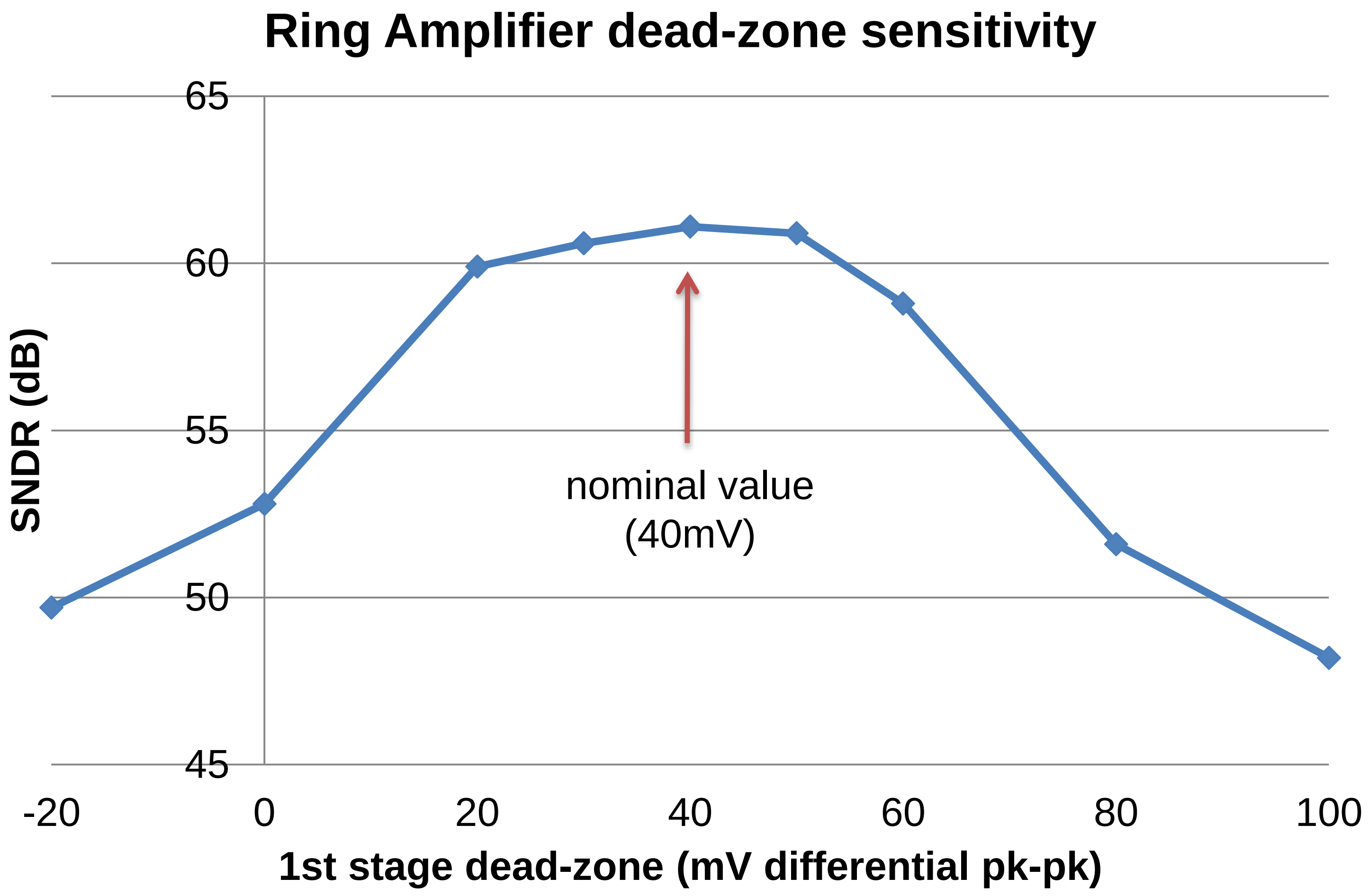


- Limited by quantization noise
- Inherent noise advantage demonstrated

Rail-to-Rail Output Swing Test



Ring Amp Dead-Zone Sensitivity



Performance Summary

Technology	0.18μm 1P4M CMOS
Resolution	10.5 bits
Analog Supply	1.3 V
Sampling rate	30 Msps
ERBW	15 MHz
Input Range	2.2 V pk-pk diff.
SNDR	61.5 dB
SNR	61.9 dB
SFDR	74.2 dB
ENOB	9.9 bits
Total Power	2.6 mW
FoM	90 fJ/c-step

Room for improvement

- Design meant to probe THD, SNR limits of minimum sized ringamp
  - Speed set intentionally low
  - No optimization, stage scaling
  - Ringamps left ‘on’ during sampling phase
  - FoM can easily be improved
- ISSCC 2012 implementation**
  - Speed: 90Msps
  - Power save features: 50% reduction in power

** *B. Hershberg, et al. “Ring Amplifiers for Switched Capacitor Circuits”, ISSCC 2012*

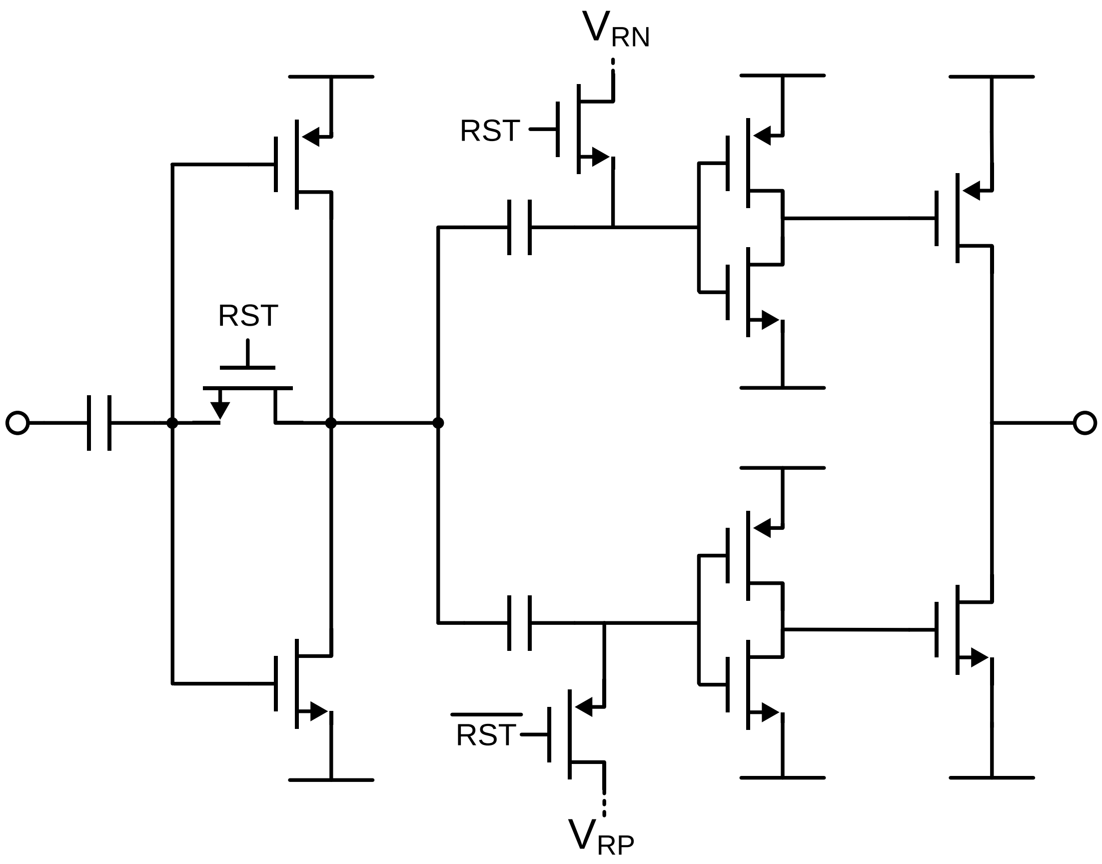
Scalability Test

- Design Challenge:
  - MDAC for 11b pipelined ADC with 10b ENOB
  - 130nm, 90nm, 65nm, 45nm, 32nm

V_{DD}	process defined
SNDR	> 66dB (input referred)
Output Swing	$0.8V_{DD}$
Total Load	800fF
Speed	proportional to $1/L_{min}$
Power	Minimize

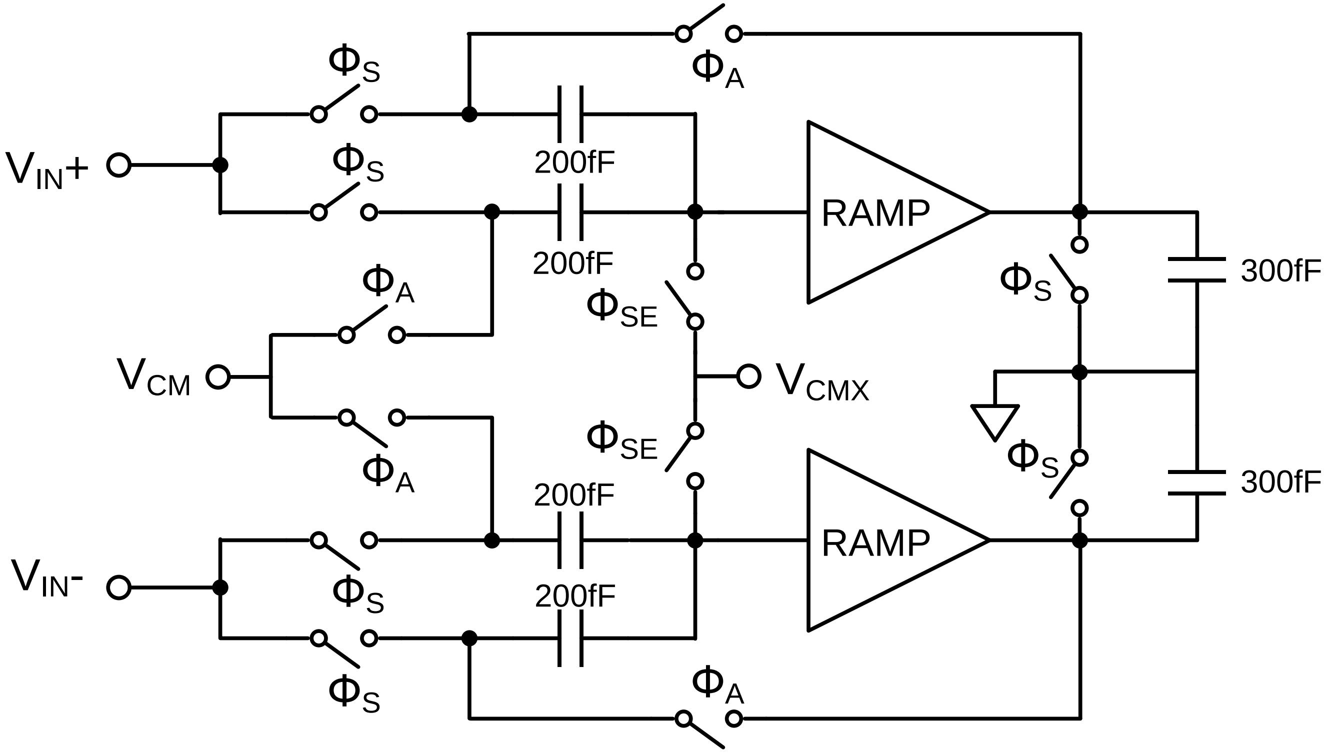
  - ASU predictive technology models [ptm.asu.edu]

Scalability Test



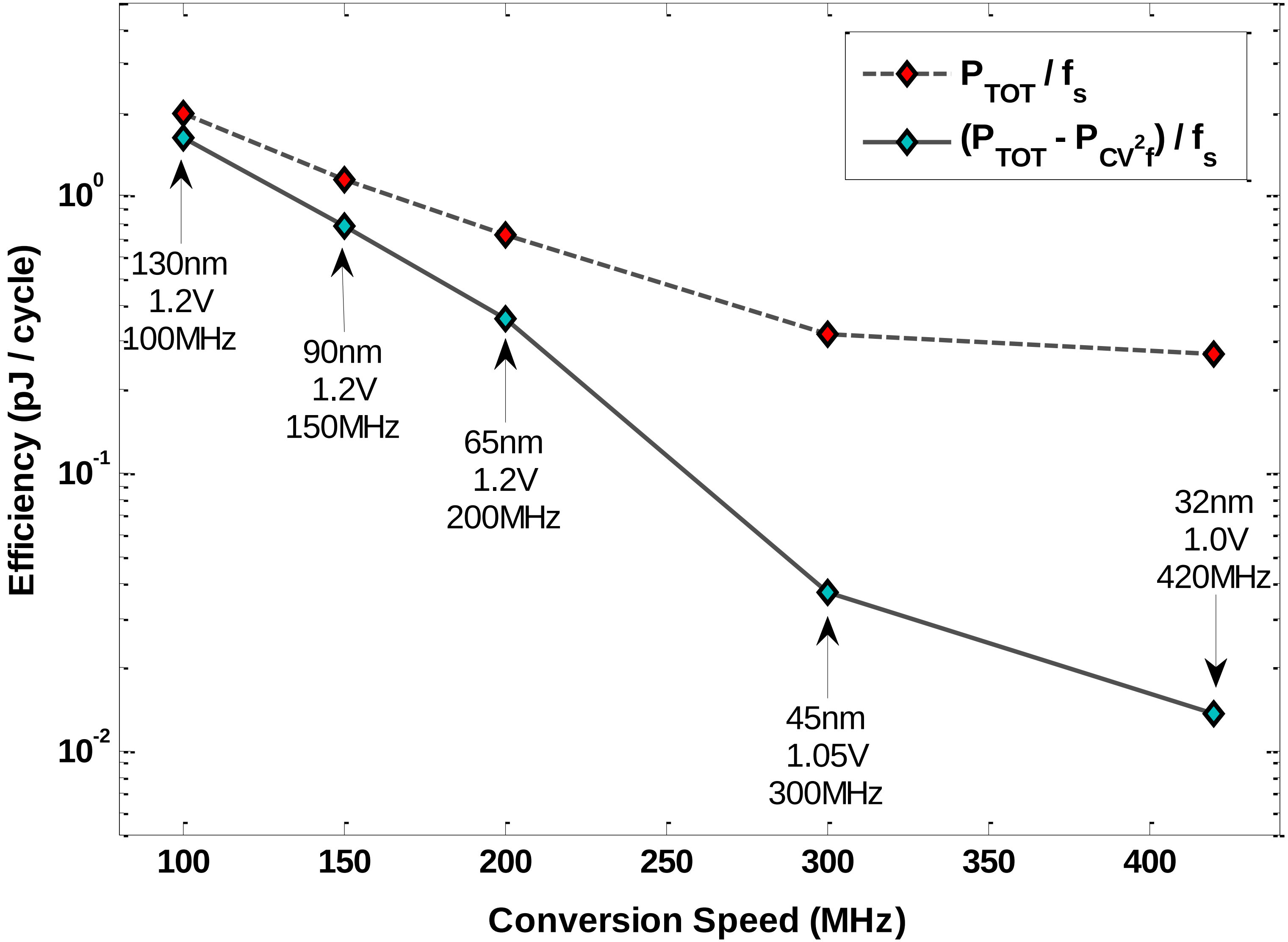
Test Ringamp

Scalability Test



Pesudo-differential Test MDAC

Scalability Test



Conclusion

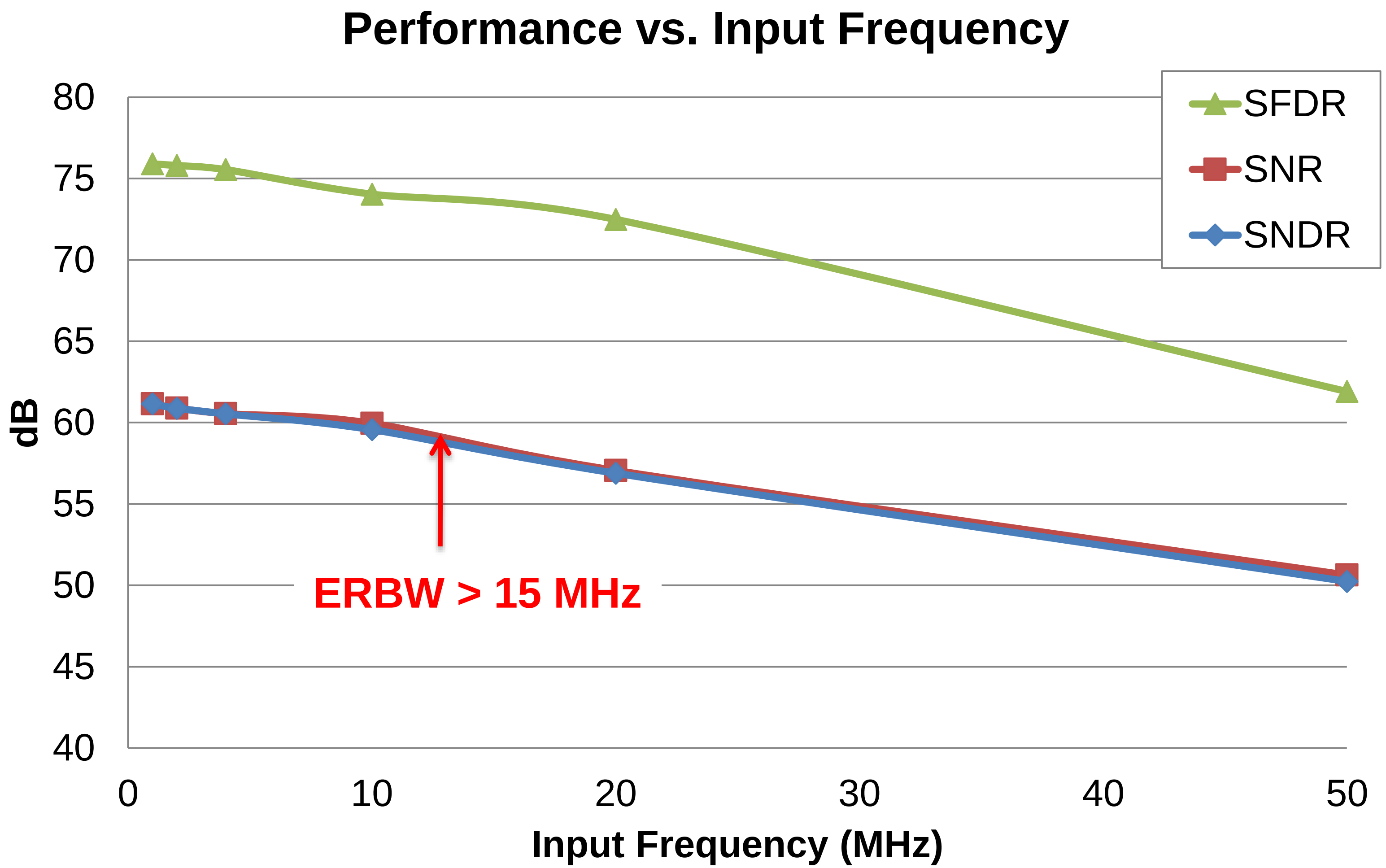
- Ring Amplification
  - High efficiency slew-based charging
  - Rail-to-rail output swing
  - Noise advantage
  - Performance scales with digital process
- Key Concepts
  - Dead-zone
  - V_{OV} pinch-off
  - Dynamic gain adjustment

Thank you for your attention

Additional Slides

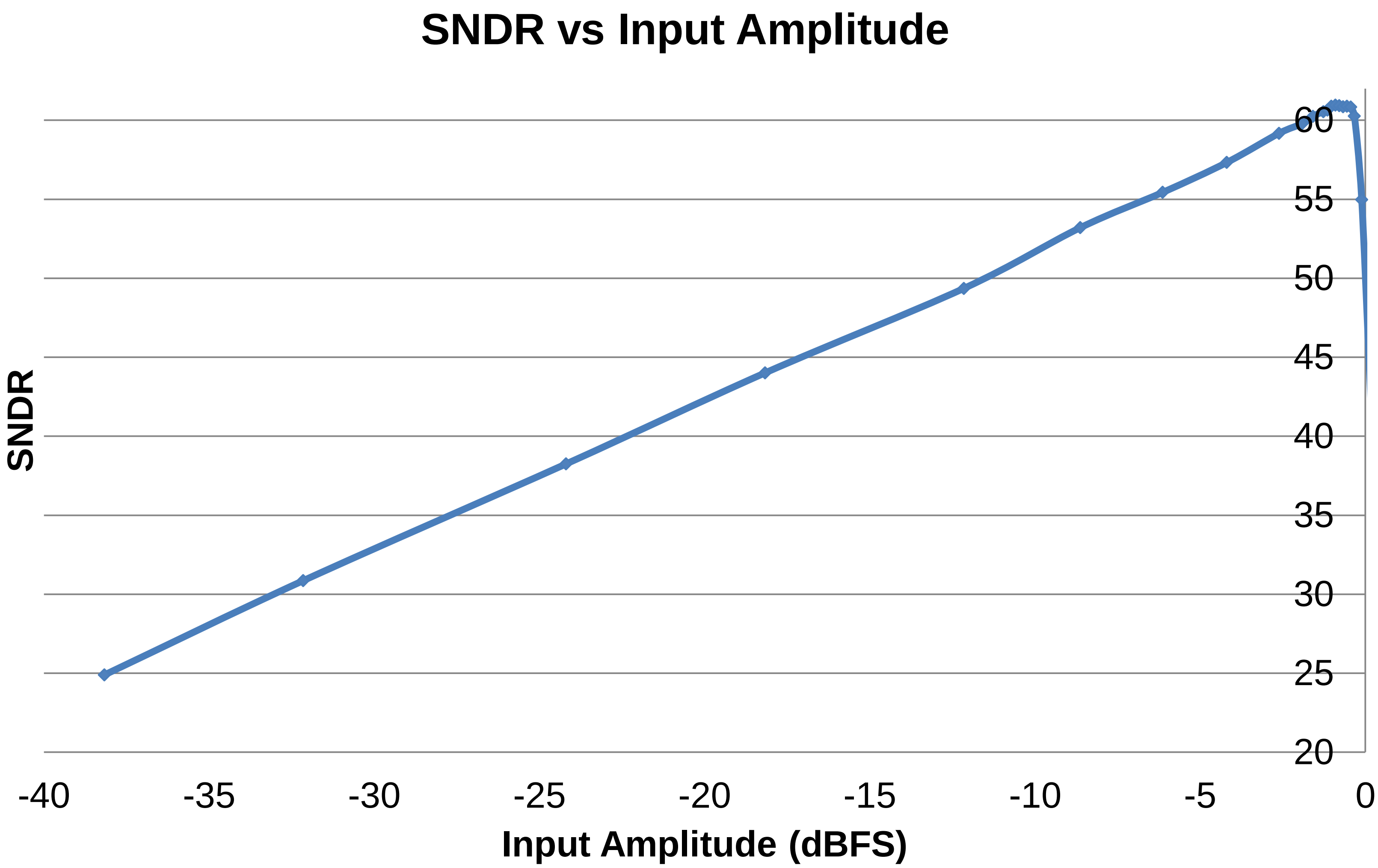
Possibly useful in Q&A afterwards

Performance vs. Input Frequency

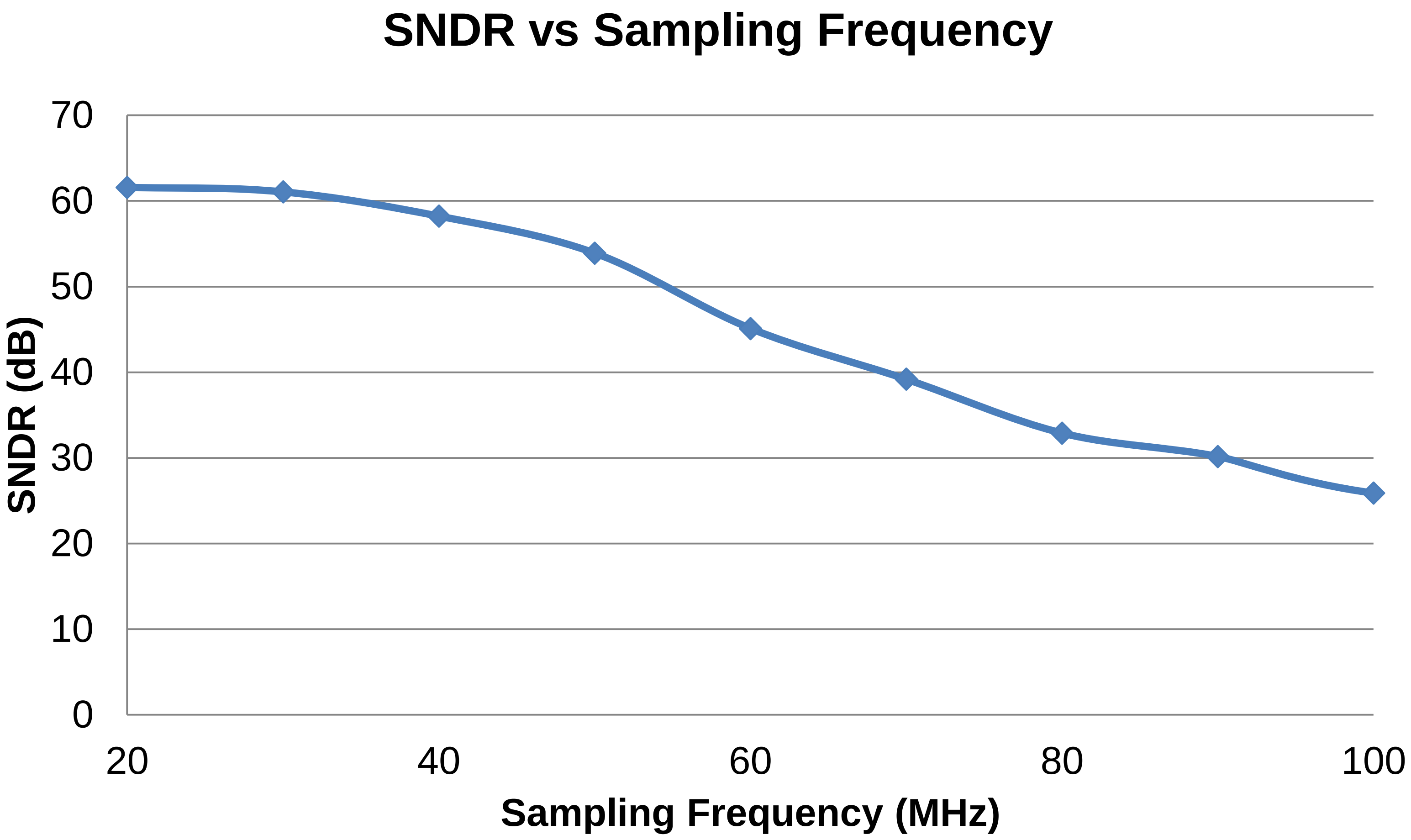


ERBW > 15 MHz

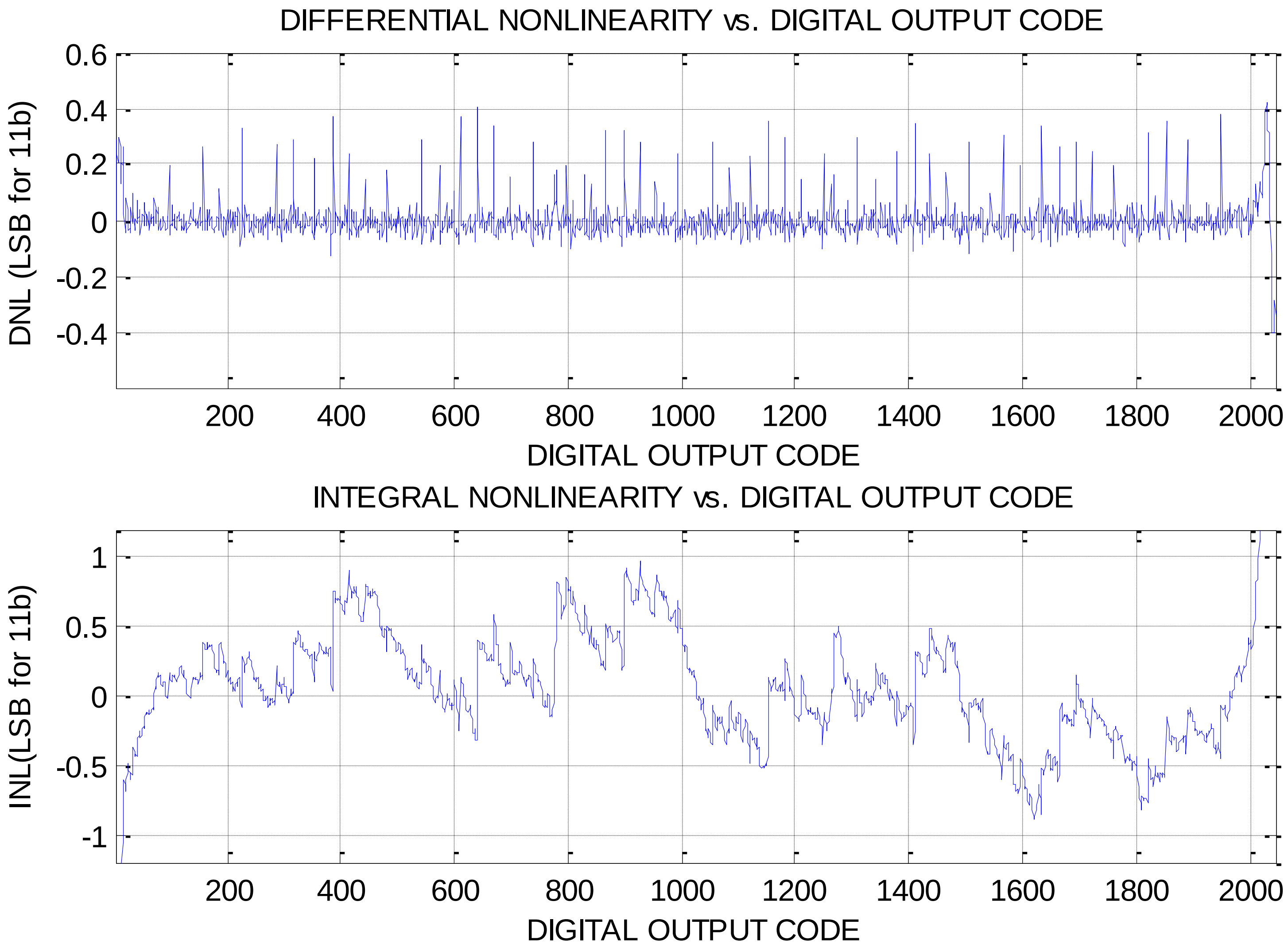
SNDR vs. Input Amplitude



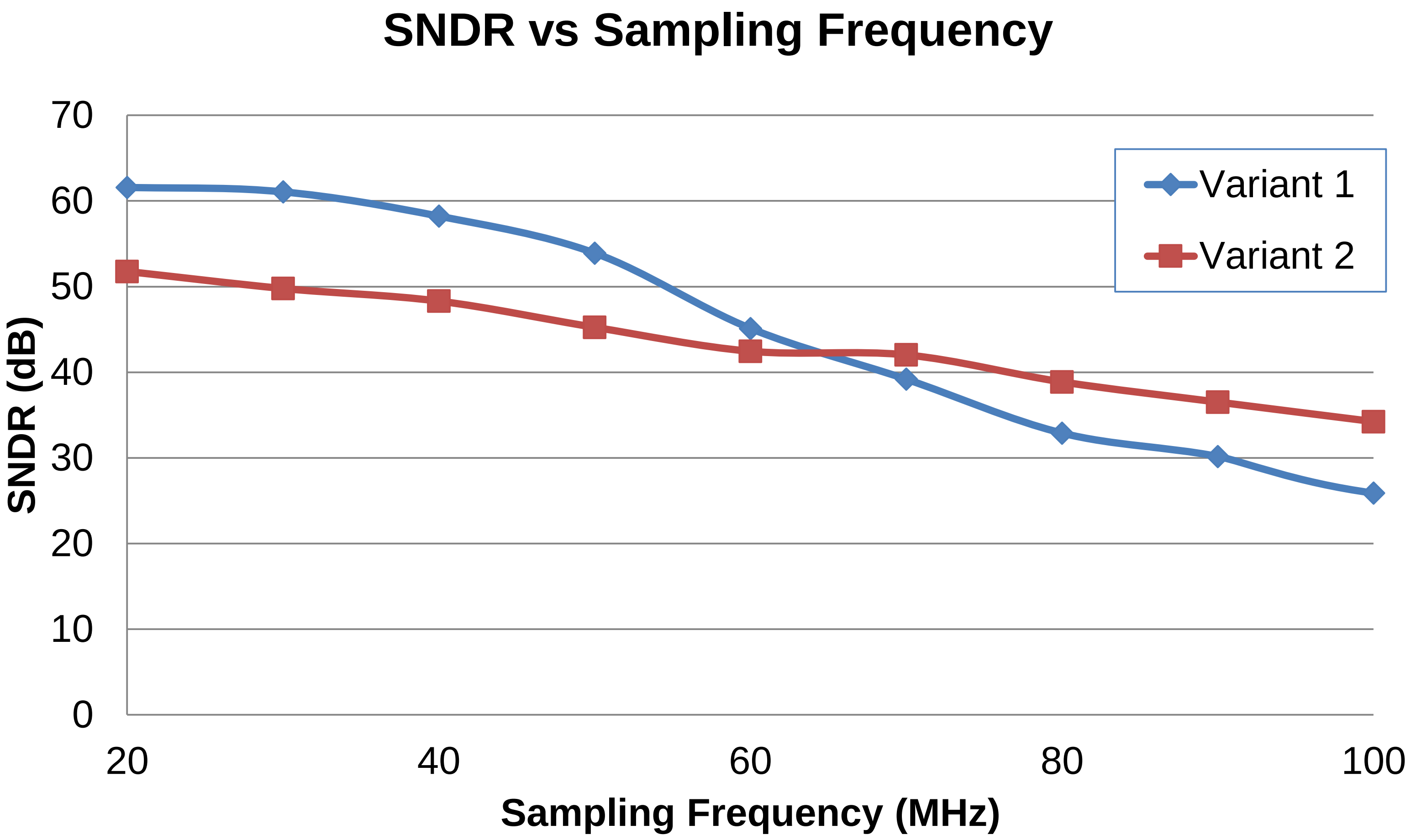
SNDR vs. Sampling Frequency



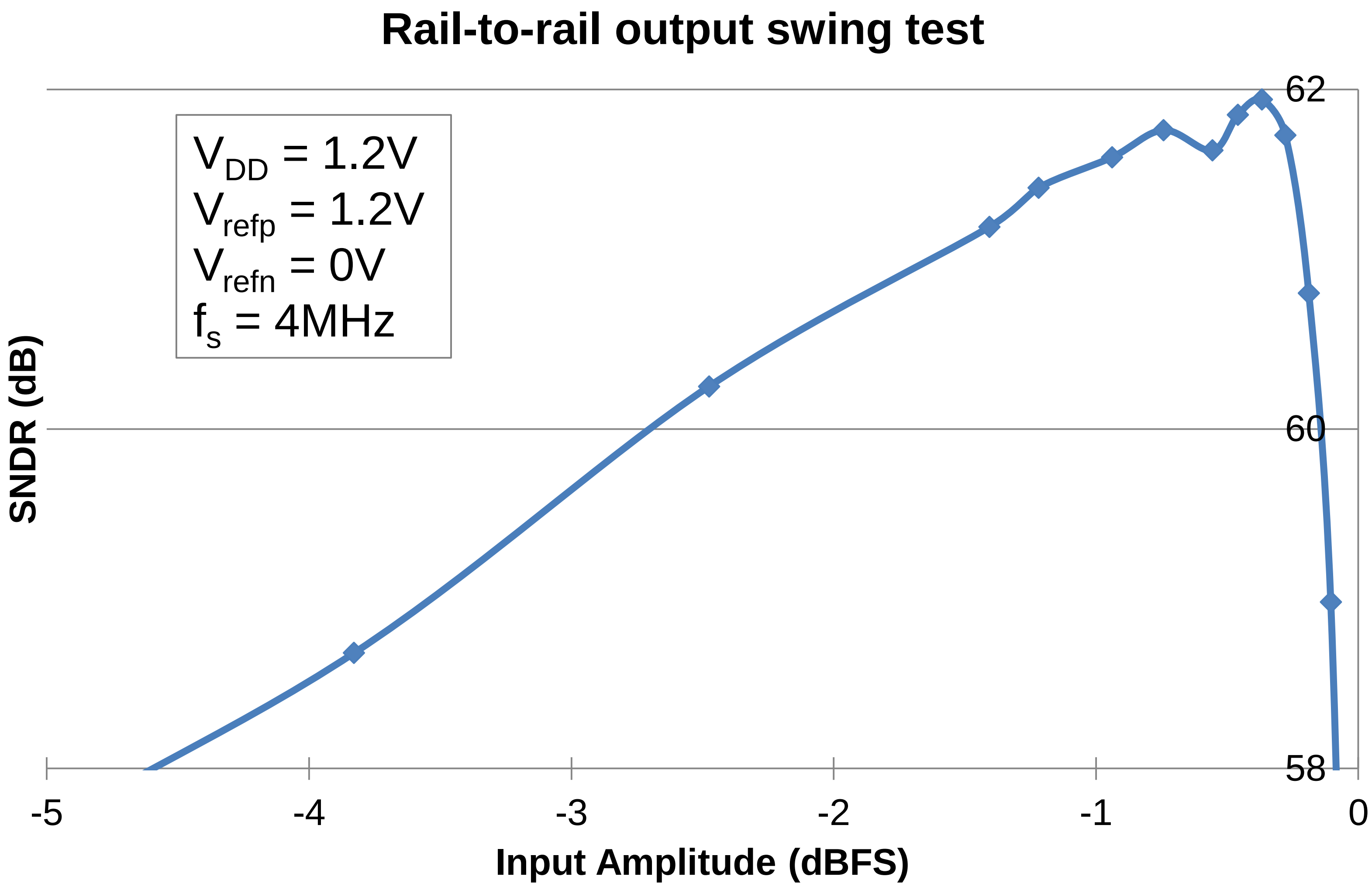
INL / DNL


DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE
DNL (LSB for 11b)
0.6
0.4
0.2
0
-0.2
-0.4
200
400
600
800
1000
1200
1400
1600
1800
2000
DIGITAL OUTPUT CODE
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE
INL(LSB for 11b)
1
0.5
0
-0.5
-1
200
400
600
800
1000
1200
1400
1600
1800
2000
DIGITAL OUTPUT CODE

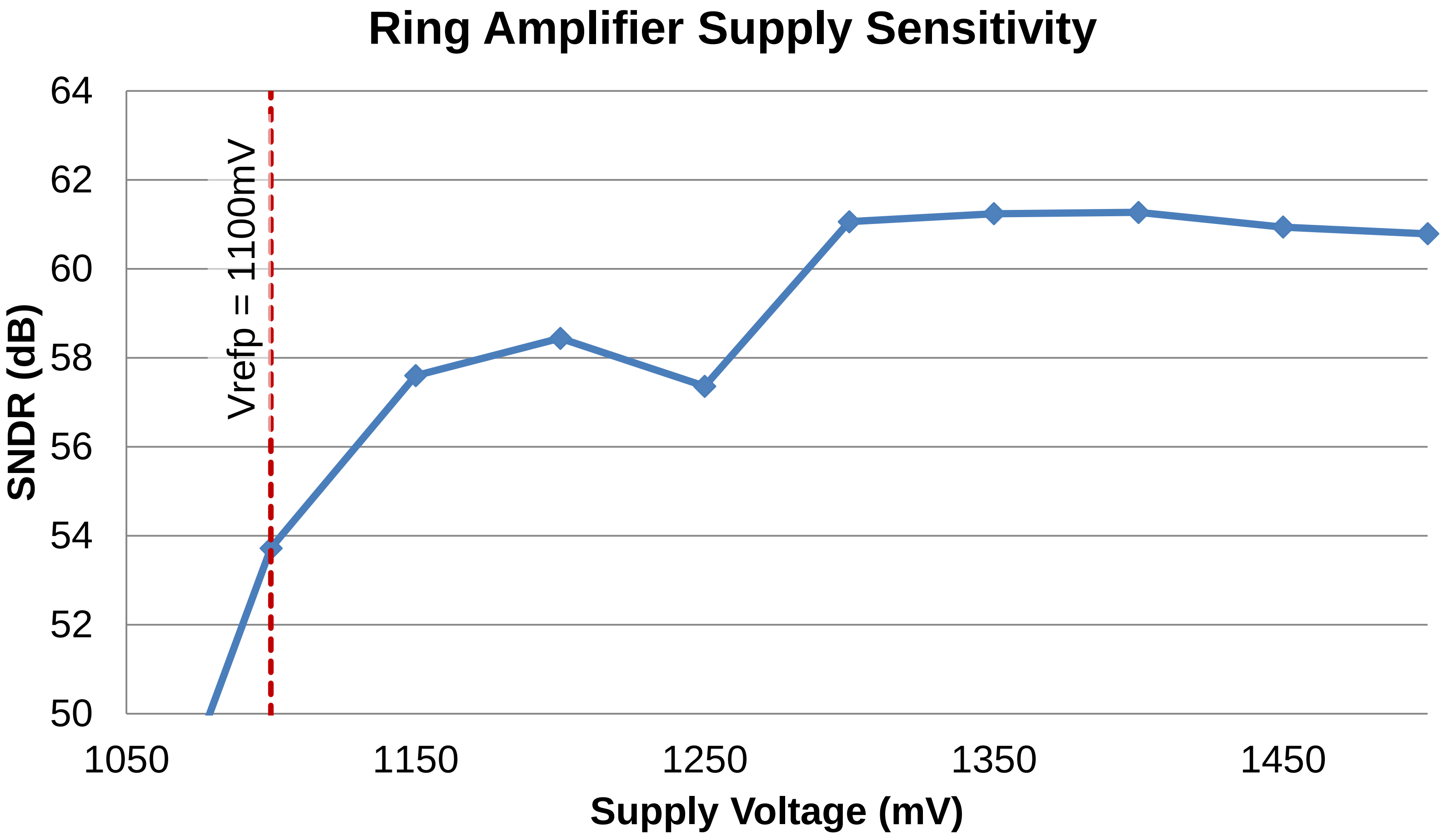
SNDR vs. Sampling Frequency



Rail-to-Rail Output Swing



Ring Amp Supply Sensitivity



Supply Current vs. Dead-zone