A 9.1-12.7 GHz VCO in 28nm CMOS with a Bottom-Pinning Bias Technique for Digital Varactor Stress Reduction

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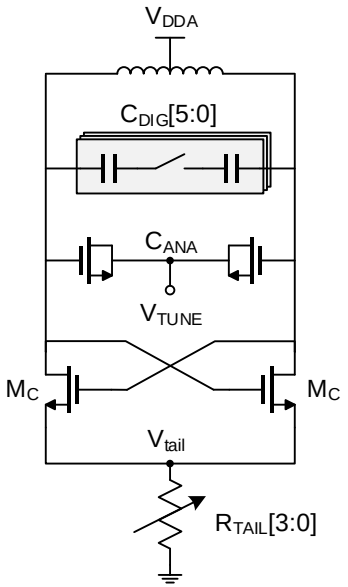
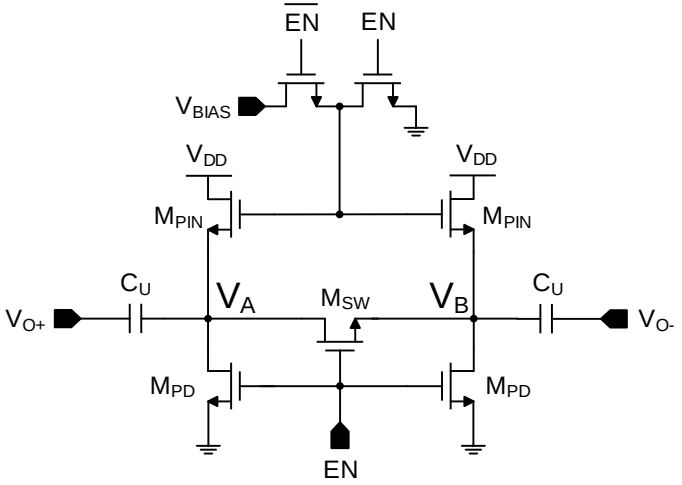
IN THIS TALK

- Design challenges of VCOs in nanoscale CMOS
- A new digital varactor cell
- Class B wide tuning range VCO in 28nm



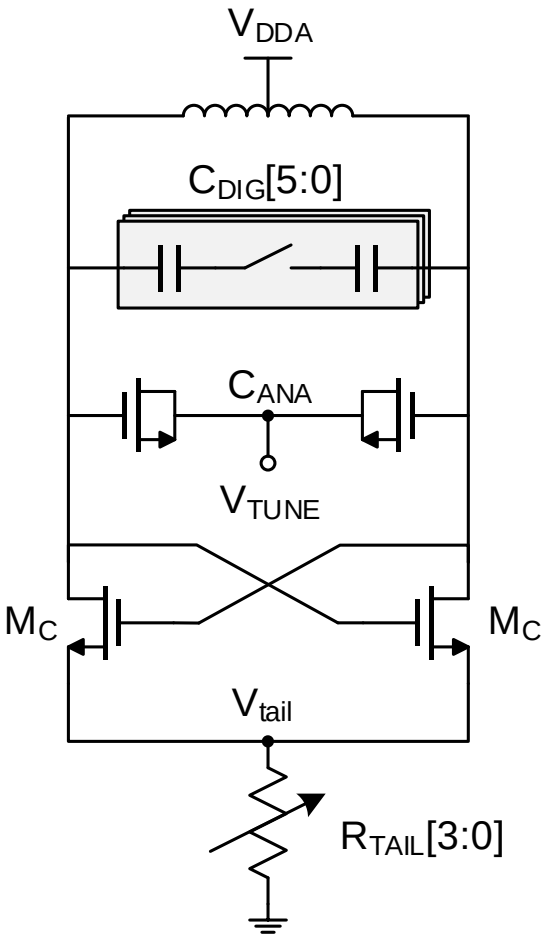
Class-B VCO



New digital varactor cell

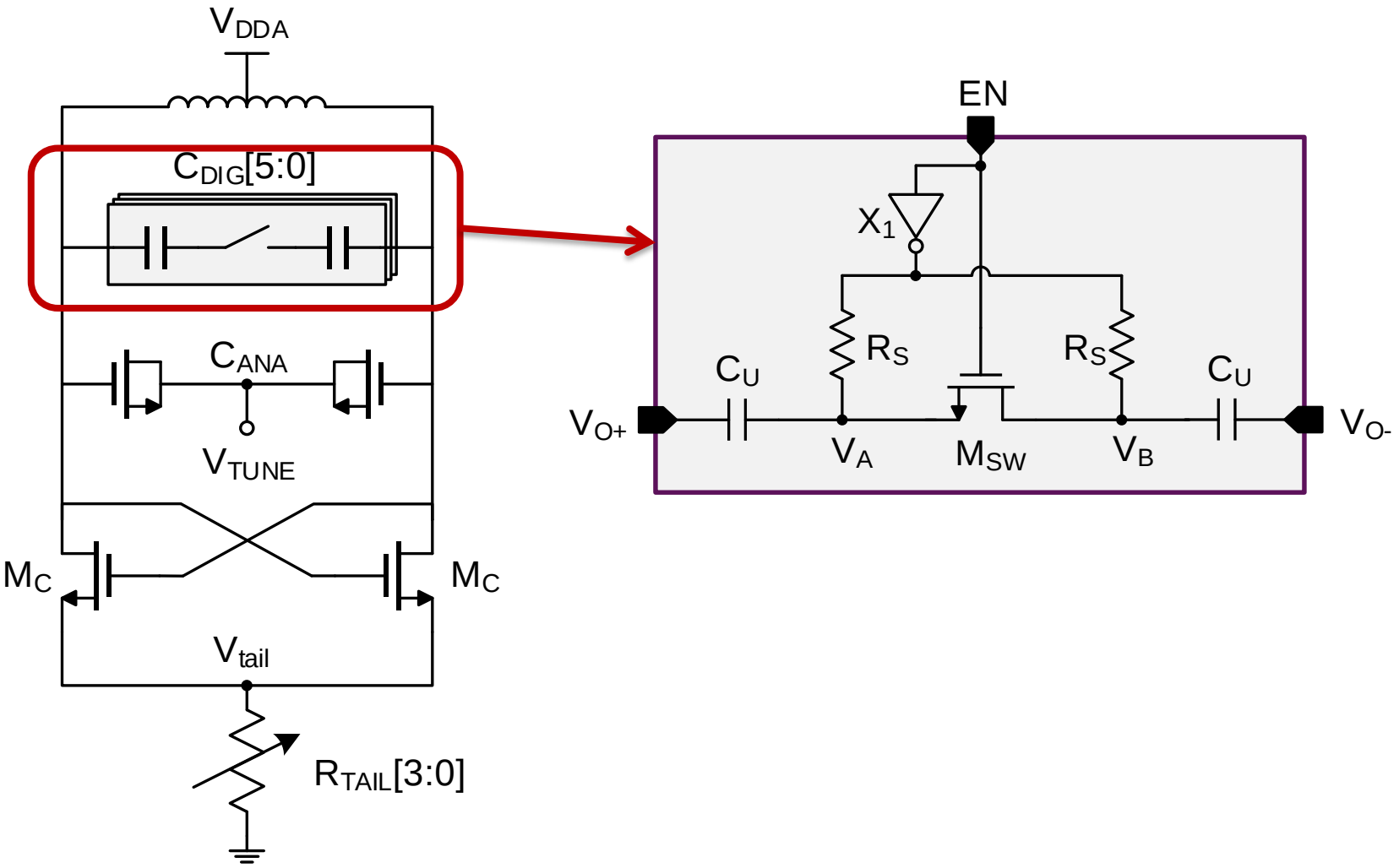
A POPULAR ARCHITECTURE

- Wide tuning range class-B VCO
  - Broad tuning for software defined radio
  - R_{TAIL}: power/noise optimization
- Coarse digital cap bank
  - Switched capacitor cells
  - Controlled by Frequency Synthesizer
- Fine analog cap cell
  - Accumulation mode varactor
  - Controlled directly by V_{TUNE} of PLL

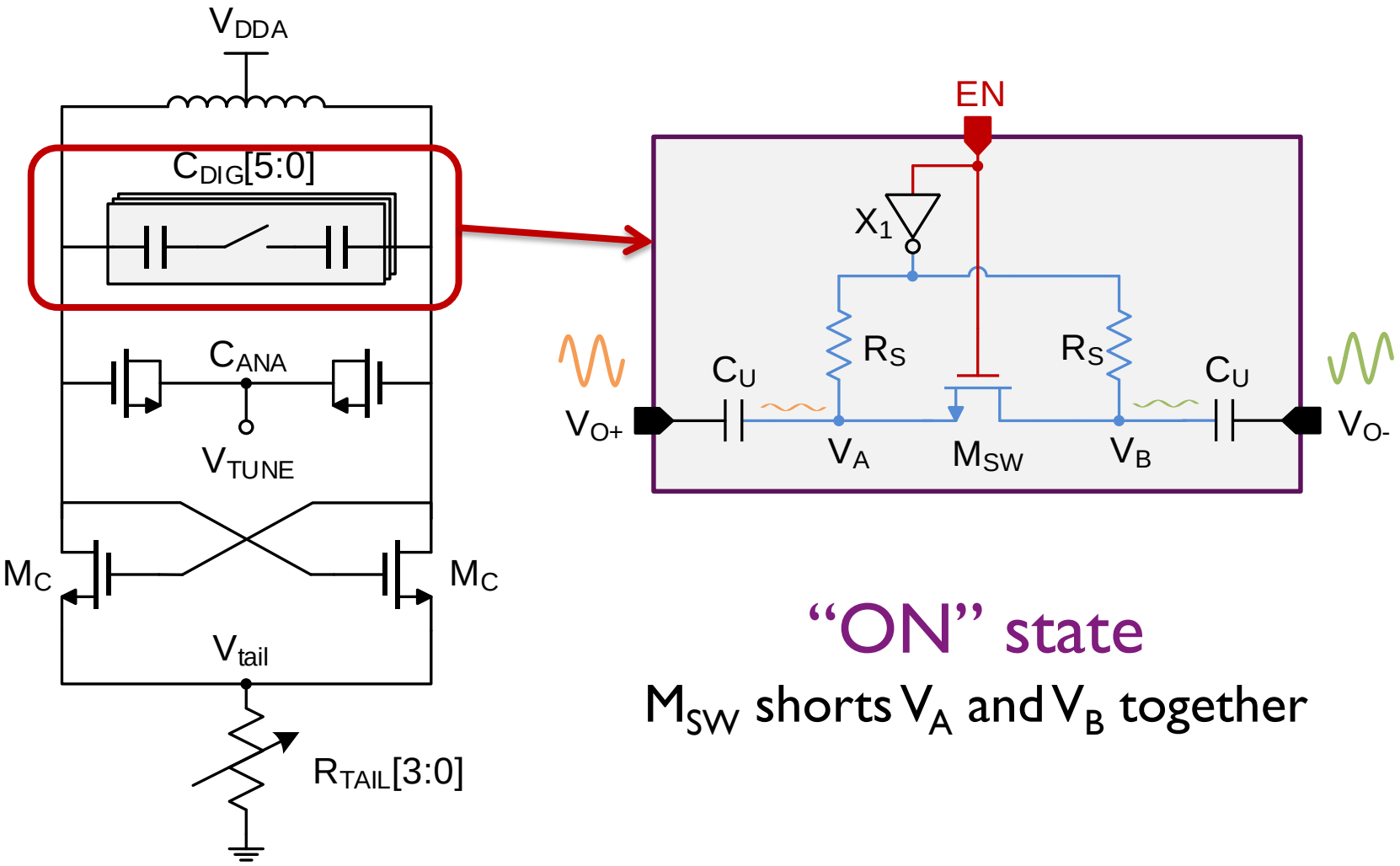


Andreani, JSSC, July 2011

CONVENTIONAL CAP CELL



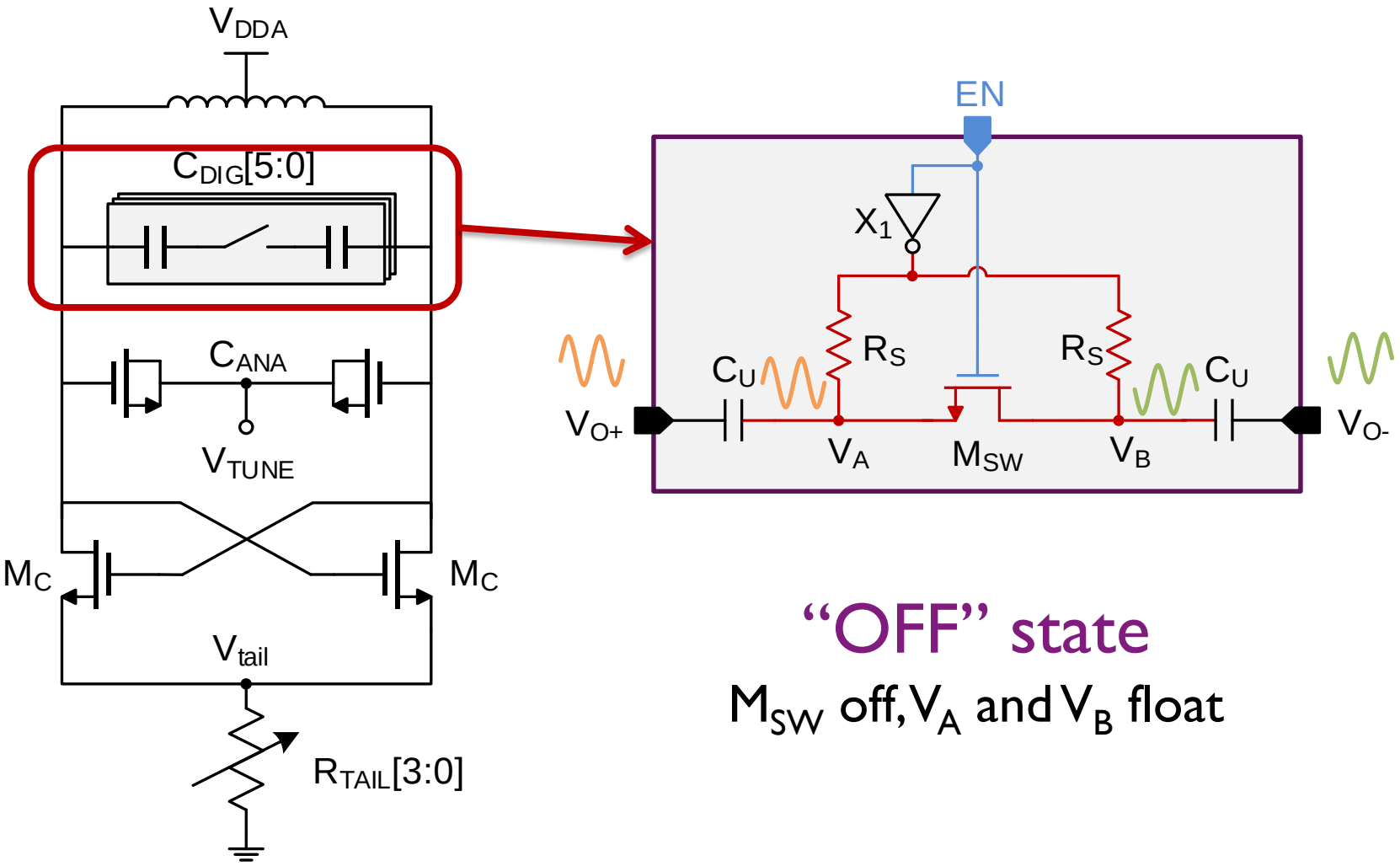
CONVENTIONAL CAP CELL



"ON" state

M_{SW} shorts V_A and V_B together

CONVENTIONAL CAP CELL

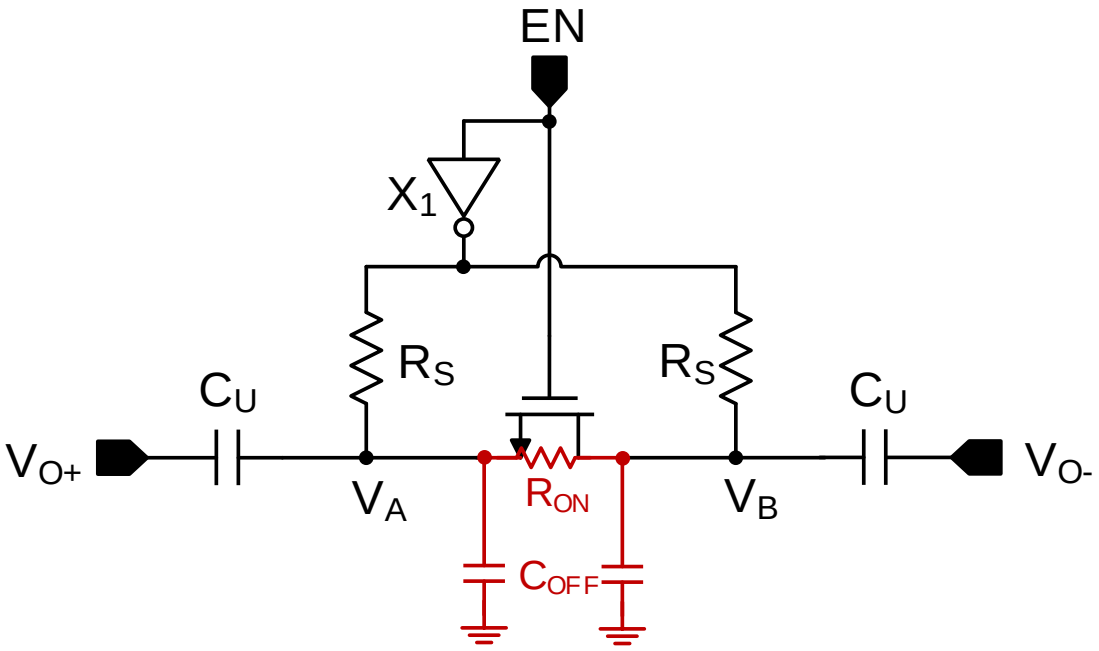


"OFF" state

M_{SW} off, V_A and V_B float

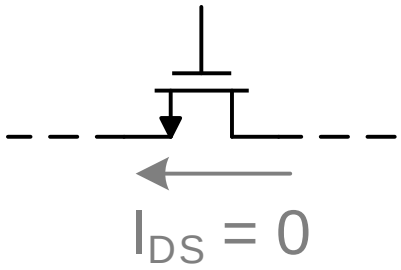
ADVANTAGES OF NANOSCALE

- R_{ON}/C_{OFF} switch scaling advantage
  - Wider tuning range of VCO
  - Better capacitor on-state Q



STRESS IN NANOSCALE

- Voltage stress above native V_{DD} with thin oxide?
  - ON state: no problem!
  - OFF state: possible (with limits)

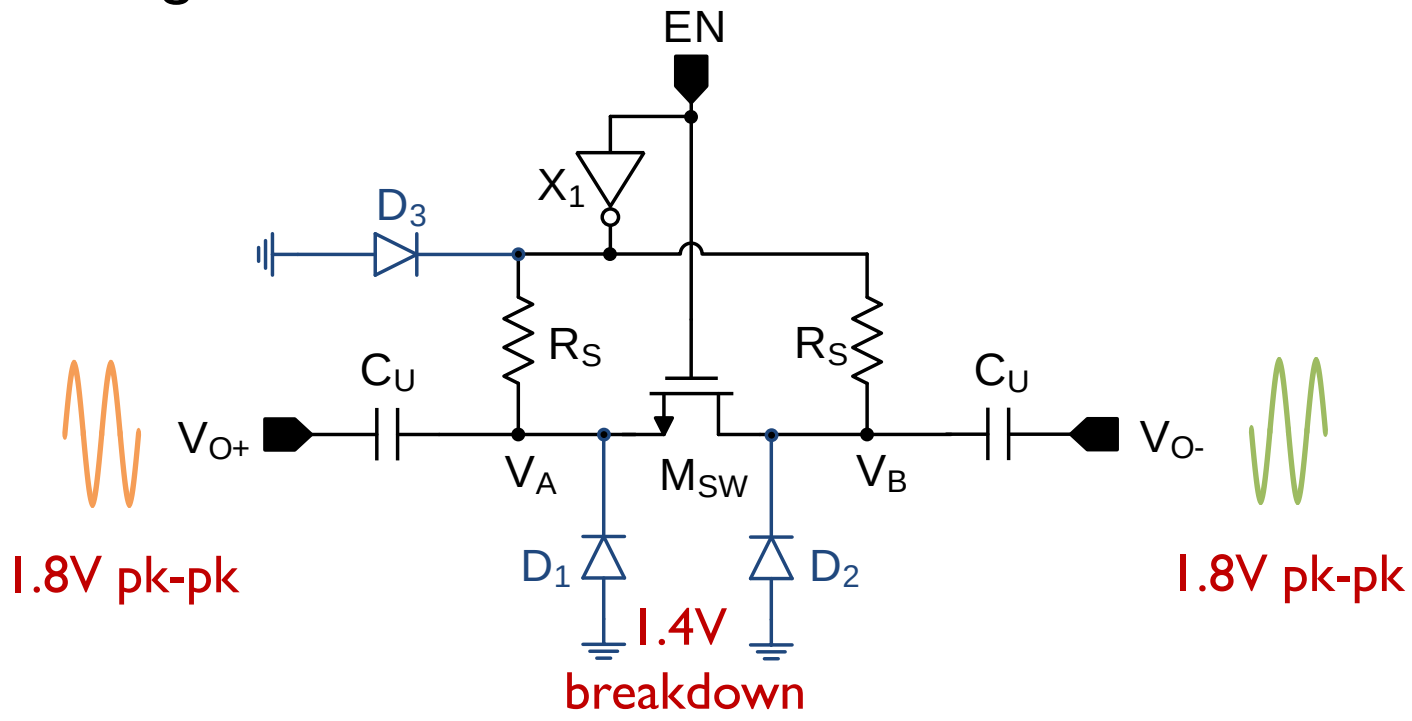


~~Impact ionization!!~~
Gate oxide breakdown
Drain-source punch-through

- Some amount of gate oxide stress is OK

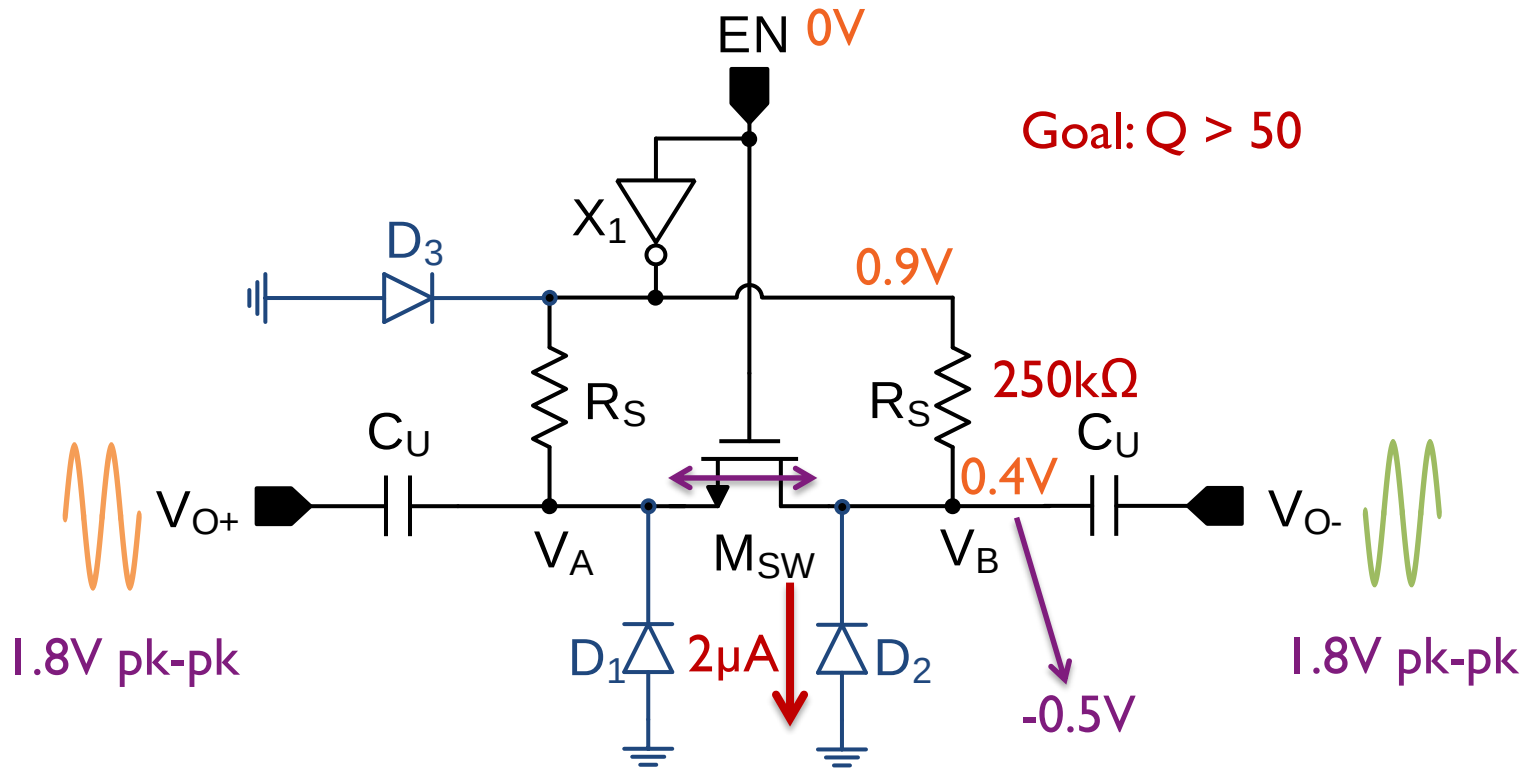
JUNCTION DIODES IN 28NM

- Intrinsic transistor junction diodes
- Reverse-bias current begins at ~1.4V
  - Depends on doping flavor (ulvt, lvt, stdvt, hvt, …)
- Degrades off-state Q



JUNCTION DIODES IN 28NM

- Diode leakage causes common-mode droop
- Common-mode droop can turn on M_{SW}!



DESIRED PROPERTIES

- Minimize oxide stress
- Minimize diode leakage

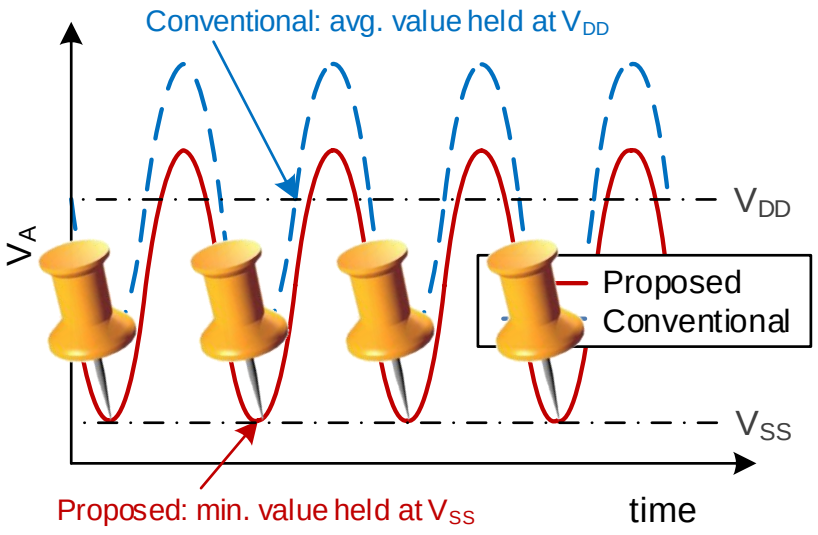
Minimize peak voltage
(upper constraint)

- Q gracefully degrades in the presence of diode leakage

Never drop below min voltage
(lower constraint)

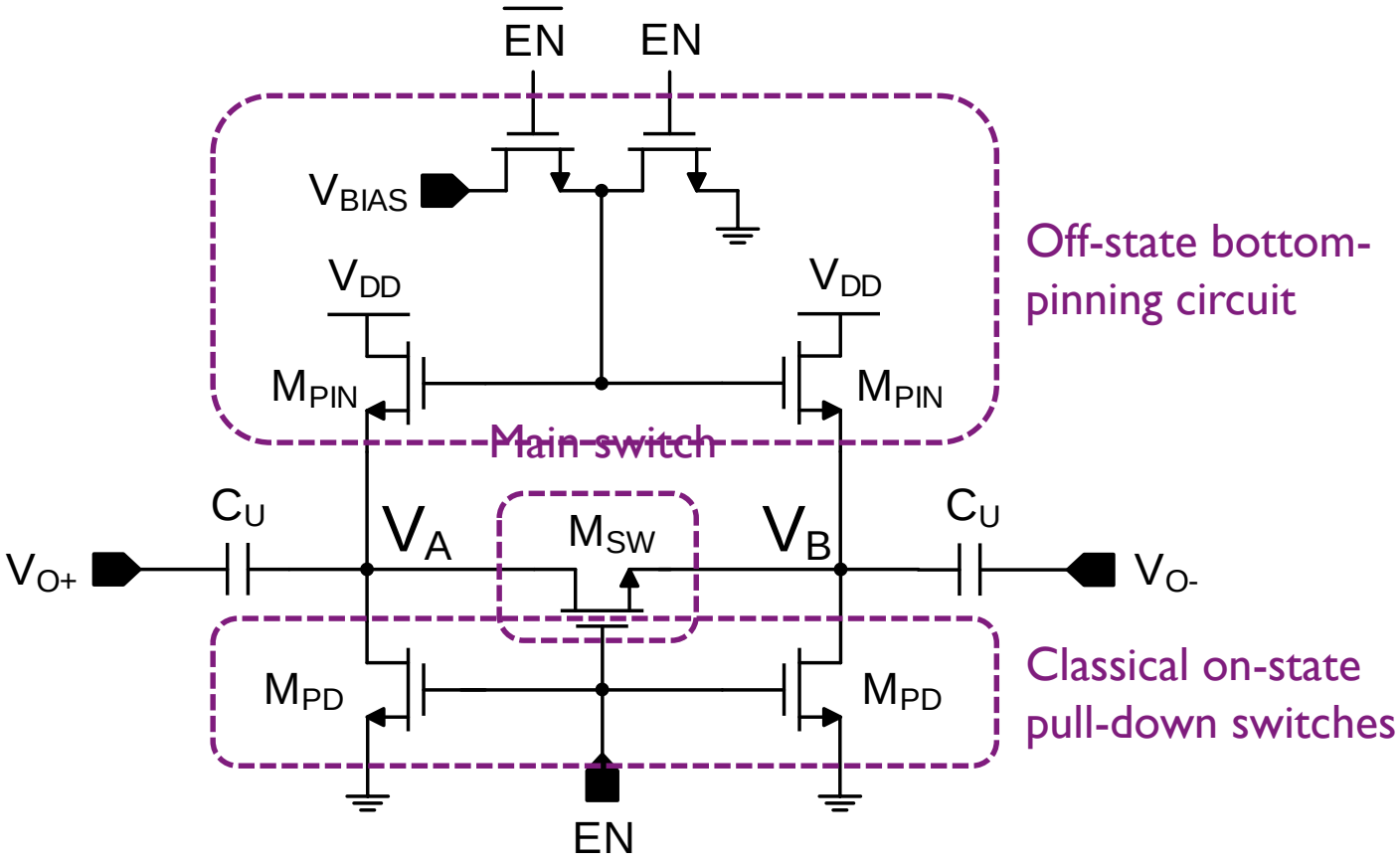
THE OPTIMAL SOLUTION

Transient VCO waveform
(seen at V_A or V_B in off-state)

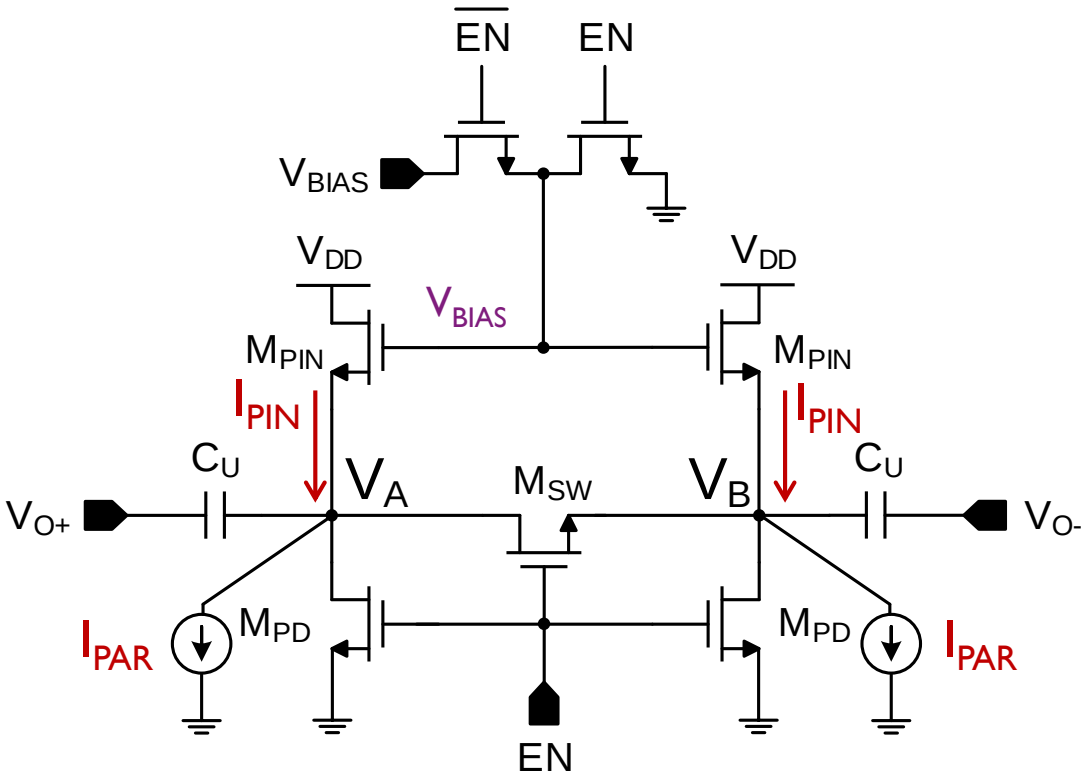


- Old: Average-value referenced
- New: Min-value referenced
- "Bottom Pinning"

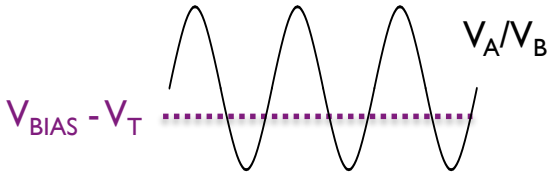
PROPOSED CELL



PRINCIPLE OF OPERATION

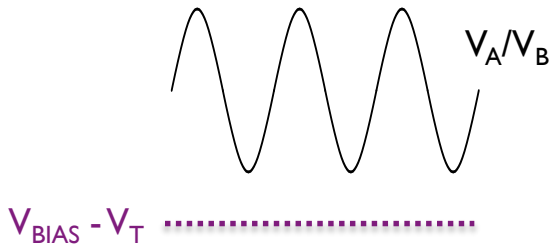


Case 1: V_A (or V_B) too low



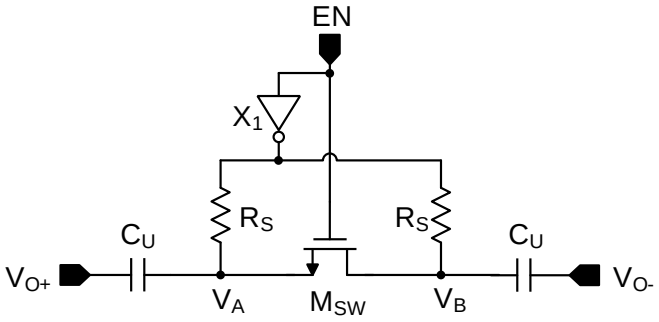
$I_{PIN} > I_{PAR}$

Case 2: V_A (or V_B) too high

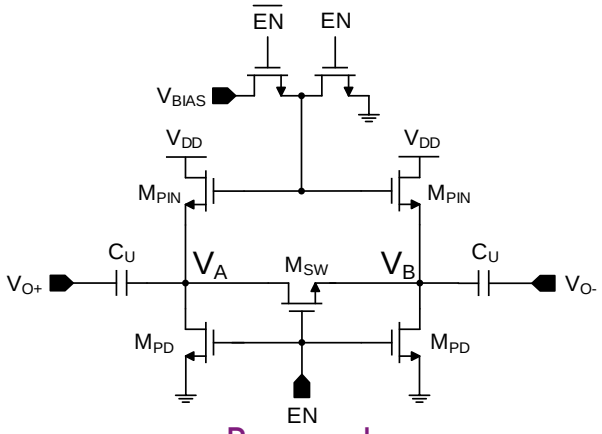


$I_{PIN} < I_{PAR}$

OPTIMAL OFF-STATE Q

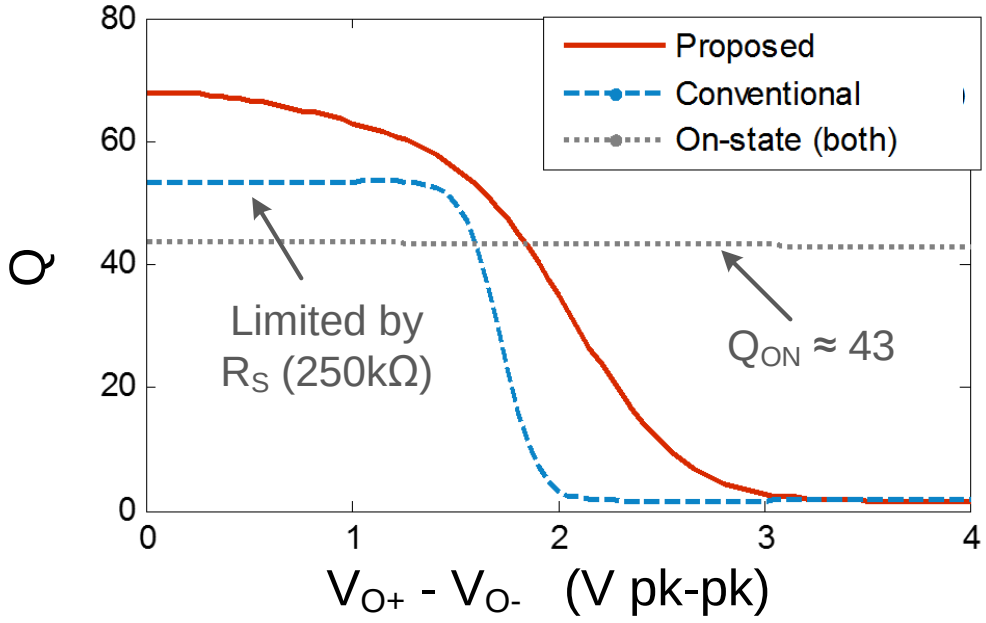


Conventional

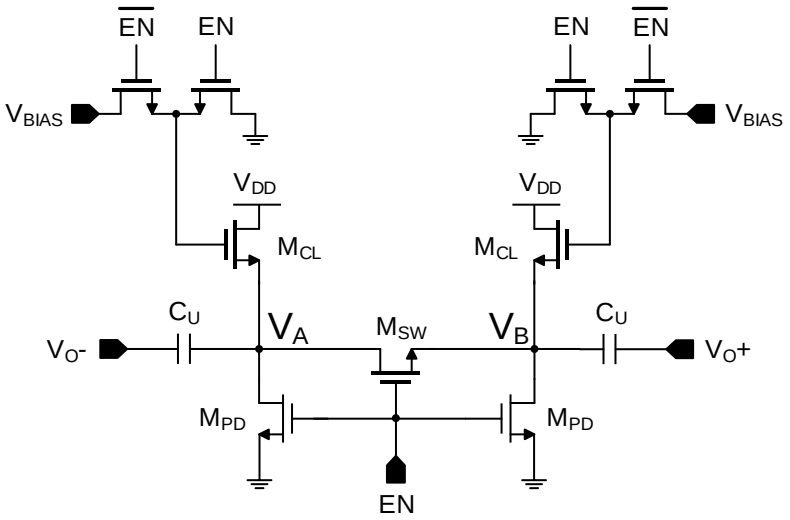


Proposed

- DC current equilibrium at V_A & V_B *always* maintained

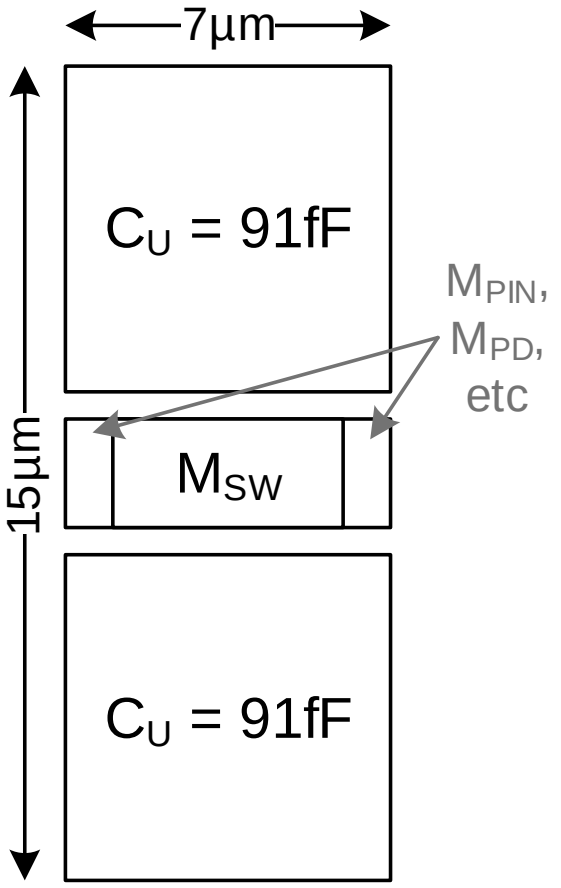


UNIT CELL LAYOUT



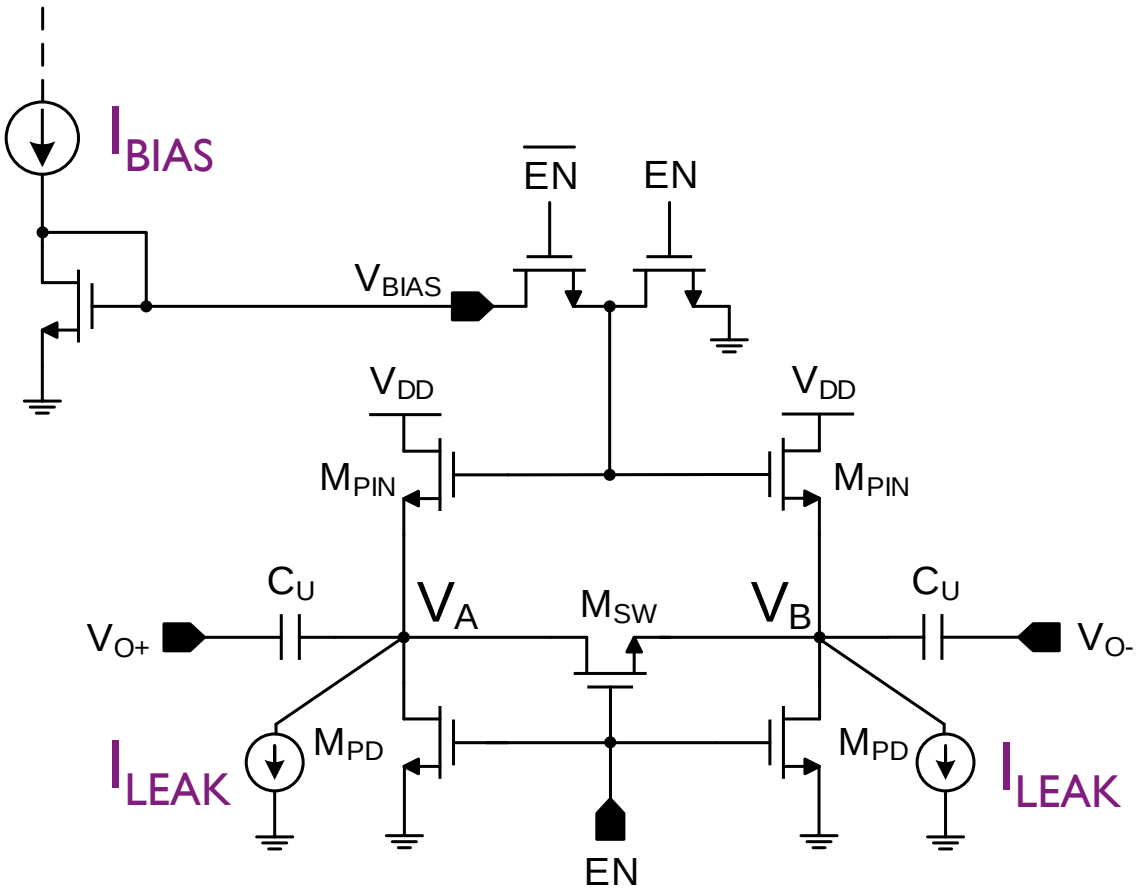
Layout-friendly final schematic

- V_{BIAS} provided to each M_{PIN} through independent paths



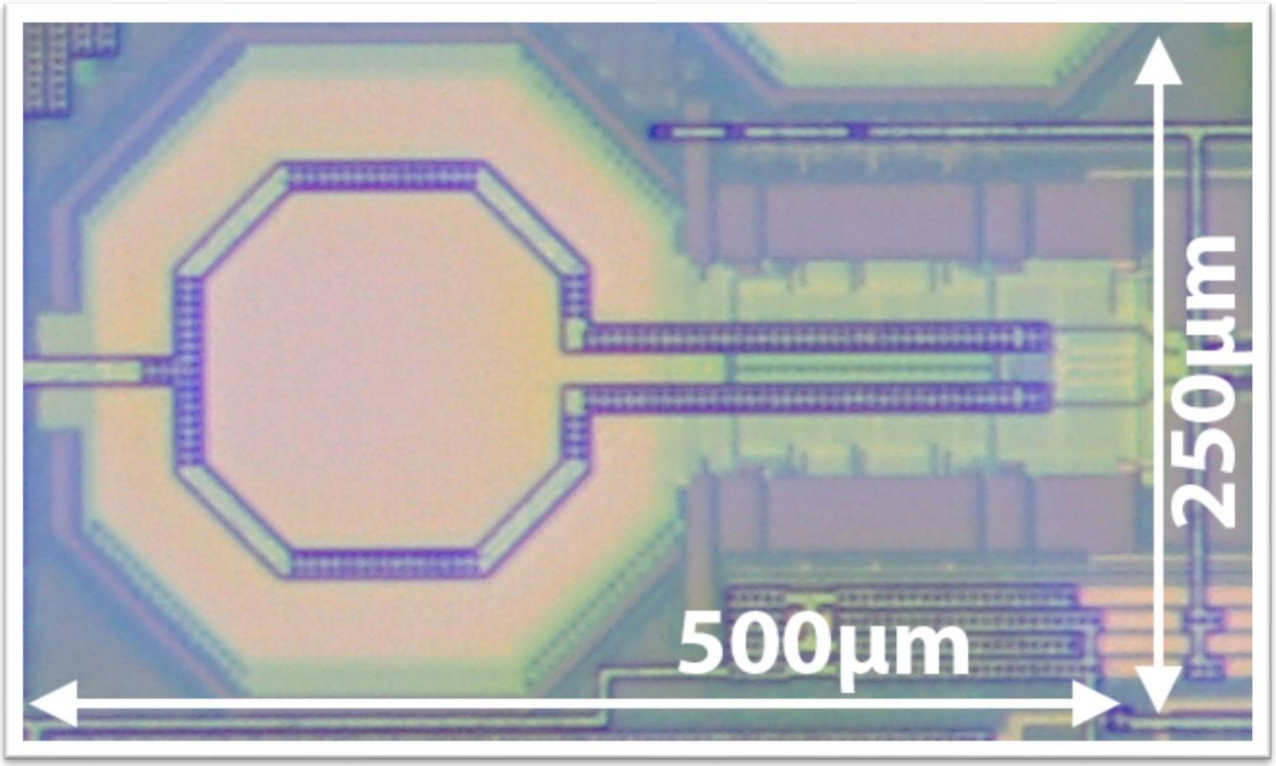
Layout floorplan

SIMPLE BIASING OPTION



$$I_{LEAK} < I_{BIAS} \rightarrow V_A, V_B > 0V$$

MEASURED RESULTS



SUMMARY OF PERFORMANCE

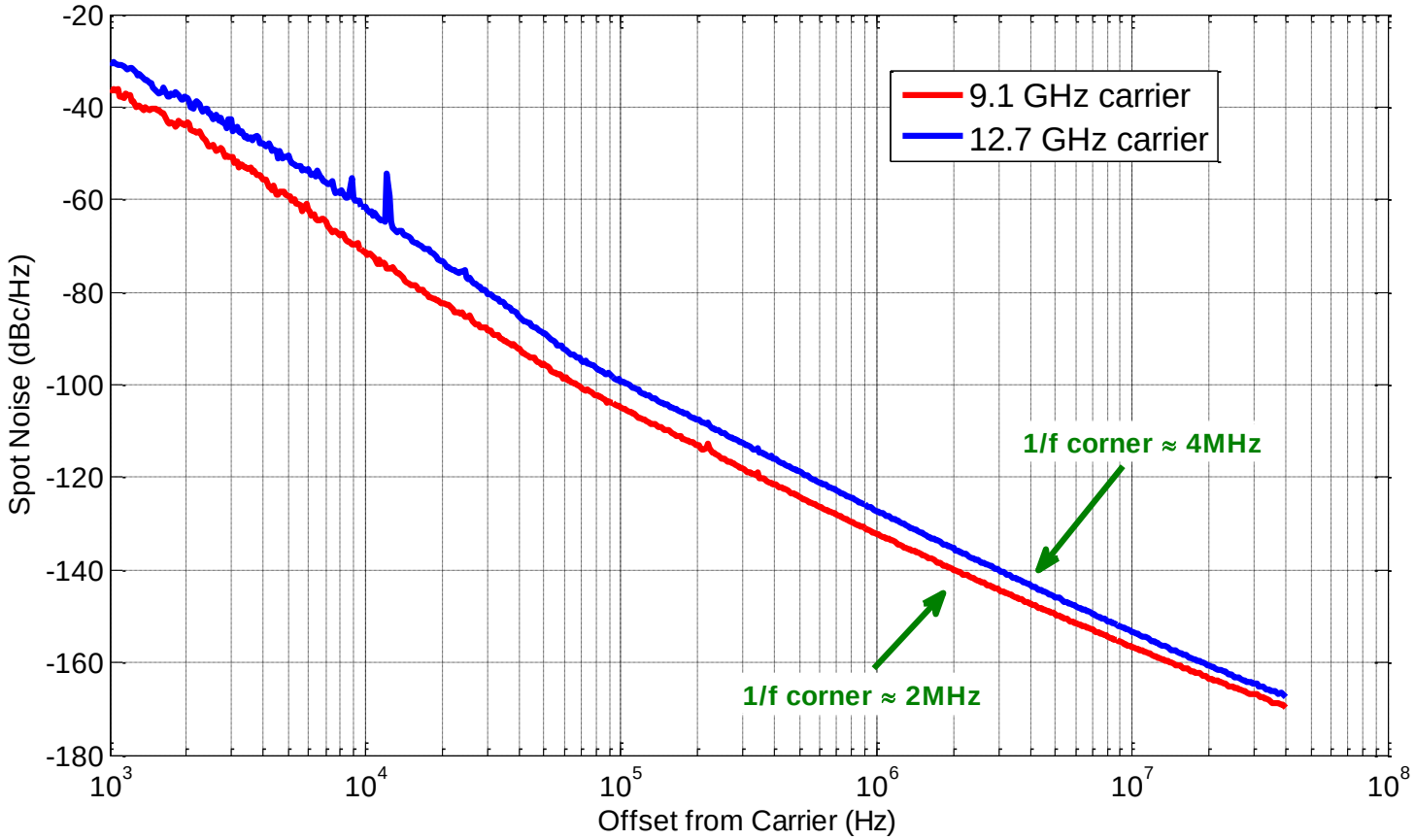
Technology	**28nm CMOS**	
Active Area	**0.125 mm^2 (500 µm x 250 µm)**	
Digital Supply (V_{DD})	**0.9 V**	
	Efficiency Configuration:	***Phase Noise Configuration:***
Analog Supply (V_{DDA})	**0.9 V**	**1.2 V**
Power (max/min)	**9.5 / 8.3 mW**	**20.8 / 18.4 mW**
Frequency Range	**9.1 – 12.7 GHz (32%)**	**9.0 – 12.4 GHz (32%)**
f_{min} PN @ 20MHz	**-163.2 dBc/Hz (w.r.t. 915MHz)**	**-165.2 dBc/Hz (w.r.t. 915MHz)**
f_{max} PN @ 20MHz	**-161.1 dBc/Hz (w.r.t. 915MHz)**	**-161.8 dBc/Hz (w.r.t. 915MHz)**
FoM (max/min)	**187.0 / 184.4 dBc/Hz**	**185.4 / 182.8 dBc/Hz**

COMPARISON WITH SOTA

	Area (mm^2)	Frequency (GHz)	PN @ 20MHz from 915MHz (dBc/Hz)	P_{DC} (mW)	FoM (dBc/Hz)
Fanori, ISSCC 2012	0.39 (55nm)	6.7-9.2 (32%)	-169	27	188/189
Liscidini, ISSCC 2012	0.49 (55nm)	6.5-9.0 (33%)	-168	36	185
Visweswaran, ISSCC 2012	0.19 (65nm)	7.3-8.0 (10%)	-170	25.8	190
Dal, JSSC 2010	0.06 (65nm)	13-15 (15%)	-162	8.4	185
This work	0.13 (28nm)	9.1 – 12.7 (32%)	-163	9.5	187

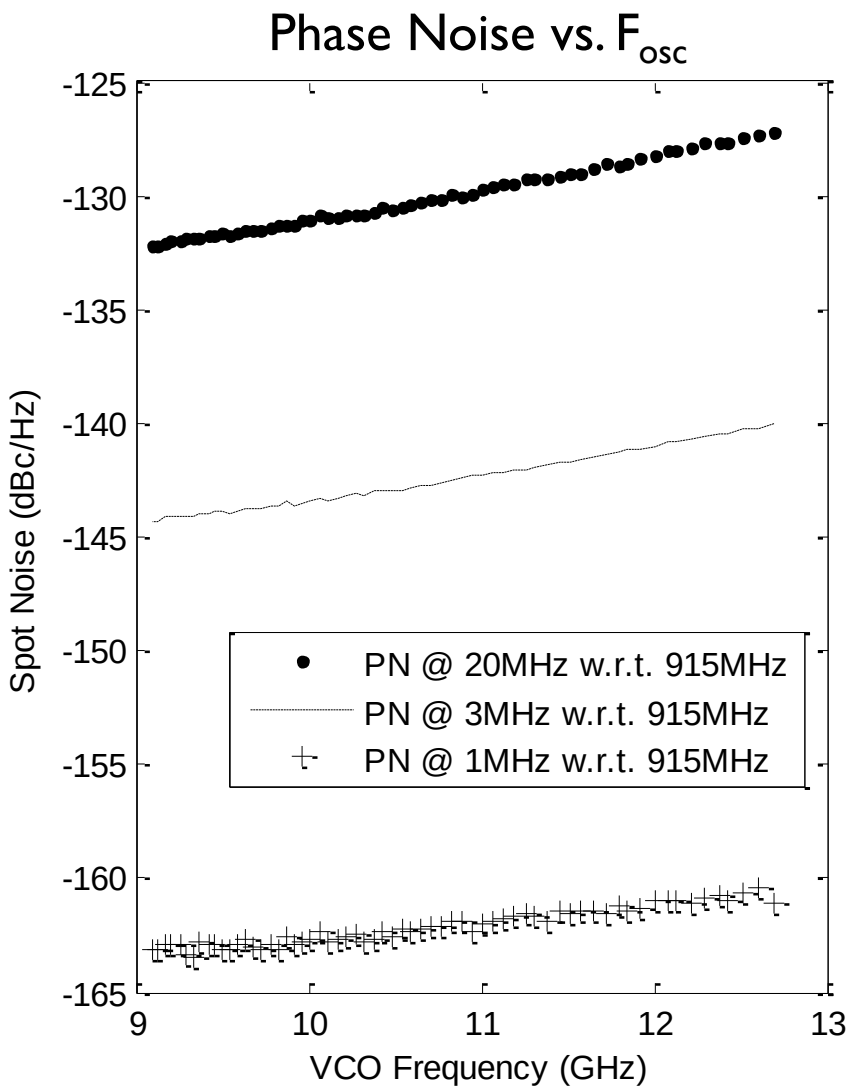
State of the art cellular TX VCOs with f_{max} > 6GHz

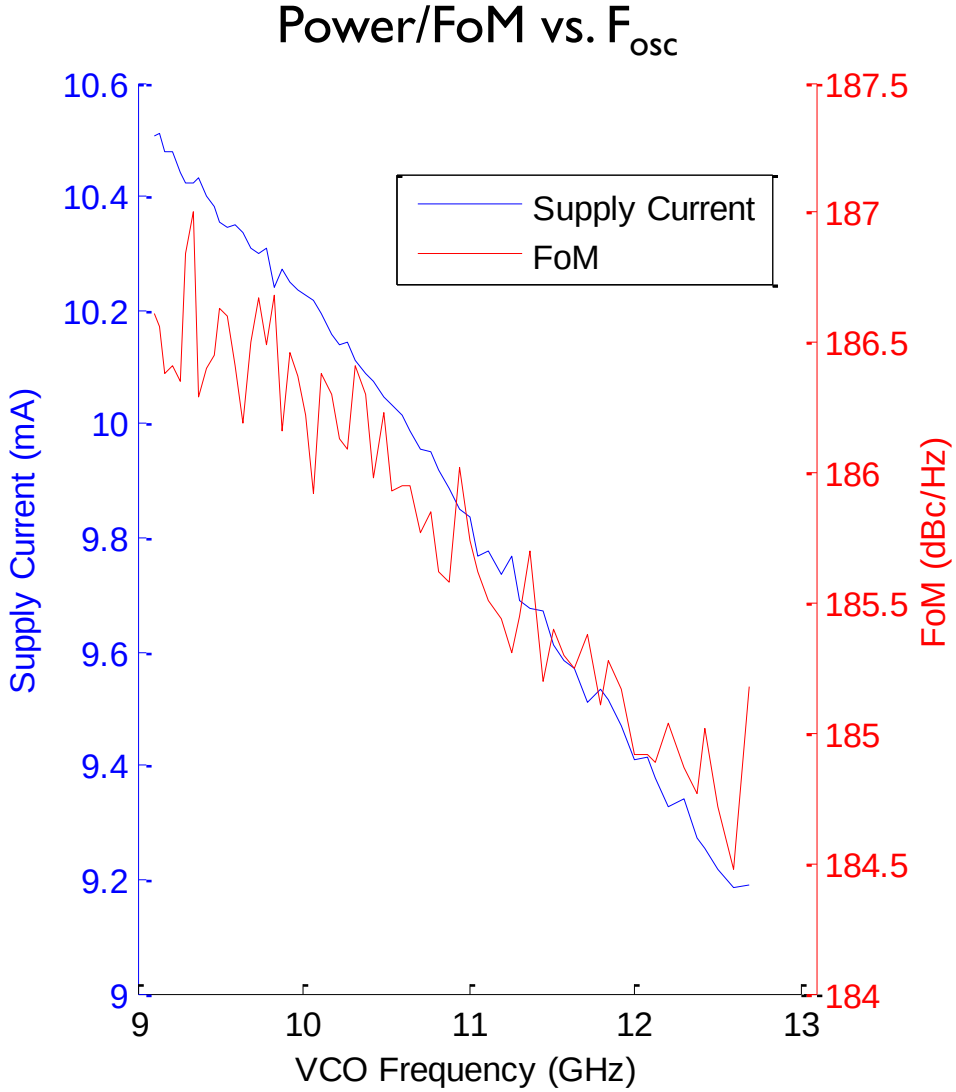
PHASE NOISE



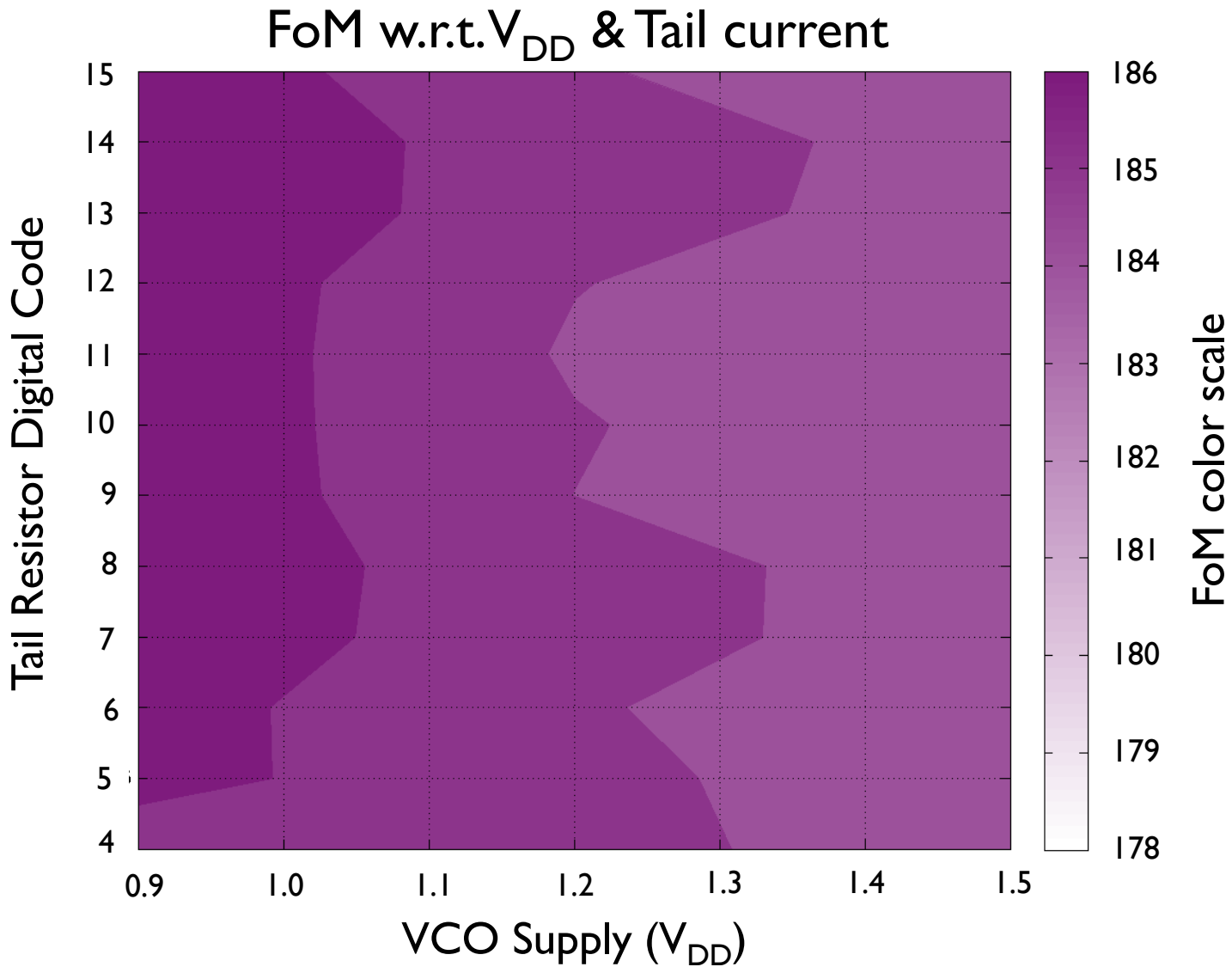
- +1.5dB @ 20MHz offset vs. simulation
  - Due to high1/f corner (700kHz in sim)
  - Large variance in 1/f noise not included in model

OPERATION ACROSS FREQUENCY

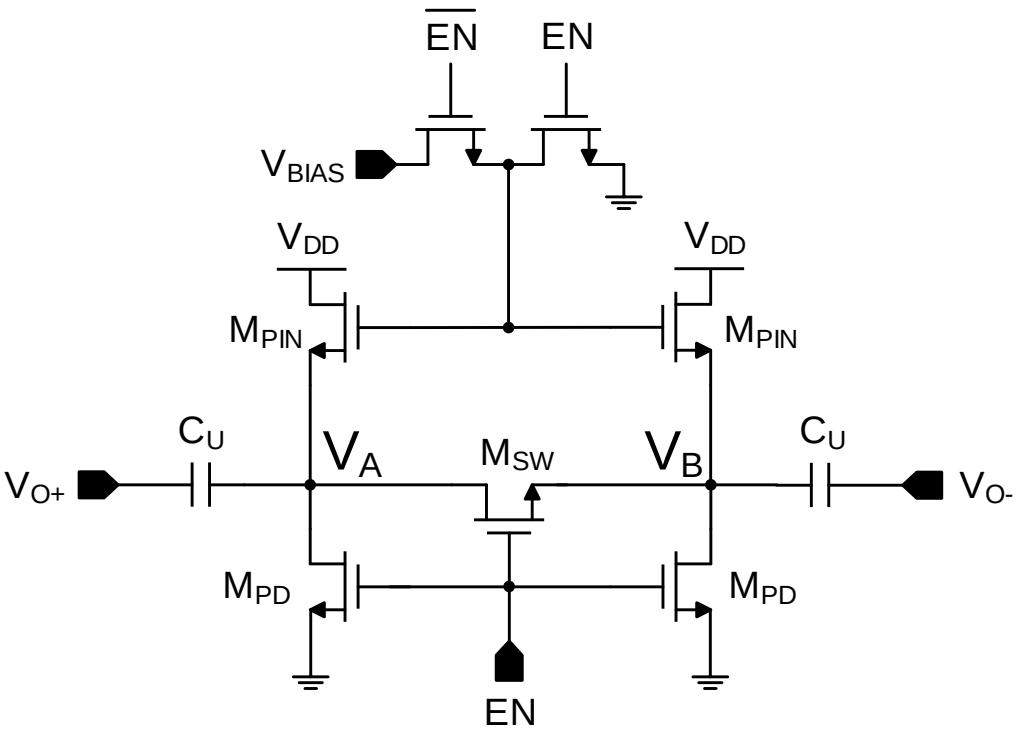




POWER EFFICIENCY



CONCLUSION

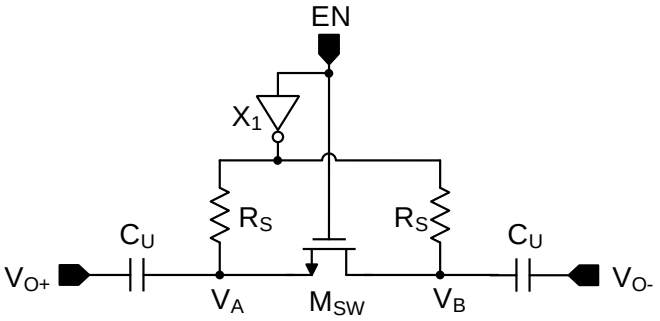


- Minimal voltage stress and diode leakage
- Optimal off-state Q
- Compact NMOS-only layout

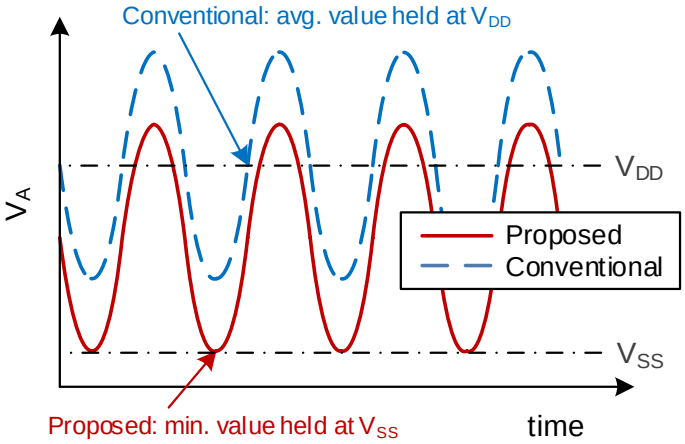
THANK YOU FOR YOUR ATTENTION

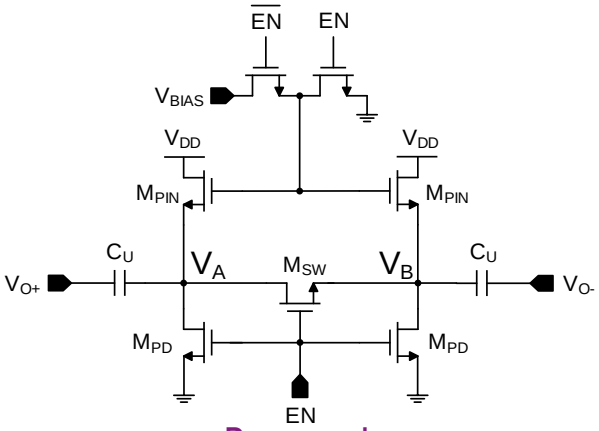
ADDITIONAL MATERIAL

“PINNING” CAPACITOR CELL

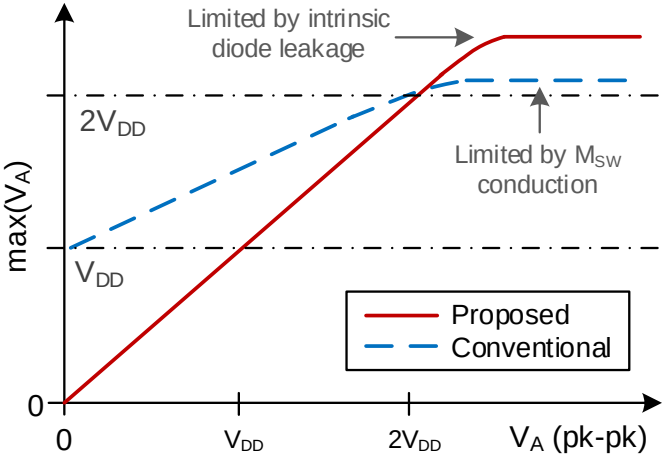


Conventional

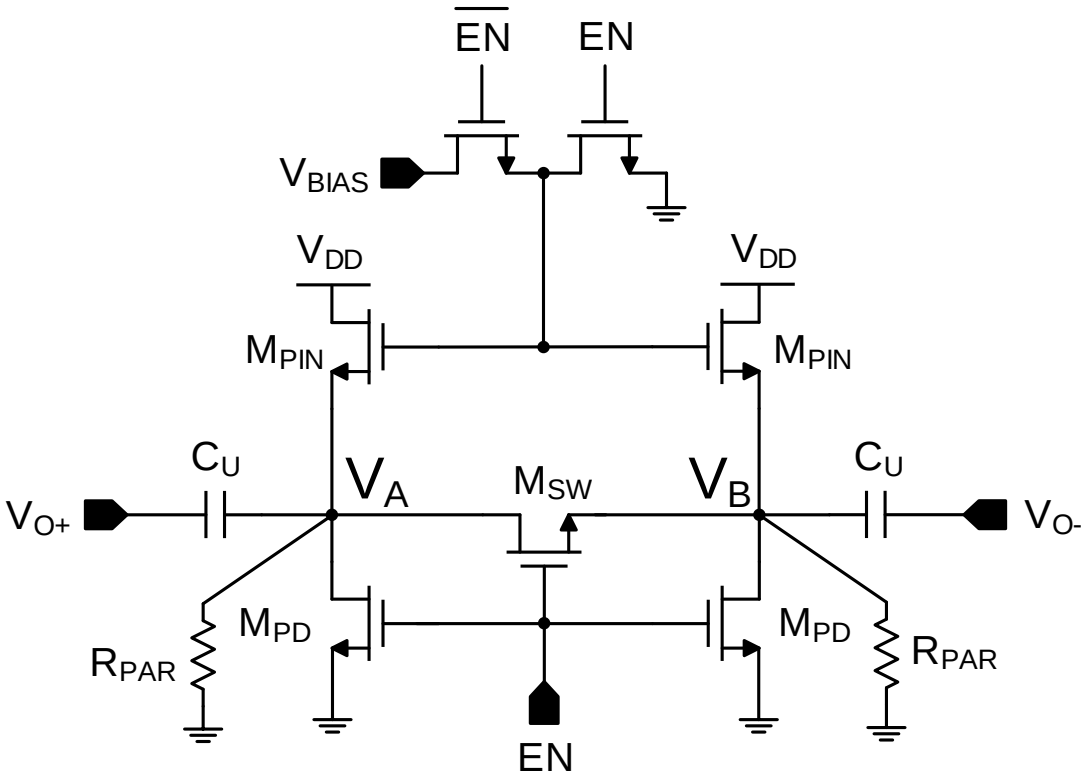




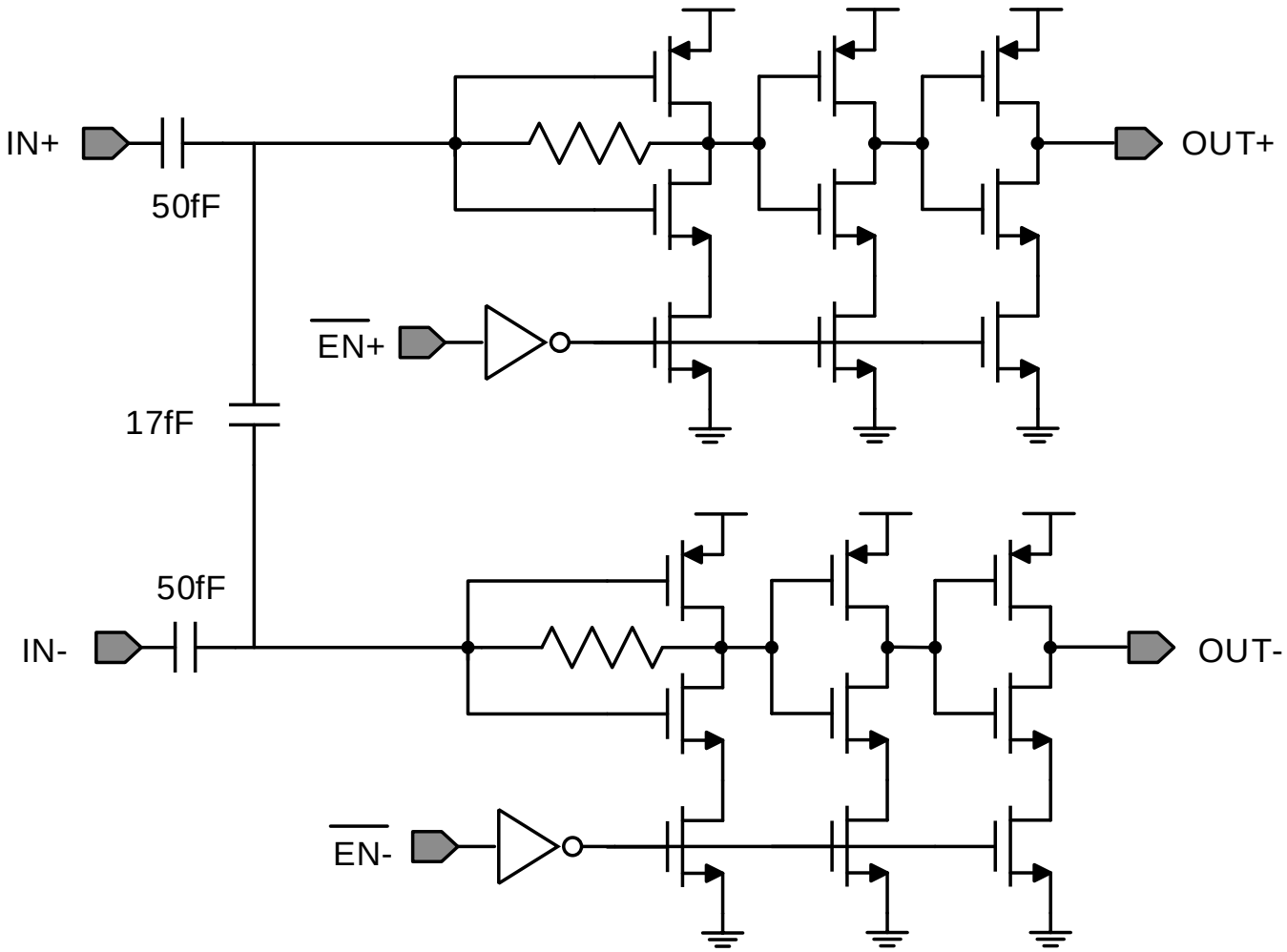
Proposed



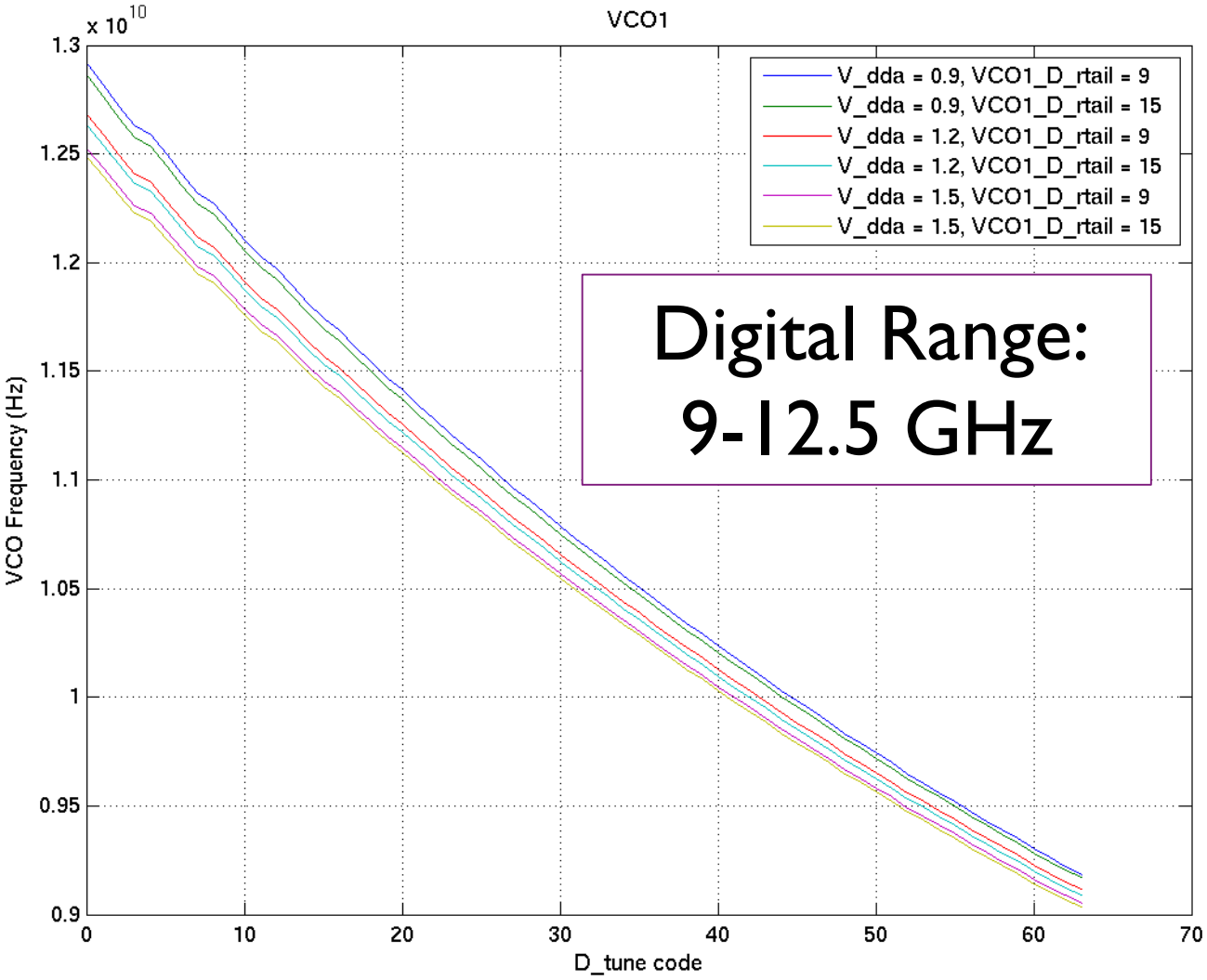
INTENTIONAL LEAKAGE PATH



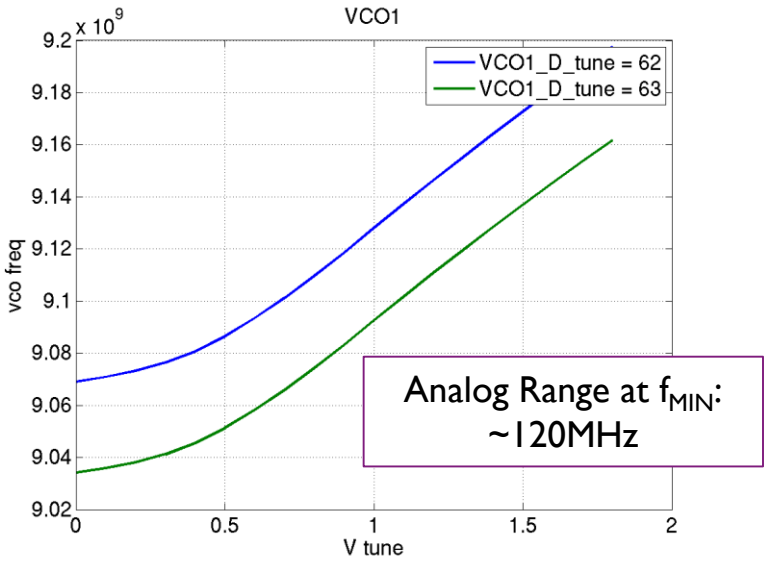
OUTPUT BUFFER

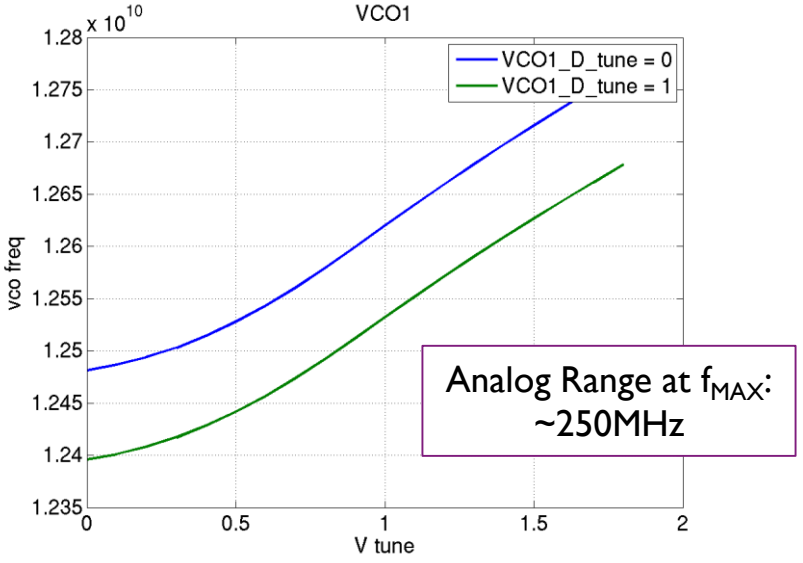


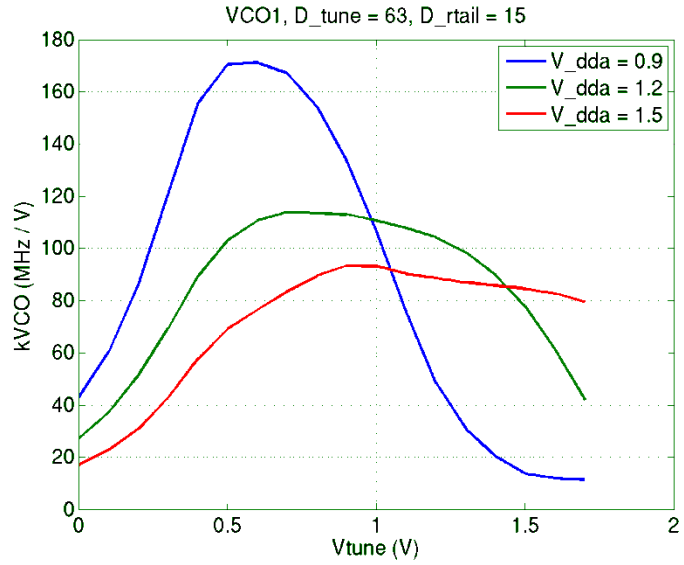
DIGITAL FREQUENCY TUNING

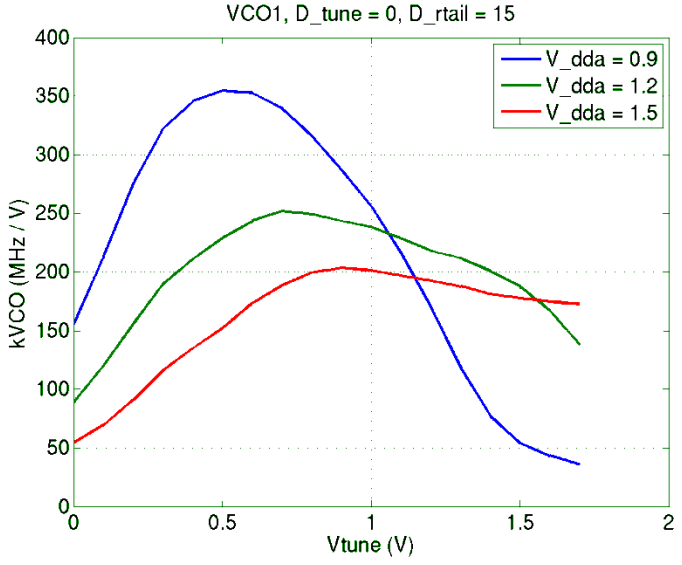


ANALOG FREQUENCY TUNING

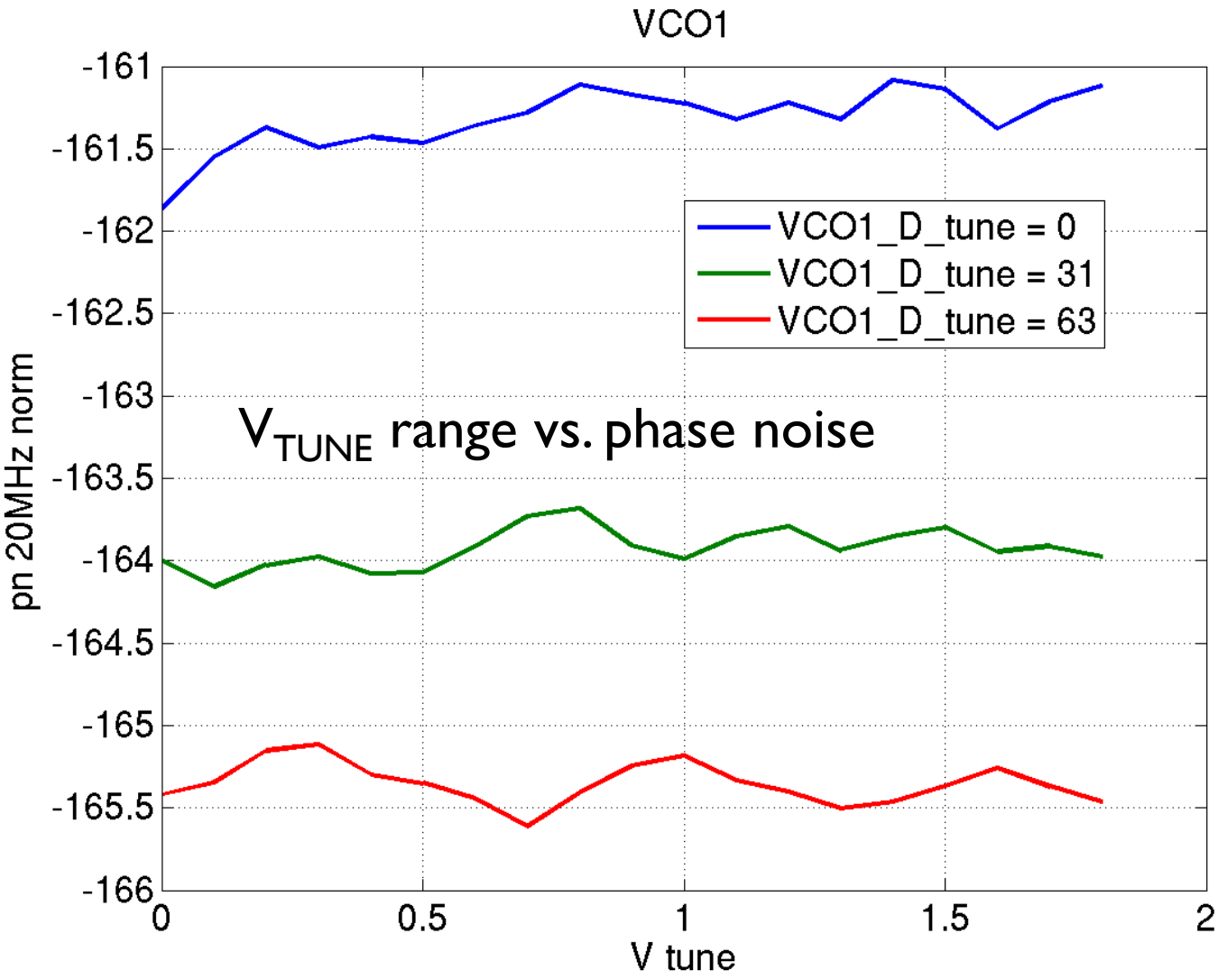




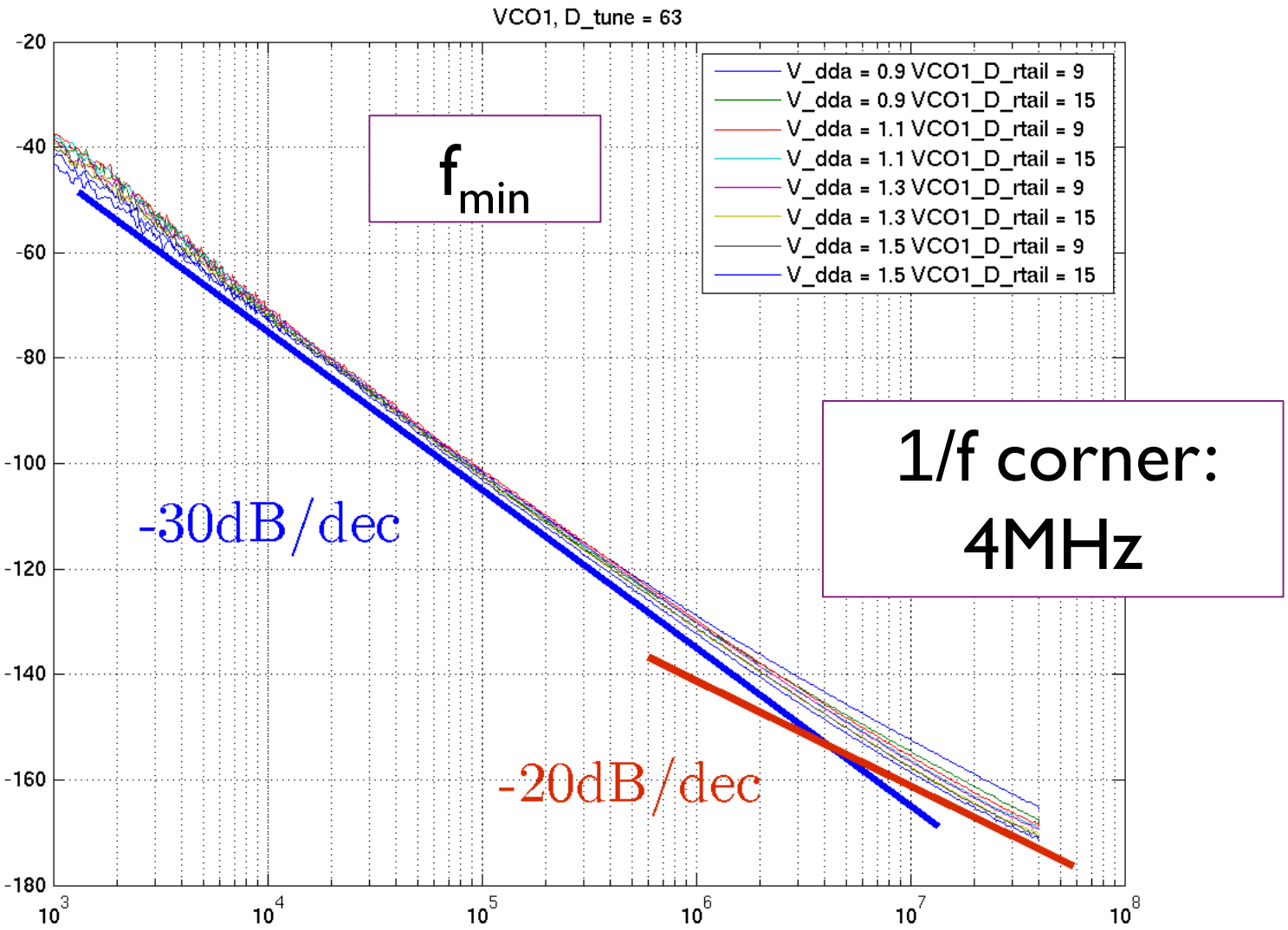




ANALOG FREQUENCY TUNING

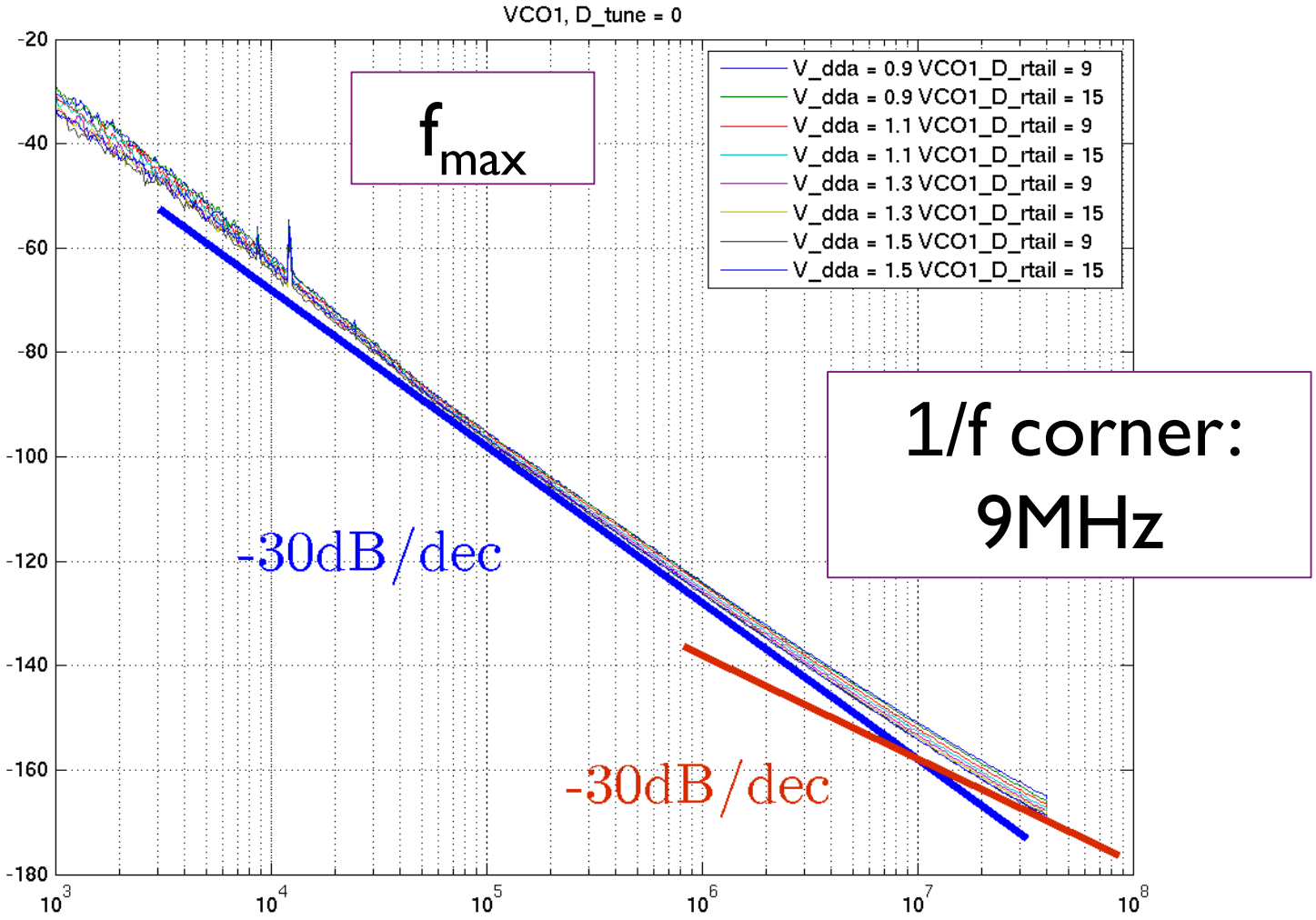


PHASE NOISE



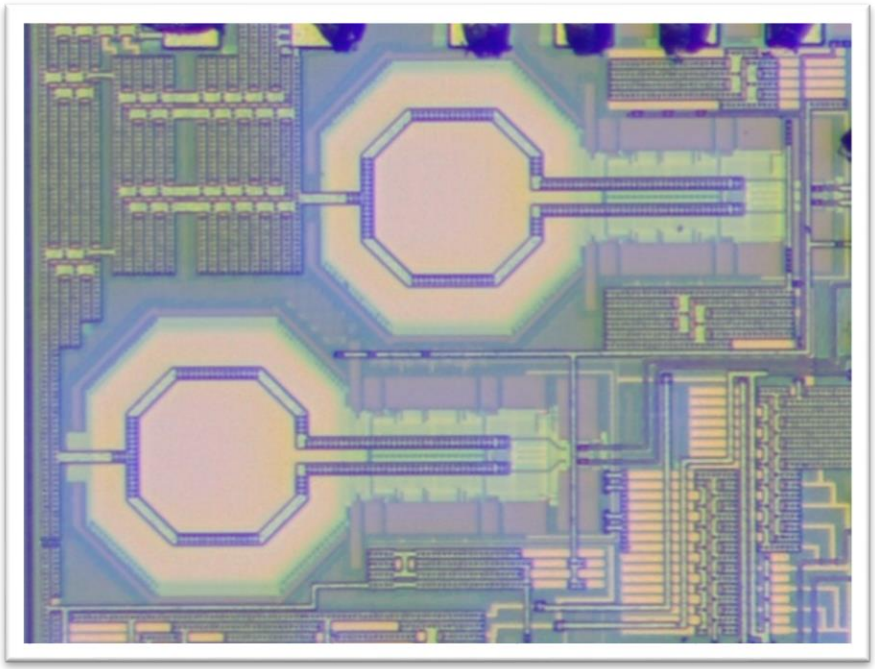
1/f corner:
4MHz

PHASE NOISE



1/f corner:
9MHz

DIODE LEAKAGE COMPARISON



- 2 flavors compared
  - Ultra-low V_T
  - Low V_T

REVERSE-BIAS LEAKAGE TEST