A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

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GIGA-SAMPLE ADCS

MOTIVATION

- High performance giga-sample ADCs
  - >9 ENOB, >70 dB SFDR, >2GS/s
  - E.g. direct-RF sampling

- Architectures use residue-amplification
  - Minimizes # of interleaved channels
  - High bandwidth amplifiers severely limit power efficiency
  - Design freedom reduced as a consequence

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- Next generation amplification solutions are needed

IN THIS TALK

PREVIEW

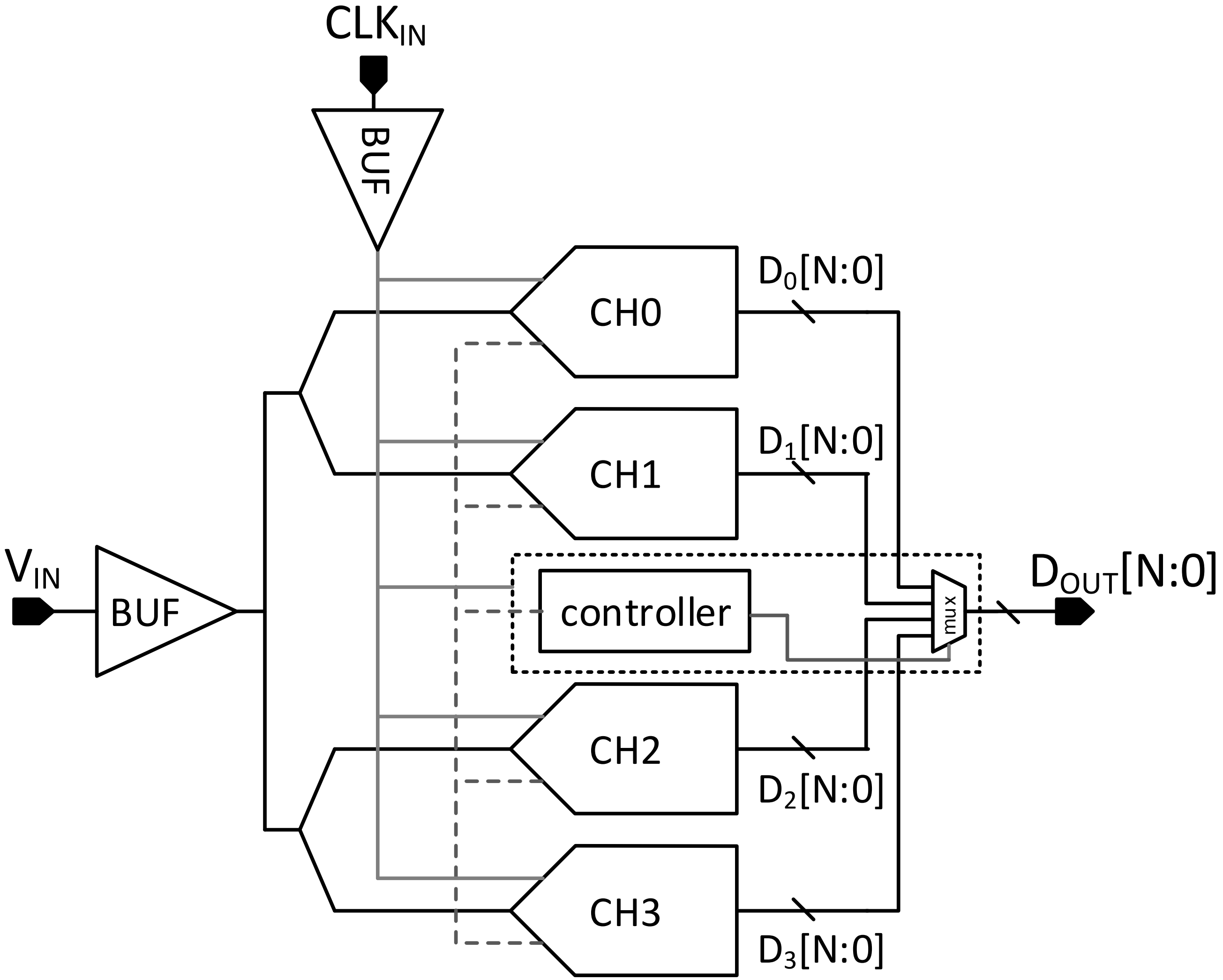
- A 3.2GS/s direct-RF sampling ADC in 16nm
  - Uses 36 ring amplifiers
  - Advances SoTA by an order of magnitude

- Technique for background measurement of Signal-to-Distortion ratio
  - Applicable to any switched capacitor feedback circuit
  - Used here to tune biasing of ringamps w.r.t. PVT

TOP LEVEL

SYSTEM OVERVIEW

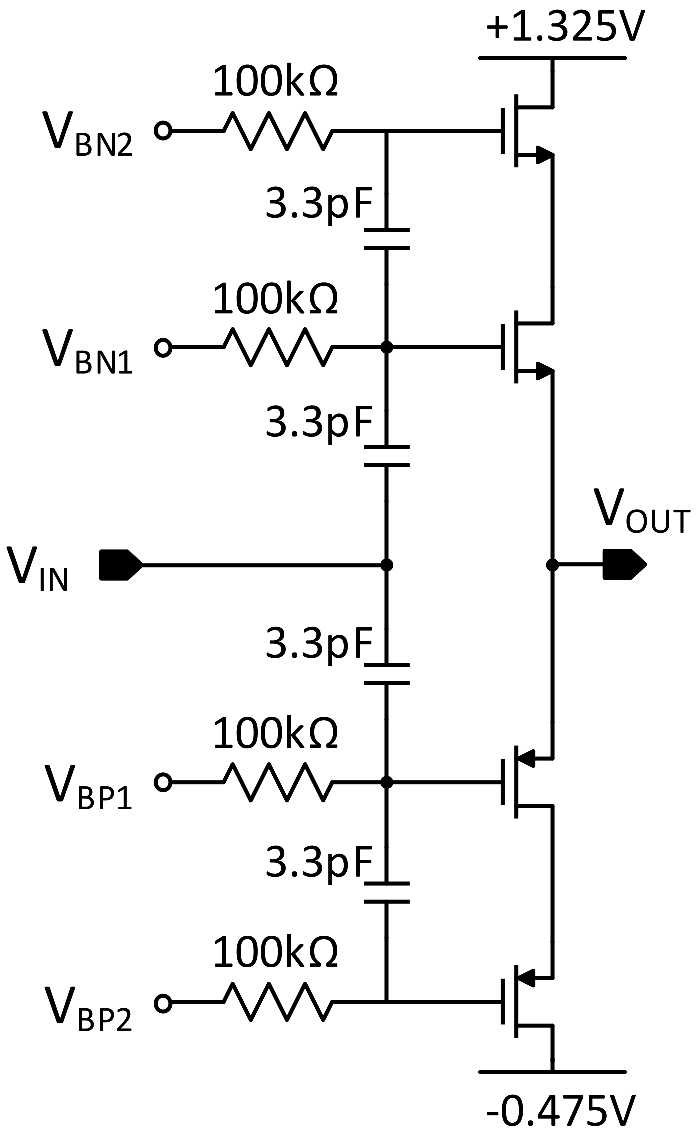
- 3.2GS/s
    - 4 channels @ 800 MS/s



INPUT BUFFER

SYSTEM OVERVIEW

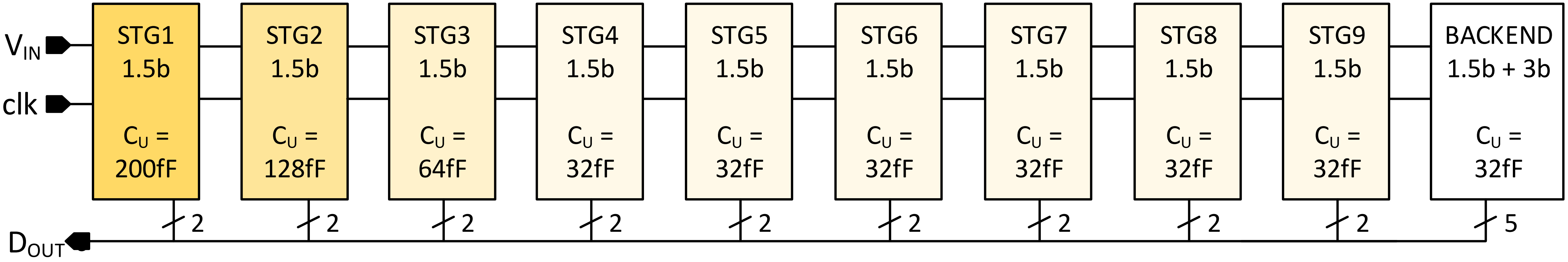
- Pseudo-differential class-AB push-pull source follower
- AC-coupled input
- 1.8V supply centered around V_{CM}



3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

CHANNEL

SYSTEM OVERVIEW



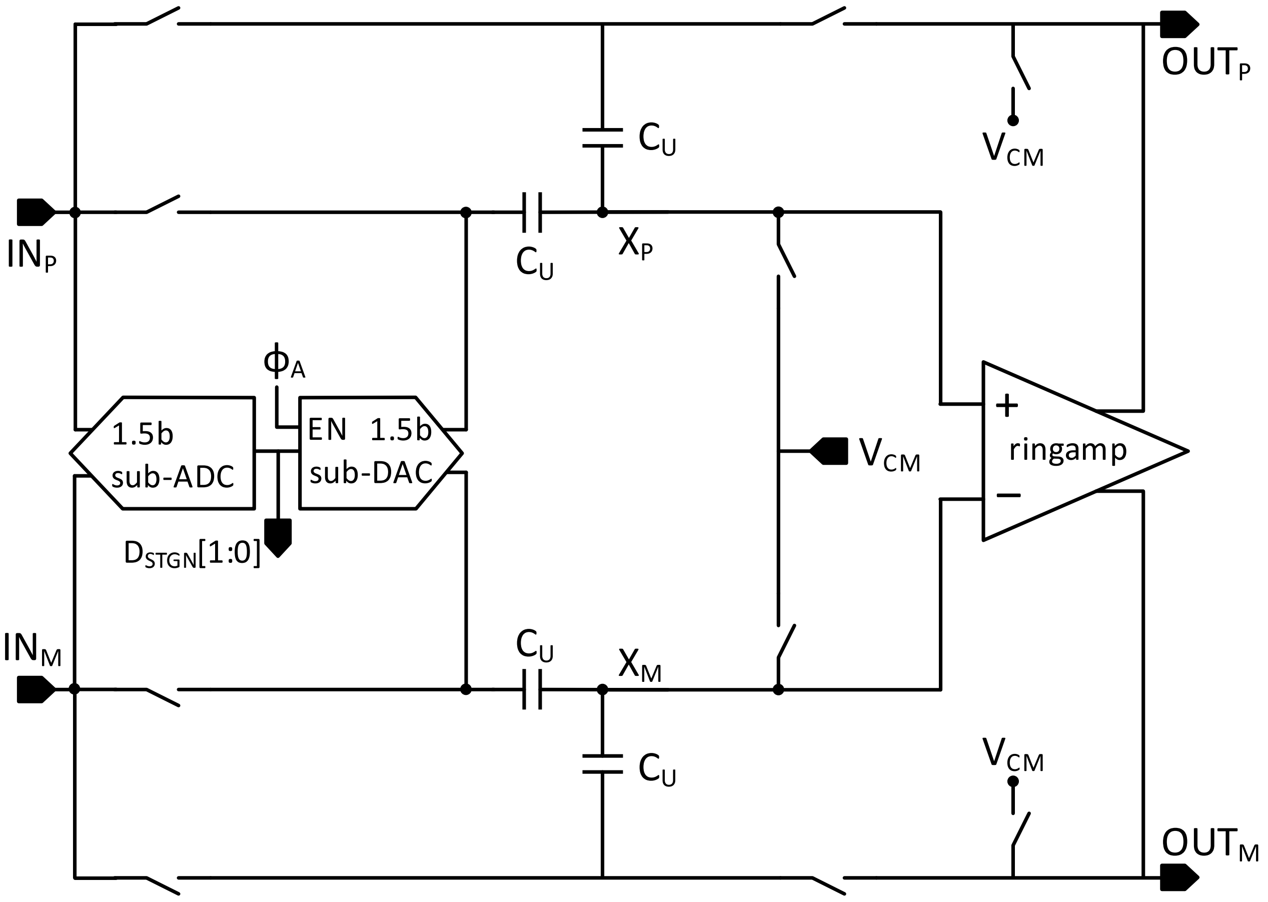
- 9 x 1.5b/stage
- 1.5b + 3b backend flash stage

STAGE 1

SYSTEM OVERVIEW

- Conventionally, there are 2 sampling networks
  - MDAC
  - sub-ADC

Conventional MDAC + sub-ADC



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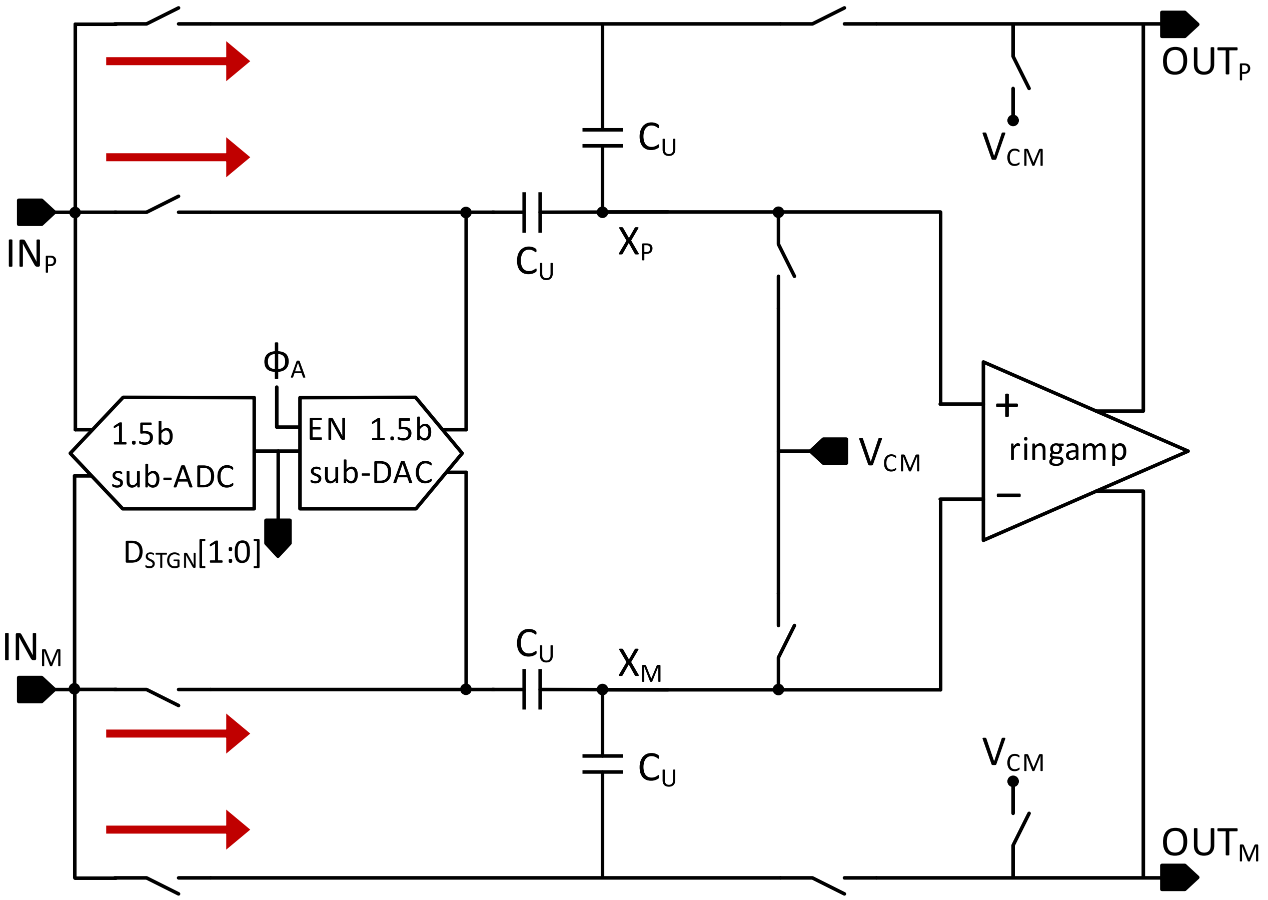

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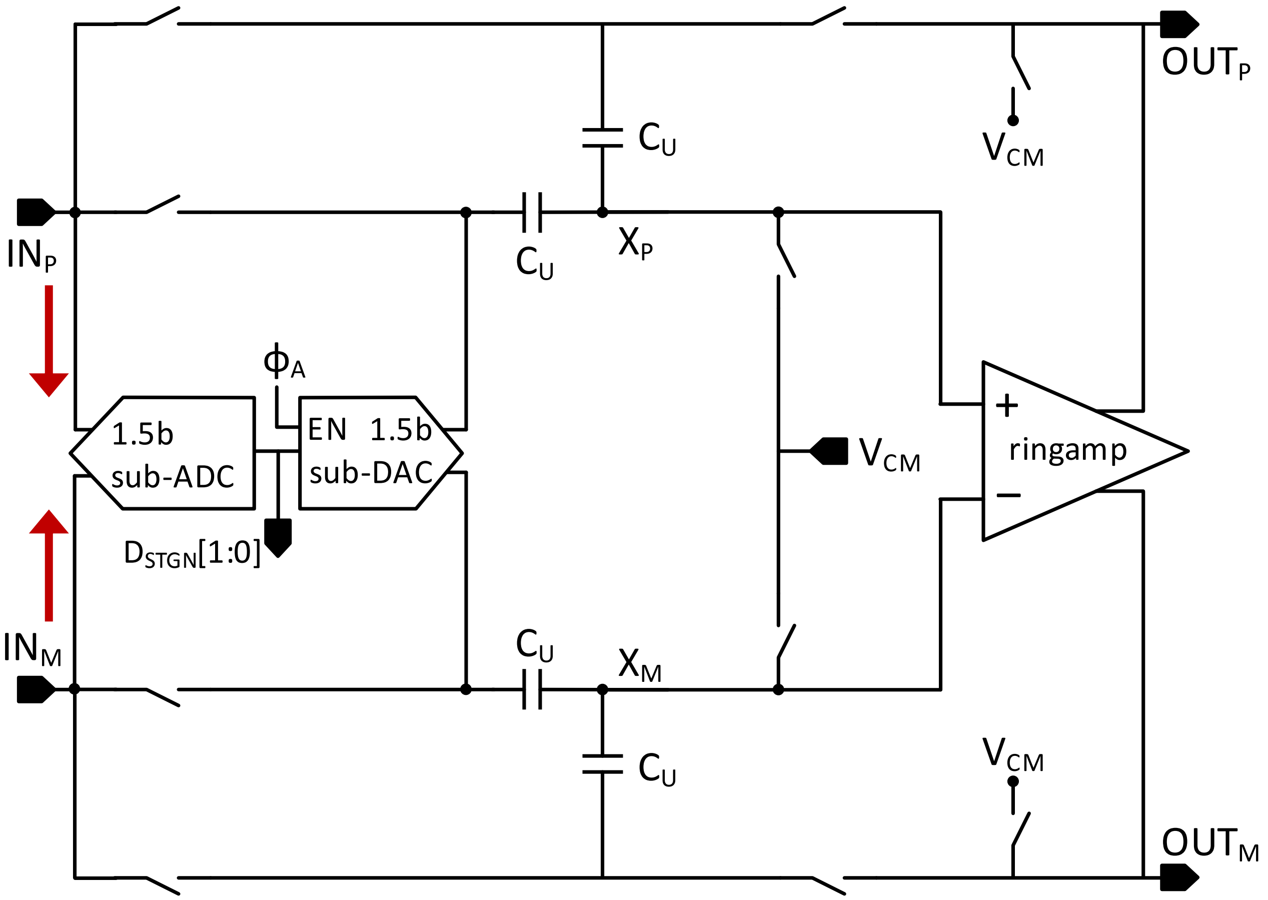
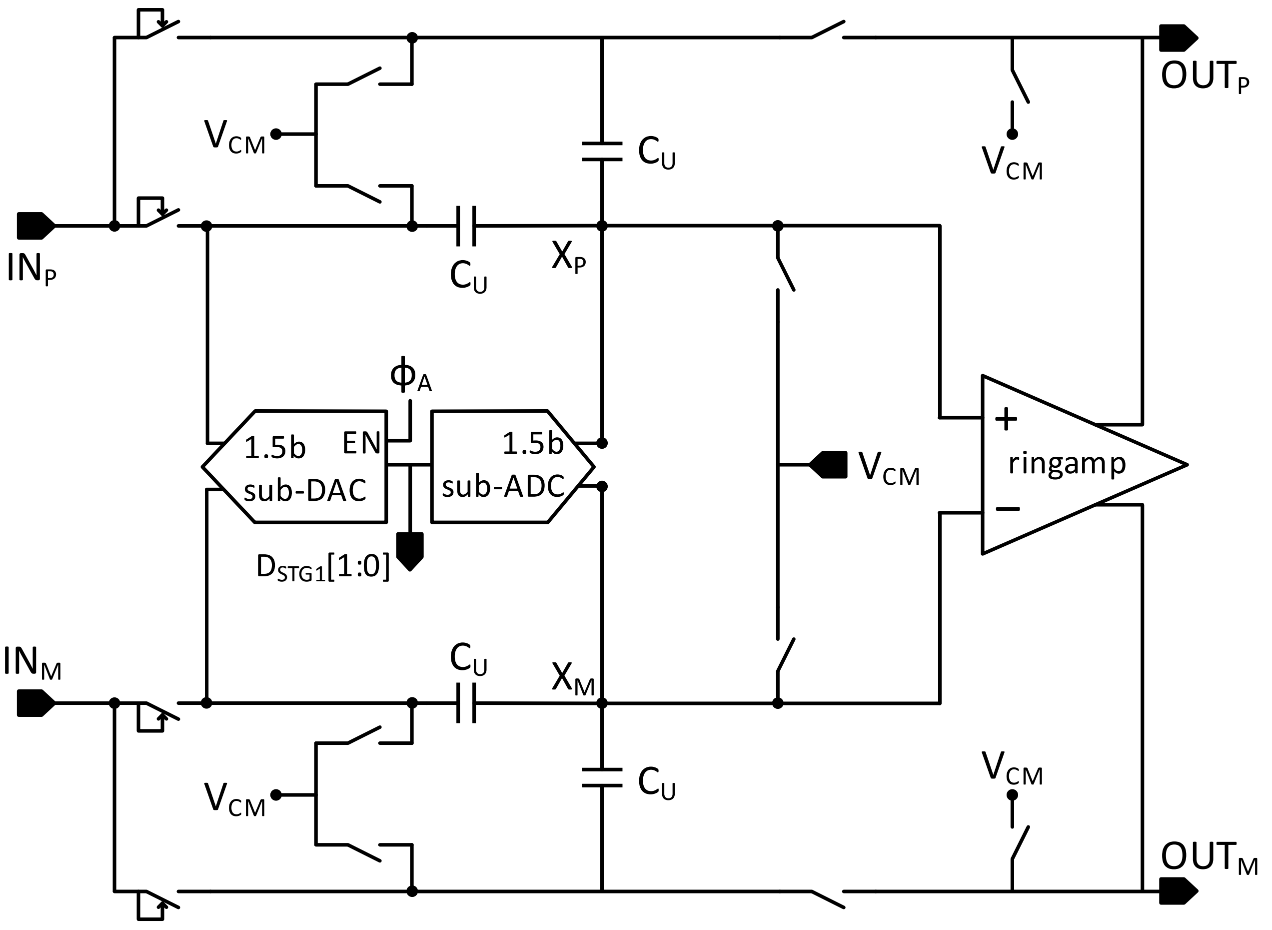


STAGE 1

SYSTEM OVERVIEW

- Conventionally, there are 2 sampling networks
  - MDAC
  - sub-ADC
- HERE: Single sampling path

Stage 1 MDAC with Passive-Hold



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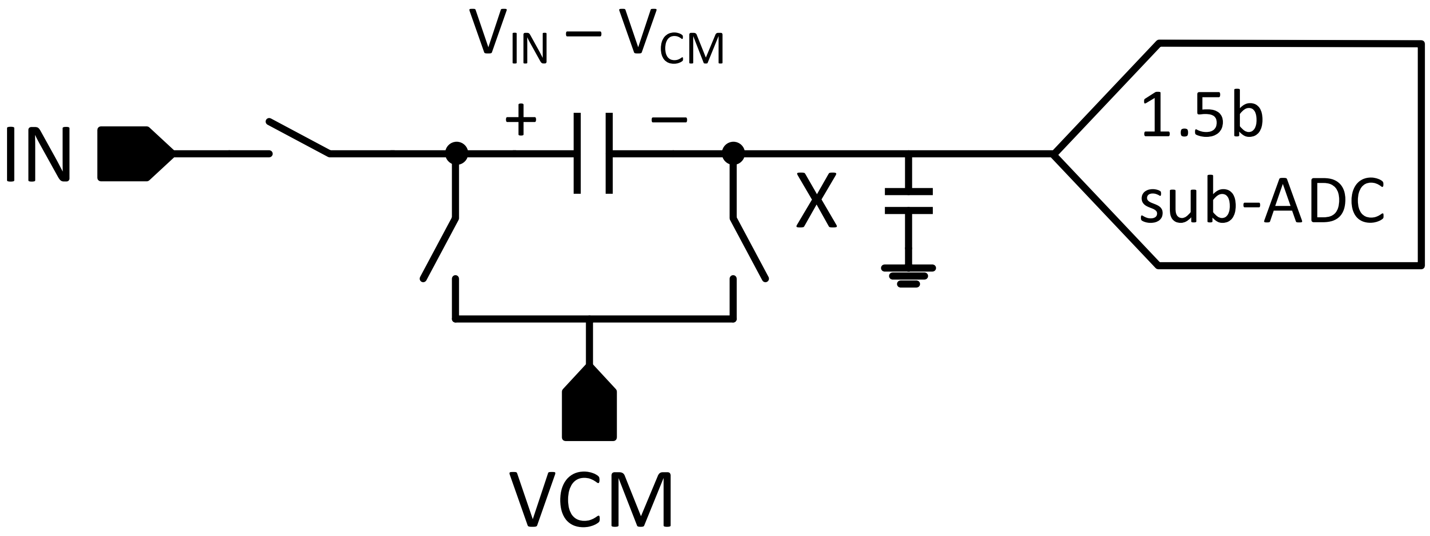
FRONTEND QUANTIZATION SCHEME

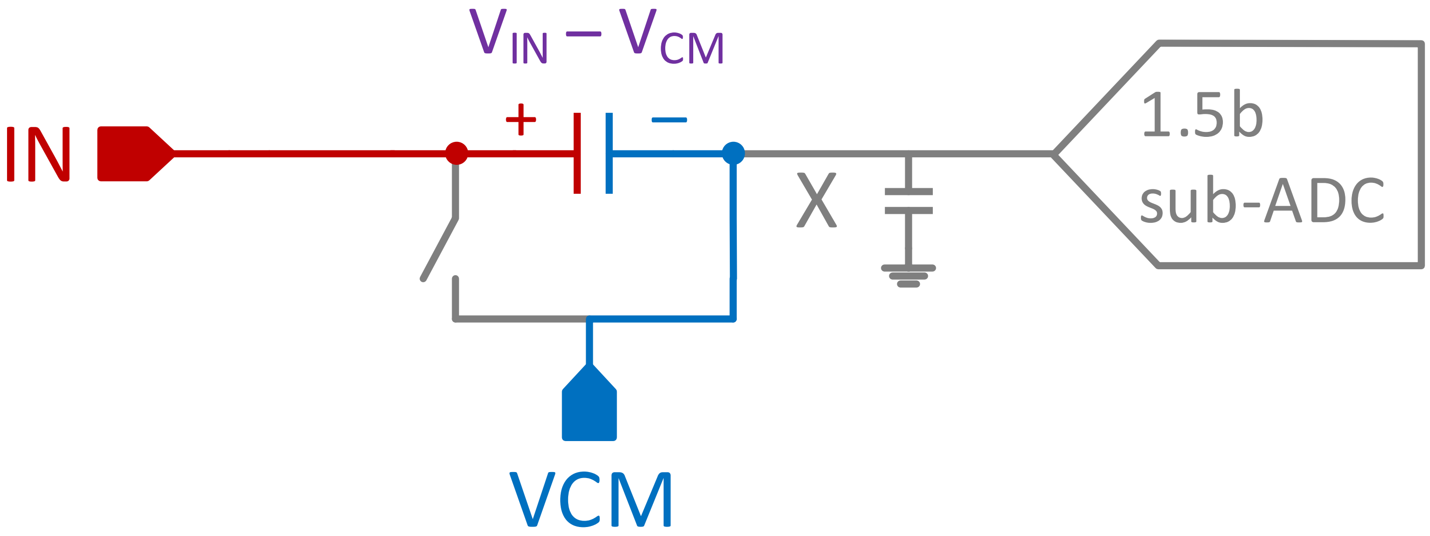
SYSTEM OVERVIEW



FRONTEND QUANTIZATION SCHEME

SYSTEM OVERVIEW

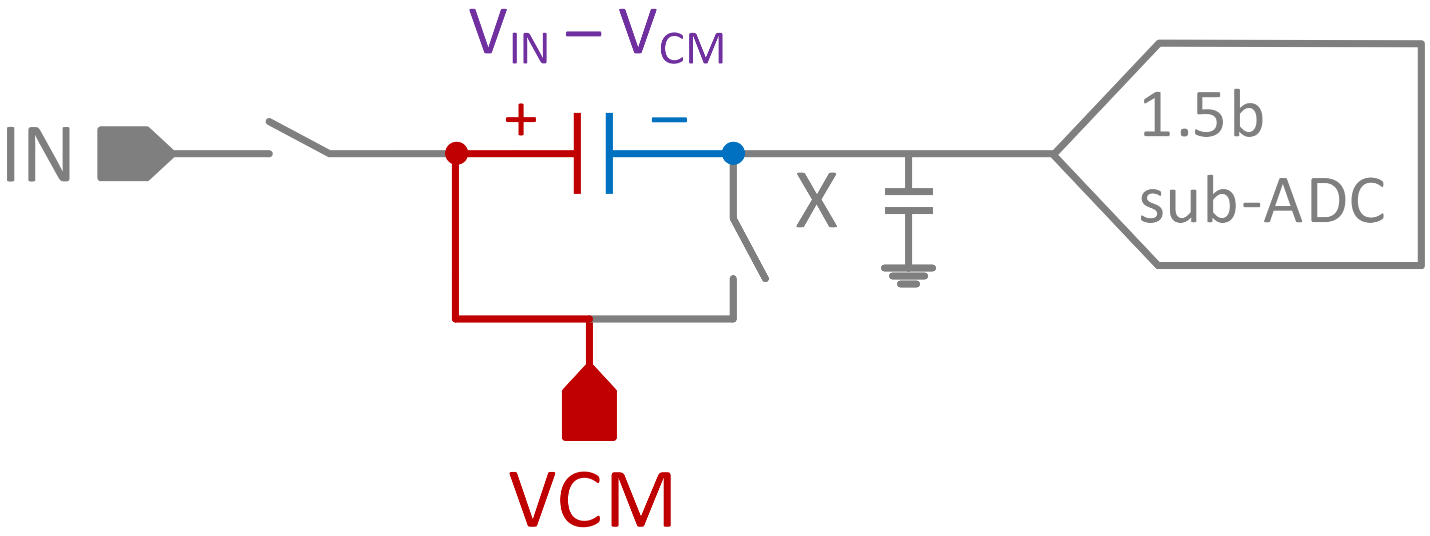
- Track



FRONTEND QUANTIZATION SCHEME

SYSTEM OVERVIEW

- Track
- Passive hold



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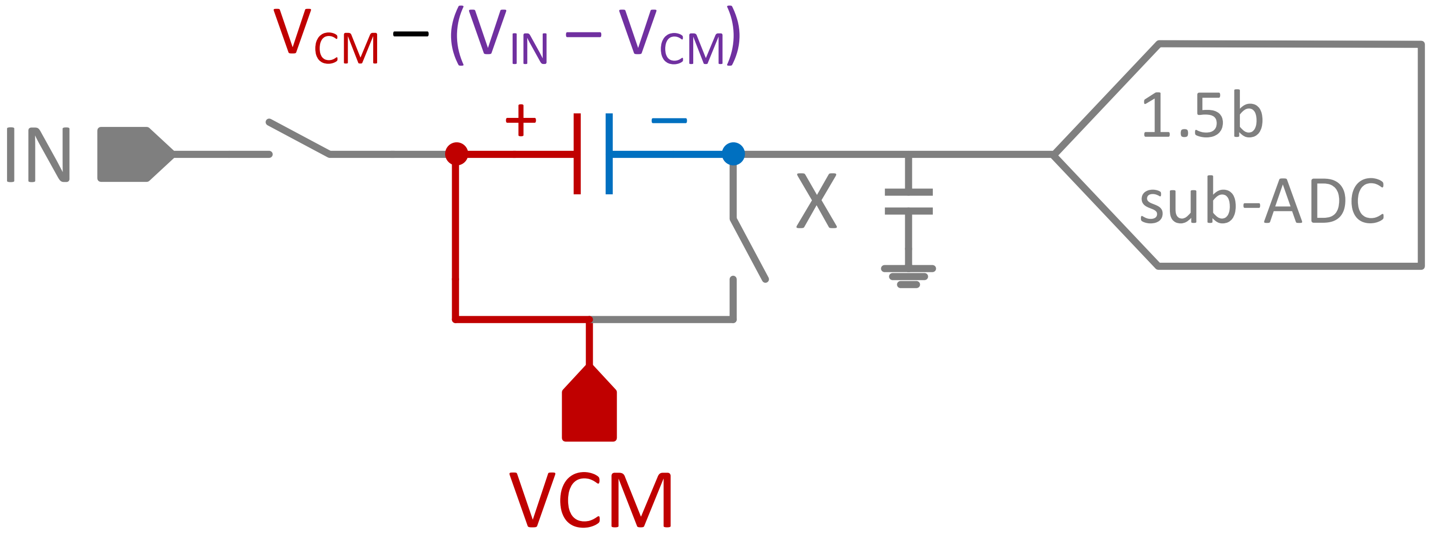

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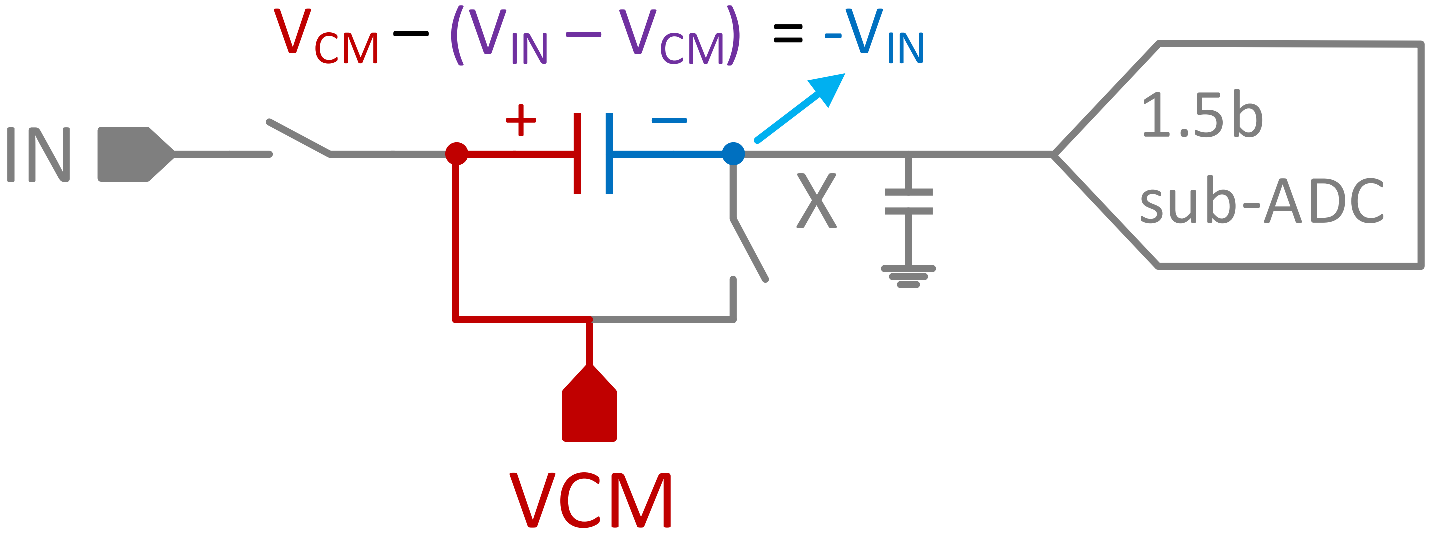

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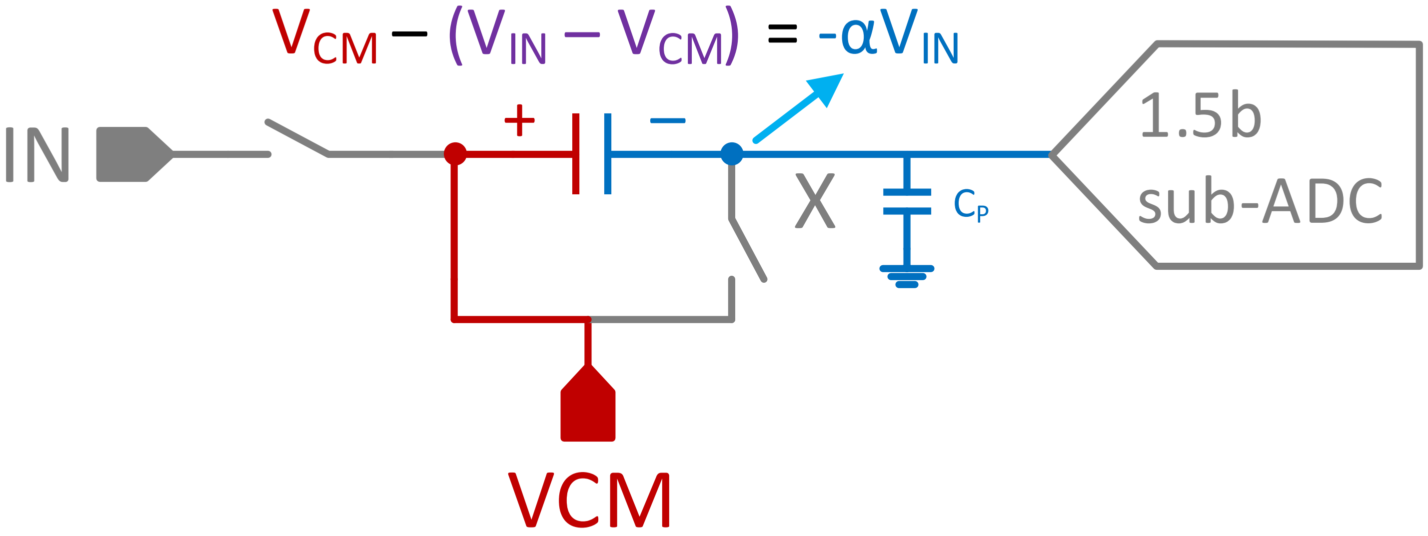


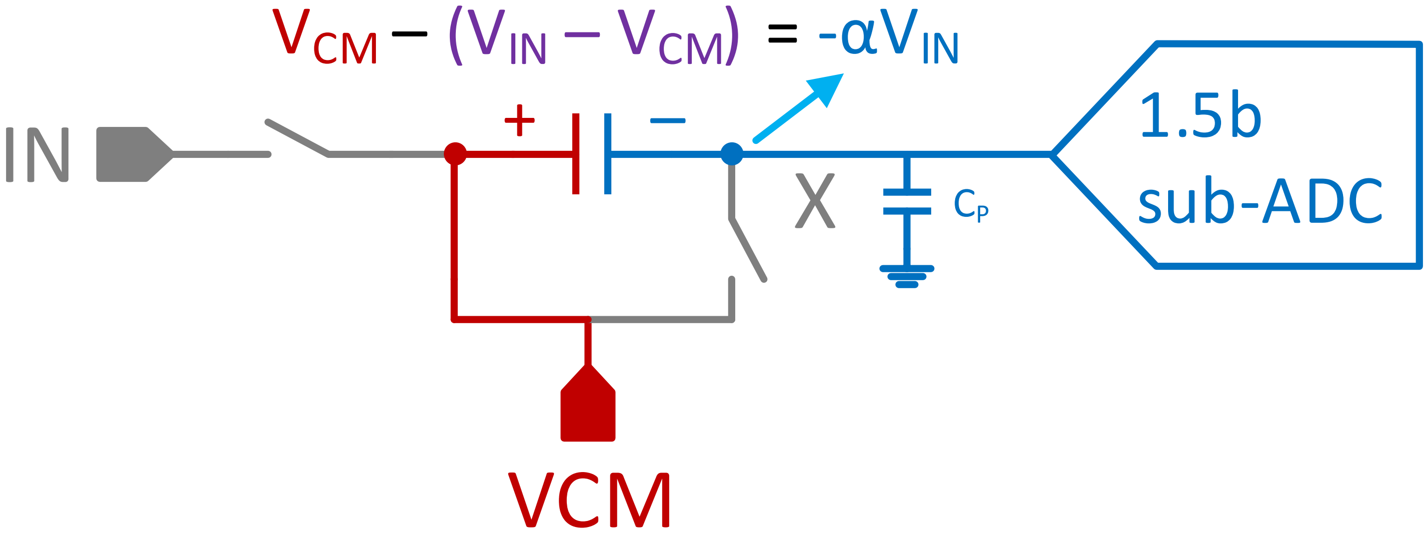
3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

FRONTEND QUANTIZATION SCHEME

SYSTEM OVERVIEW

- Track

- Passive hold
  - Quantize



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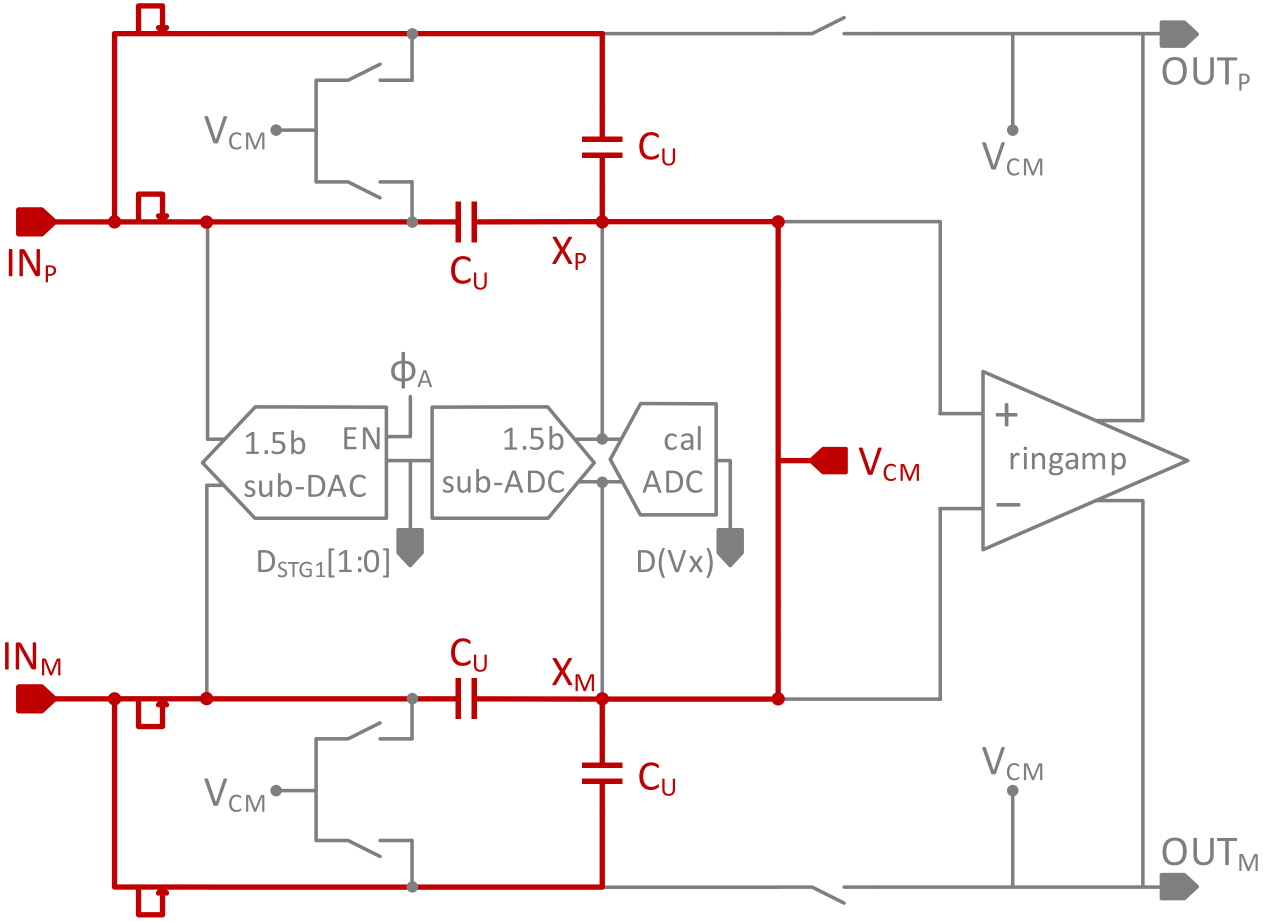
STAGE 1

SYSTEM OVERVIEW

- Track

Phase 1: Track

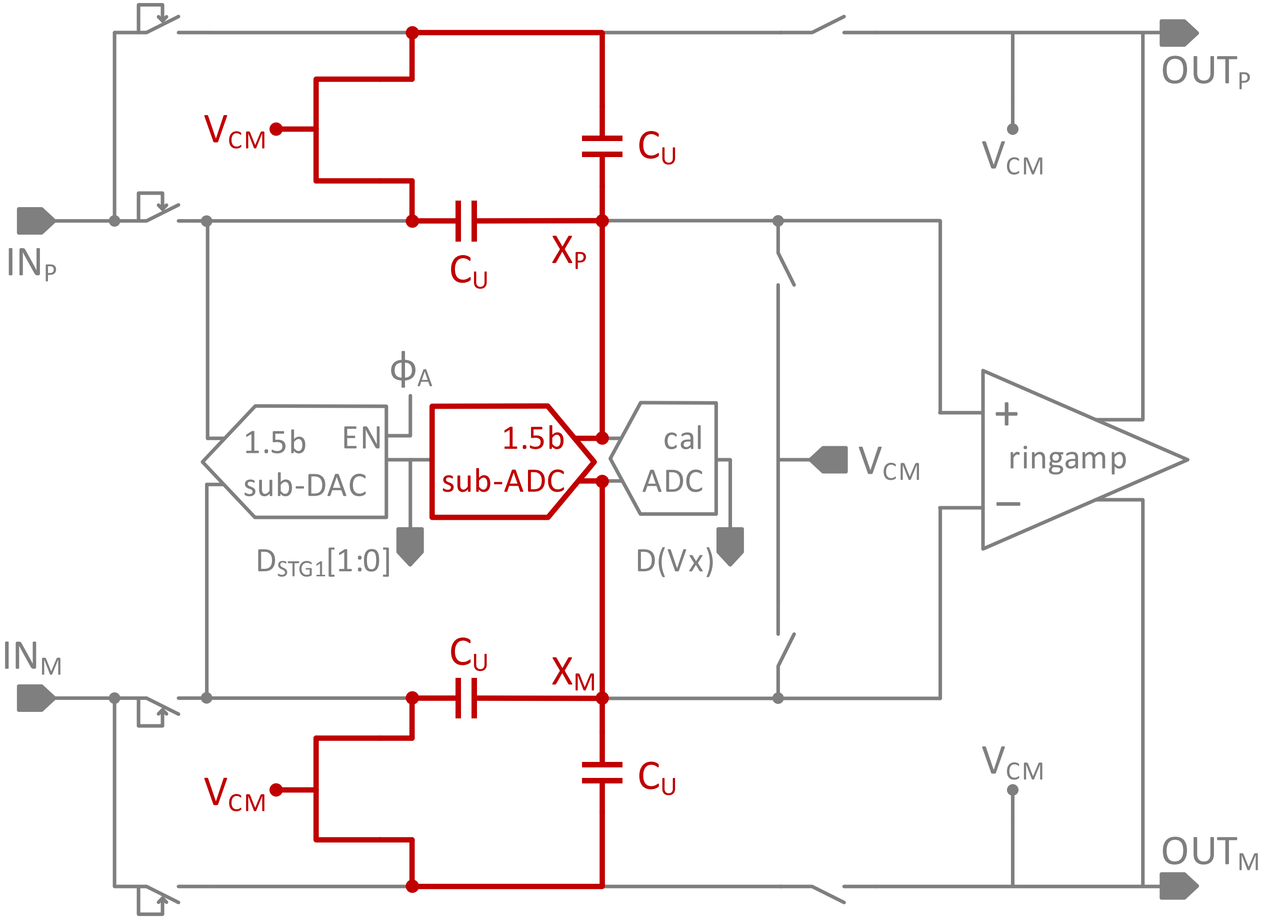


STAGE 1

SYSTEM OVERVIEW

- Track
- Quantize (Passive hold)

Phase 2: Quantize (Passive Hold)

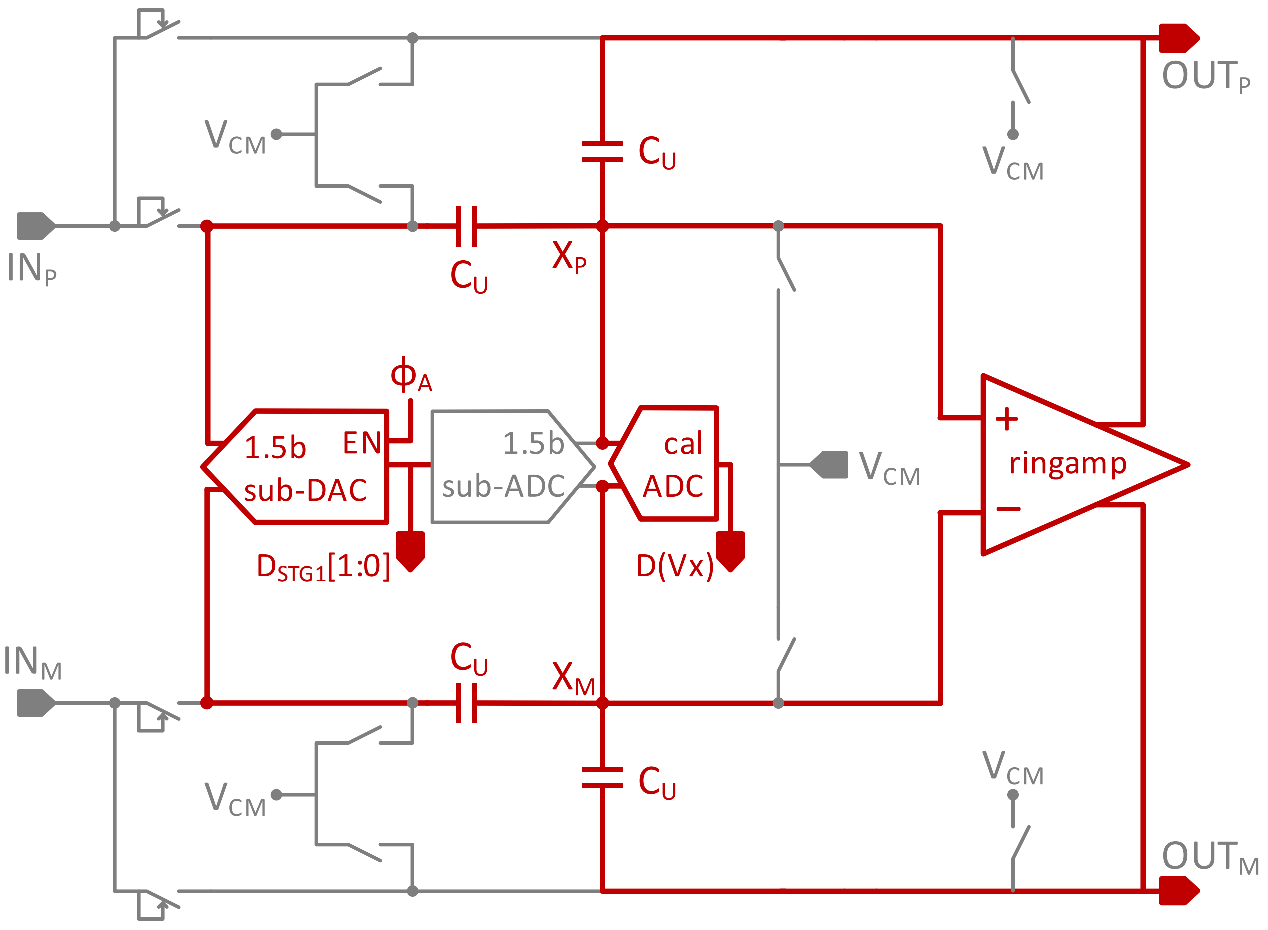


STAGE 1

SYSTEM OVERVIEW

- Track
- Quantize (Passive hold)
- Amplify

Phase 3: Amplify



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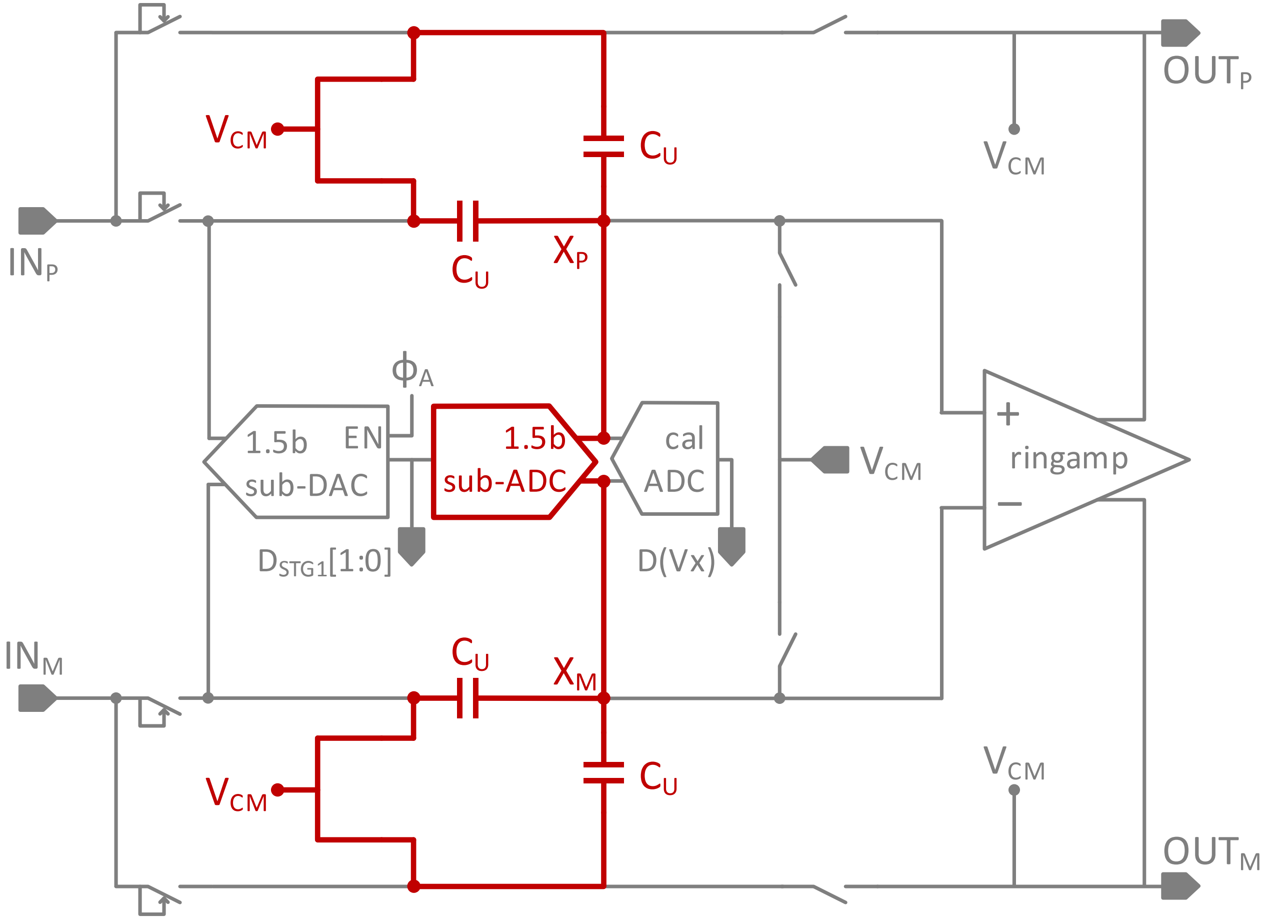
STAGE 1

SYSTEM OVERVIEW

- BENEFIT: Same capacitors used by sub-ADC *and* amplifier
    - No skew/bandwidth mismatch
    - No sub-ADC loading of input buffer

Phase 2: Quantize (Passive Hold)



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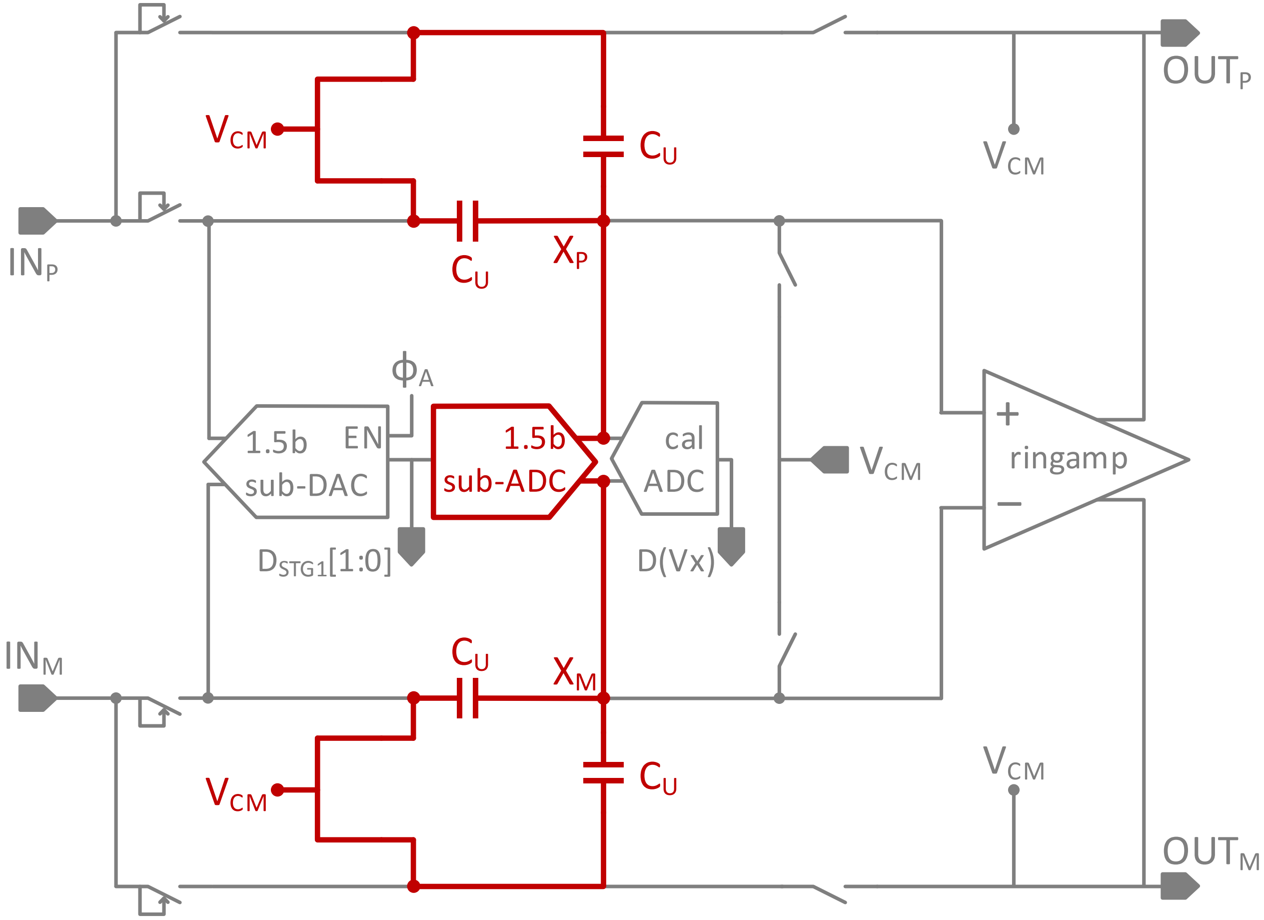
- BENEFIT: Same capacitors used by sub-ADC *and* amplifier
    - No skew/bandwidth mismatch
    - No sub-ADC loading of input buffer
- But: sub-ADC input capacitance must be minimized!

Phase 2: Quantize (Passive Hold)



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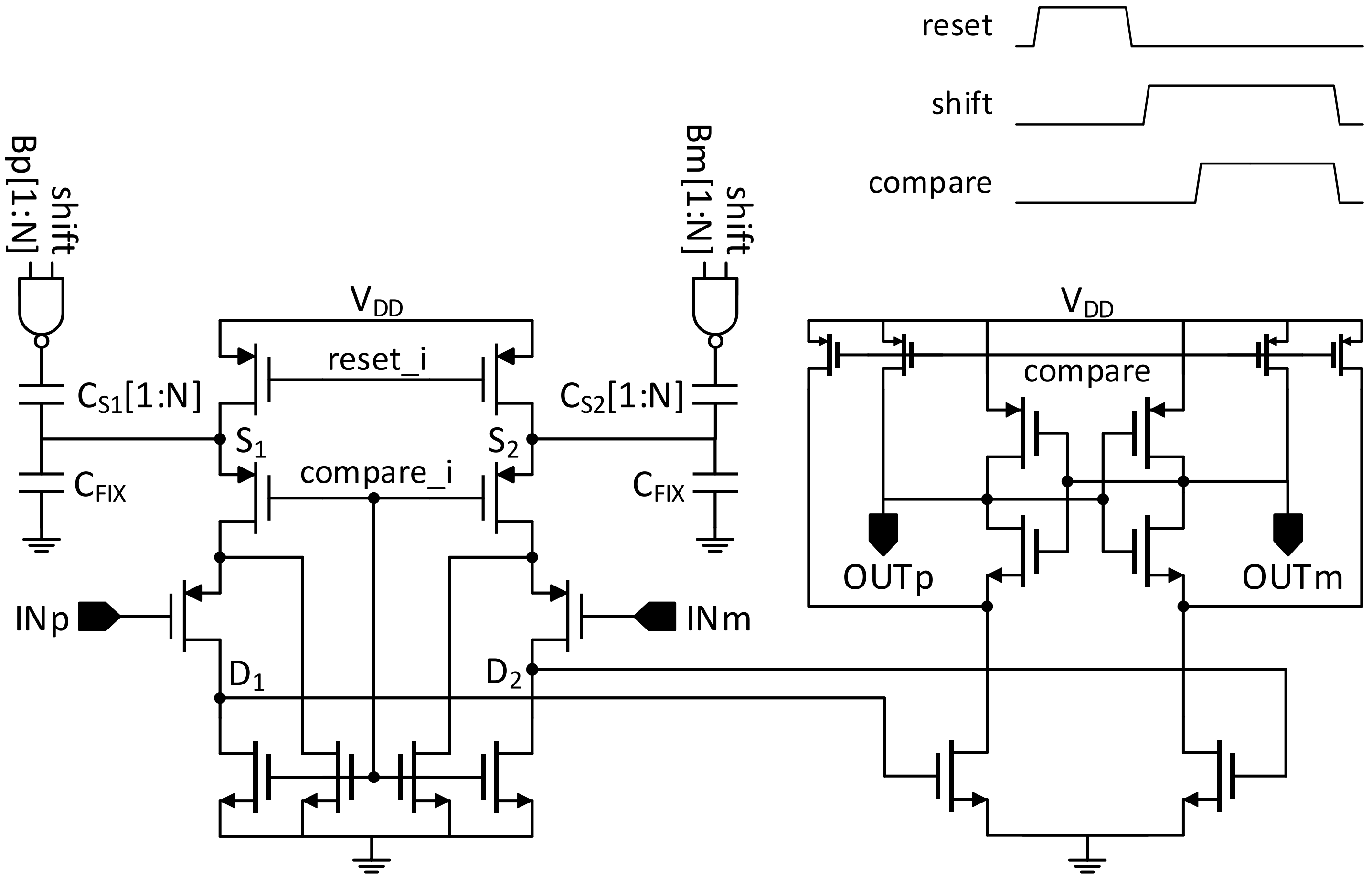
SPLIT-SOURCE COMPARATOR

SYSTEM OVERVIEW

- New “source-shifted” comparator architecture
  - Tiny input capacitance
  - Built-in threshold with wide tuning range
  - Very small decision delay
- Used in *all* sub-ADCs



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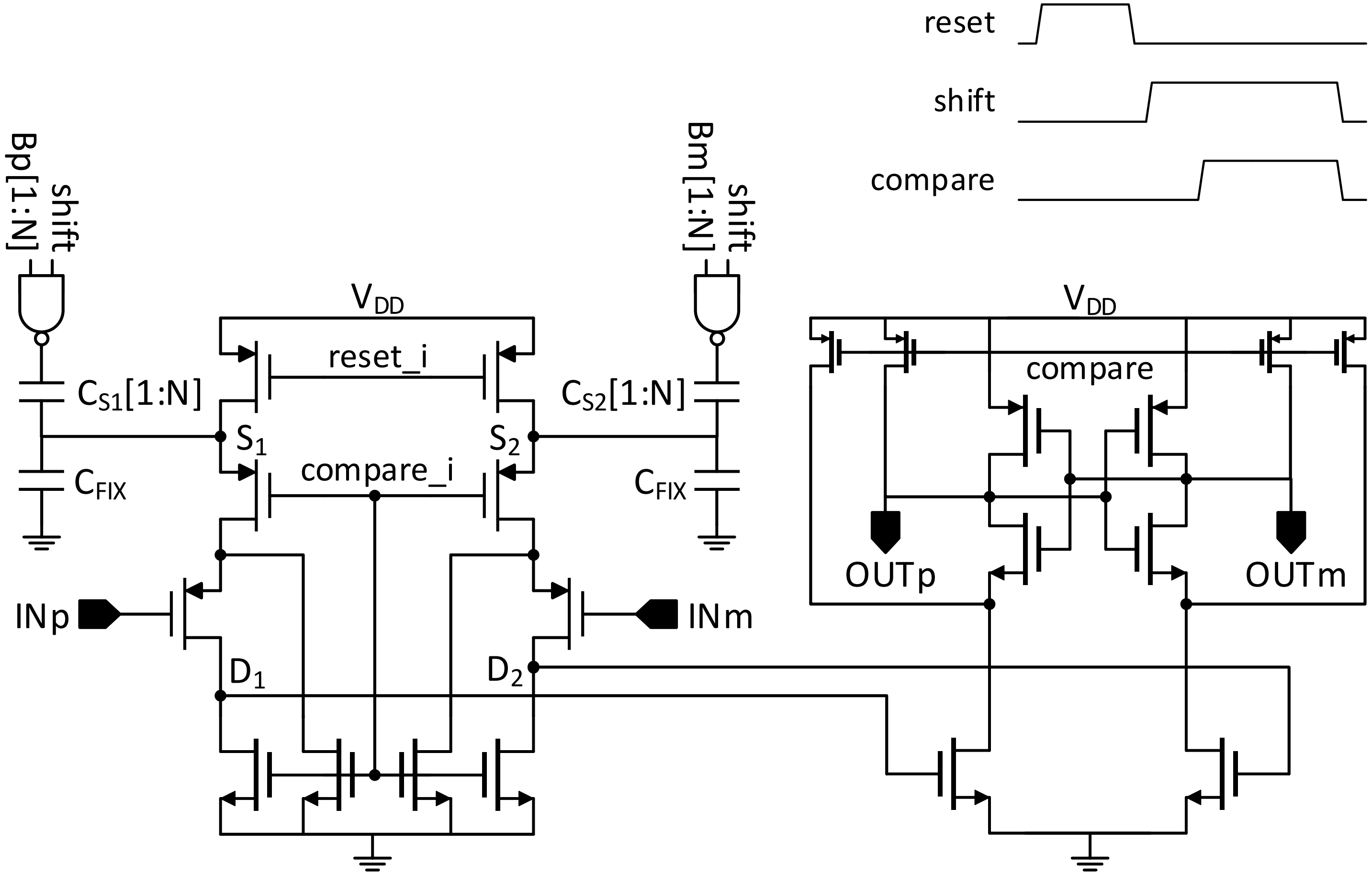
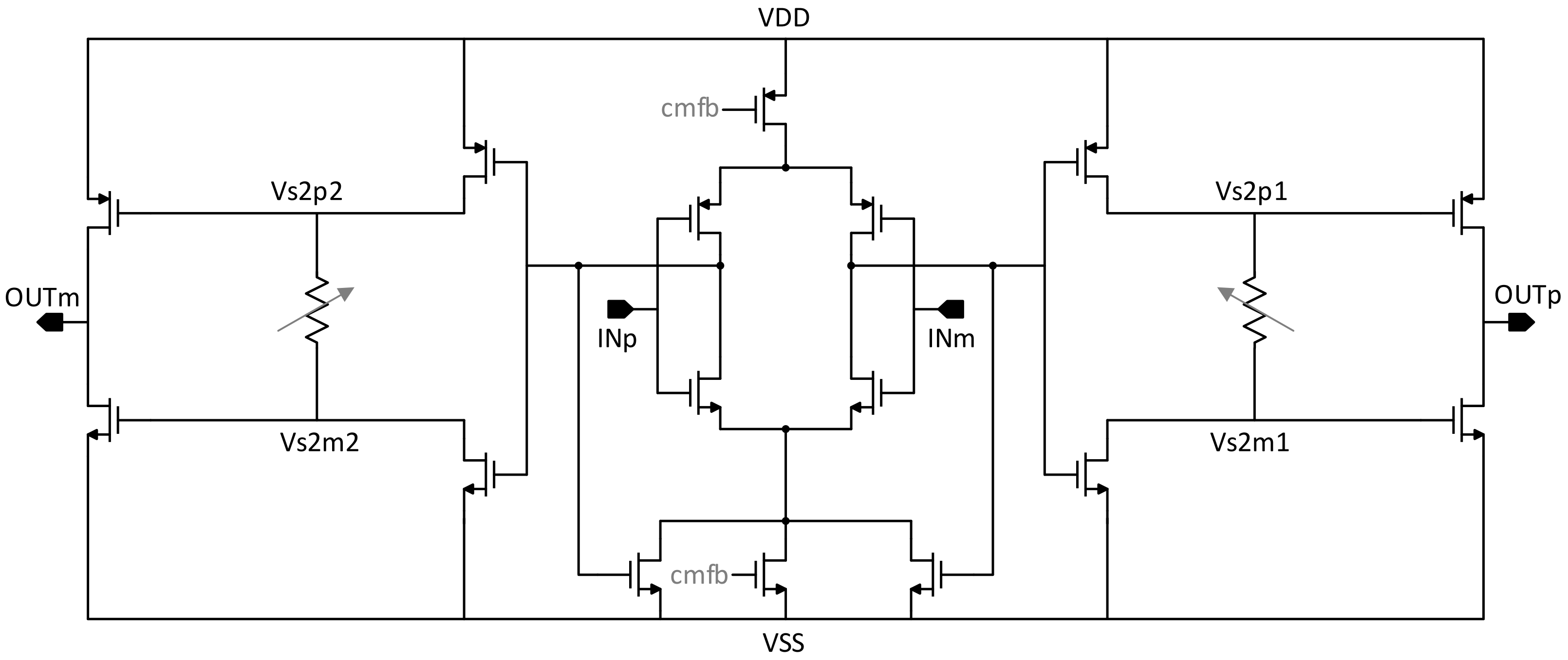


E. Martens et al., “Wide-tuning range programmable threshold comparator using capacitive source-voltage shifting”, Electronics Letters, Dec, 2018

RINGAMP

SYSTEM OVERVIEW

- Stabilized by dynamically forming a dominant output pole
- Fast
- Power efficient
- Wide swing
- Highly linear
- Inherently scalable



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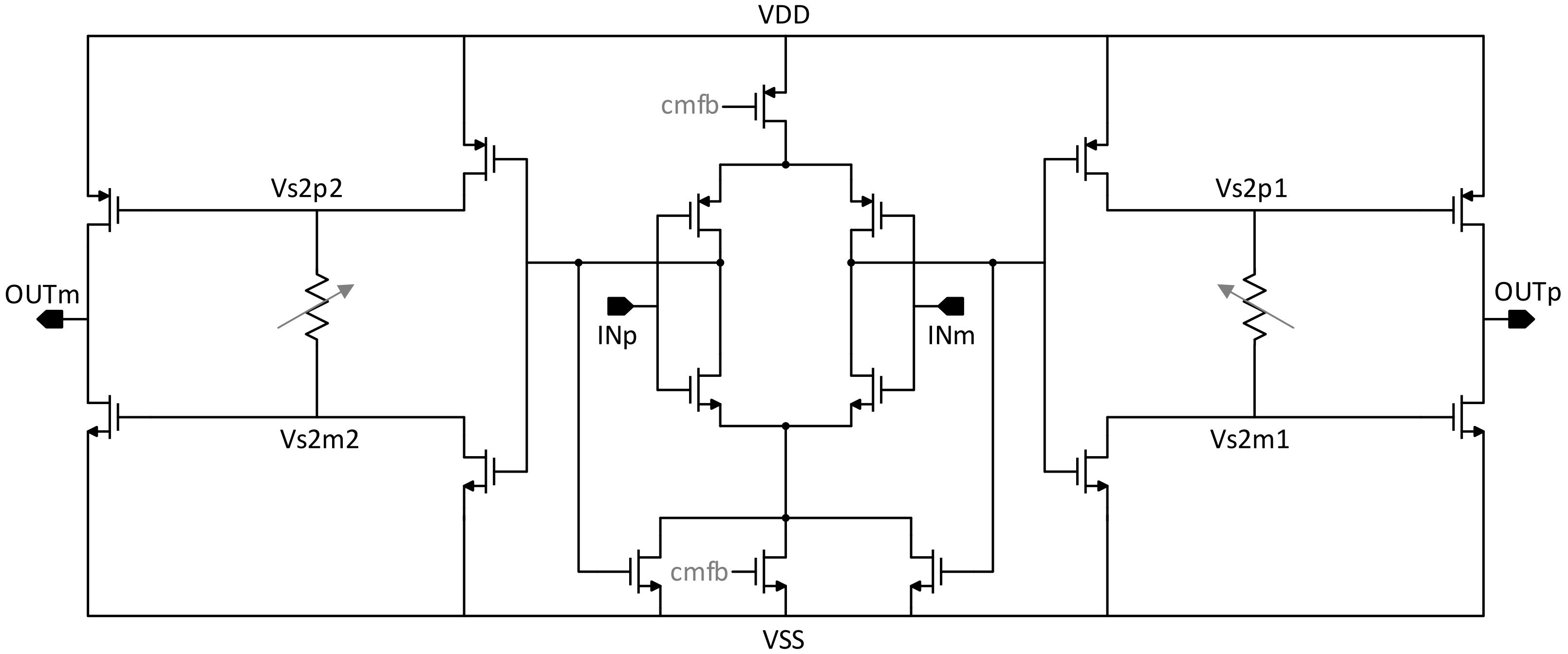

B. Hershberg, et. al. “Ring Amplifiers for Switched Capacitor Circuits” JSSC, Dec. 2012

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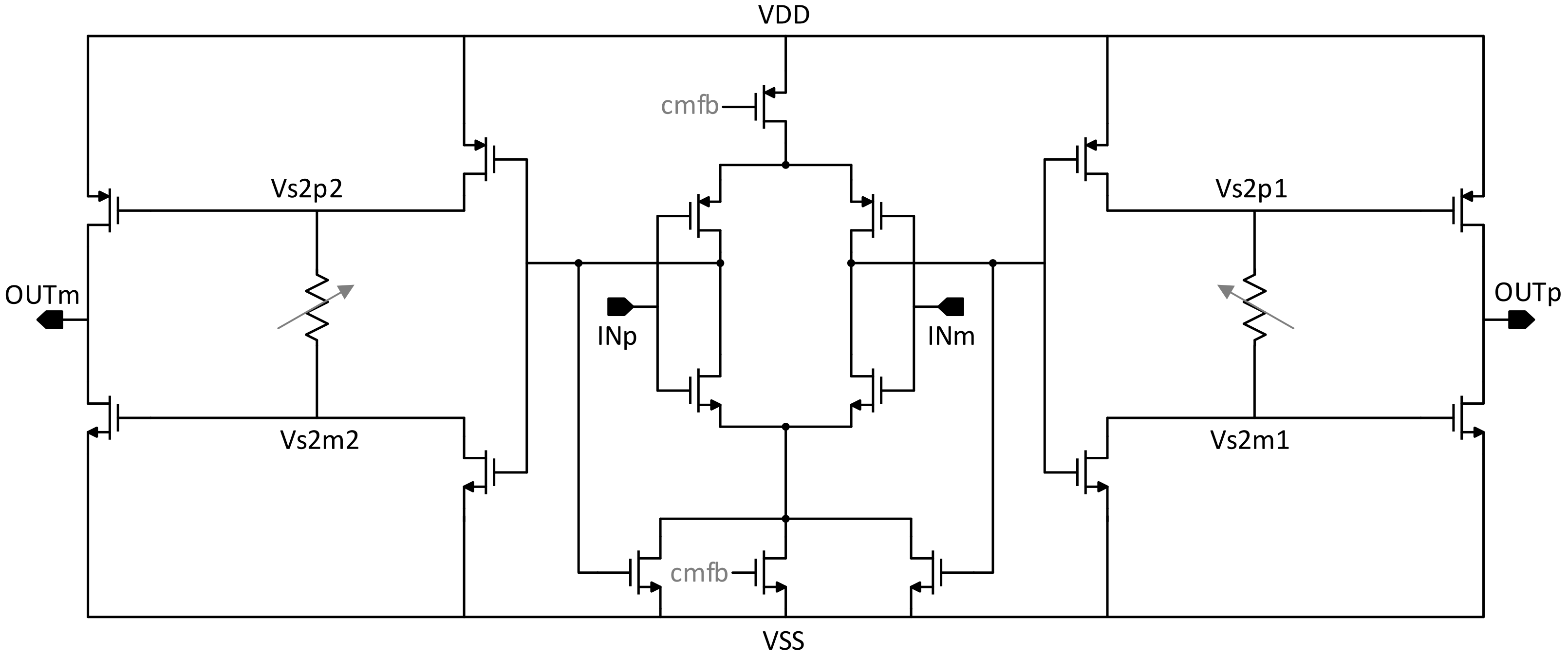

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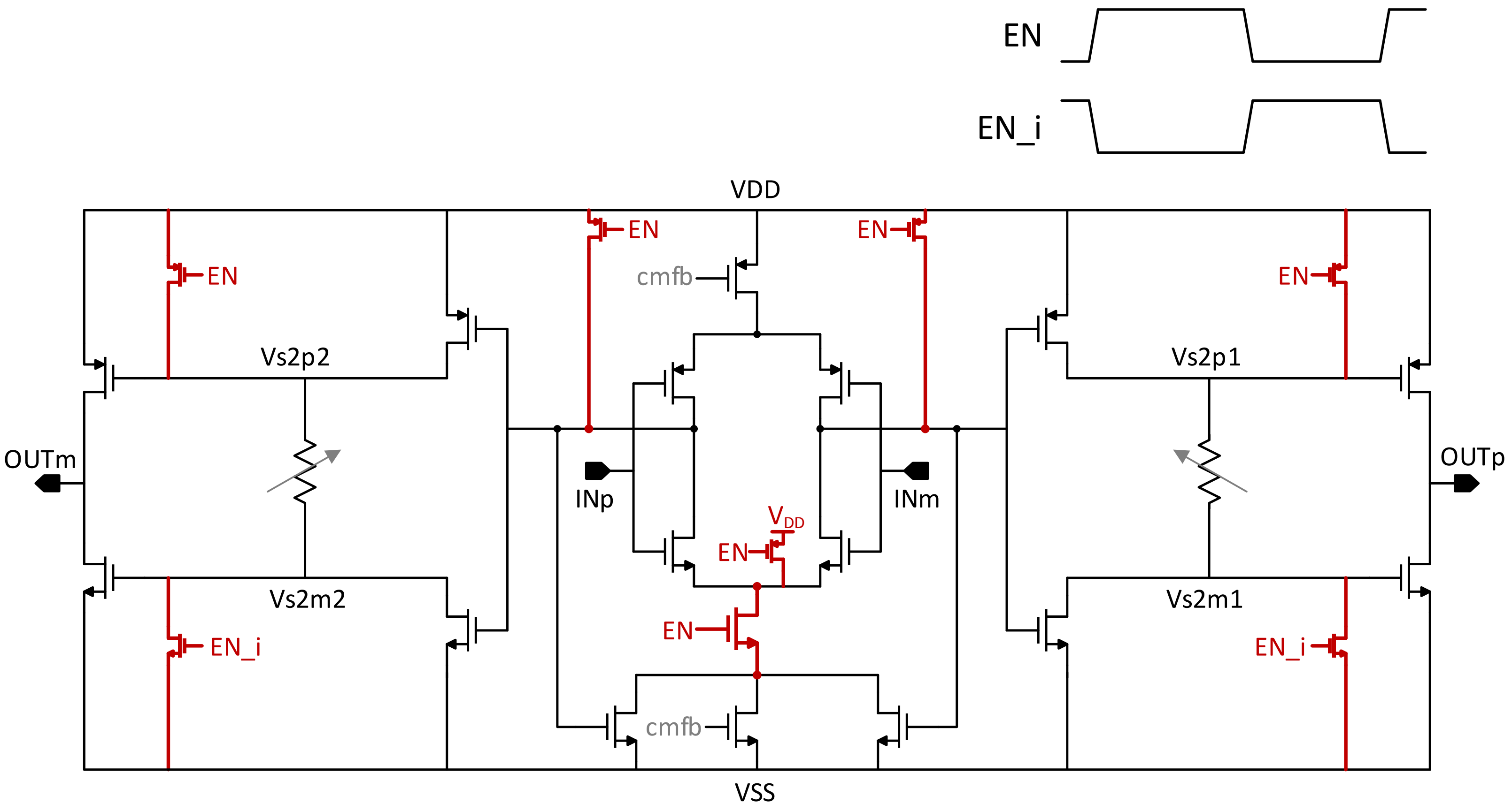
Y. Lim et. al., "A 1 mW 71.5 dB SNDR 50 MS/s 13 bit Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC" JSSC, Dec. 2015

RINGAMP

SYSTEM OVERVIEW

- Only powered during amplification phase
- Power-gating and pullup switches



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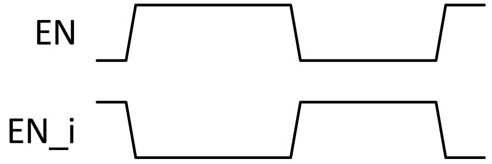
RINGAMP

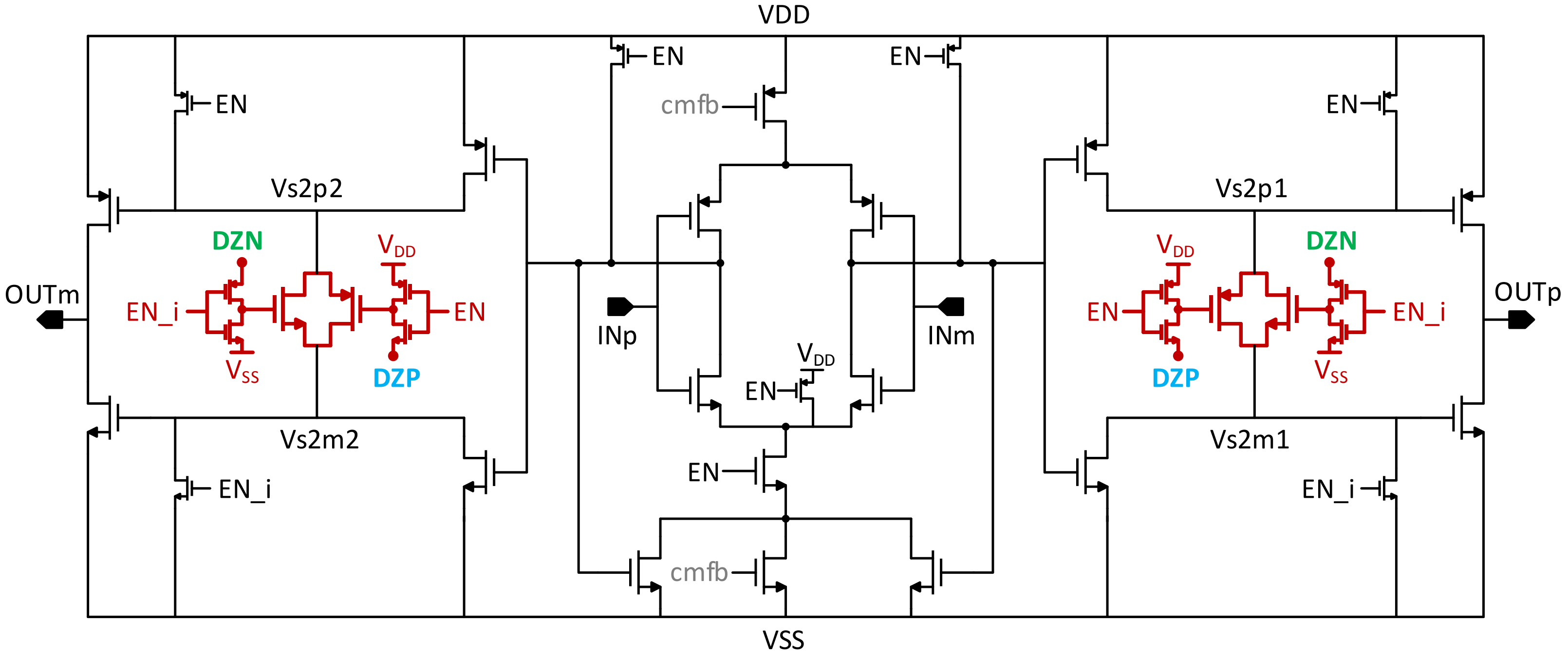
SYSTEM OVERVIEW

- Tunable CMOS resistor biasing

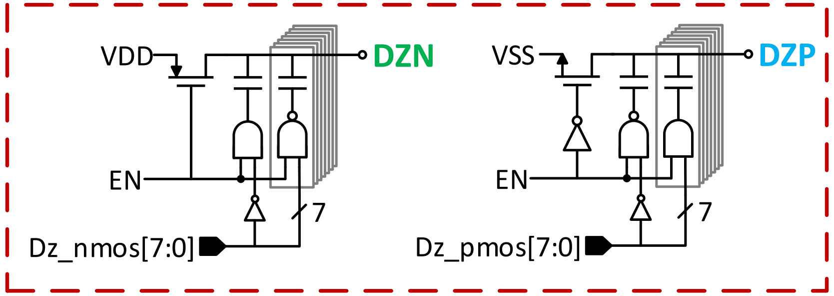
  J. Lagos, et. al. “A Single-Channel, 600-MS/s, 12-b, Ringamp-Based Pipelined ADC in 28-nm CMOS” JSSC, Feb. 2019

- Digitally controlled capacitor DACs bias the CMOS resistor with trapped-charge





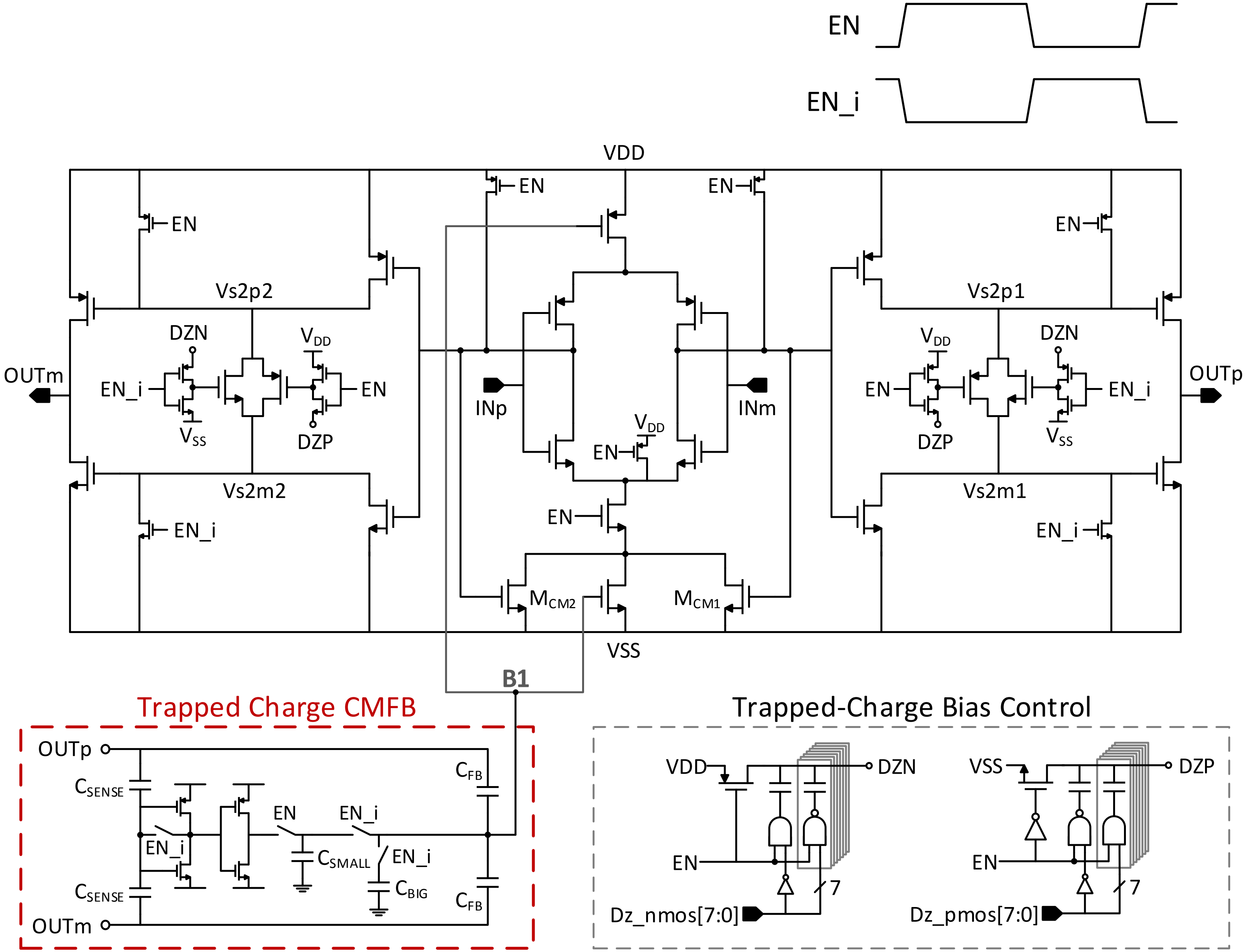
Trapped-Charge Bias Control



RINGAMP

SYSTEM OVERVIEW

- CMFB trapped-charge based biasing
- 3 CMFB loops
    - DC high-gain loop
    - AC low-gain loop
    - AC stabilizing loop



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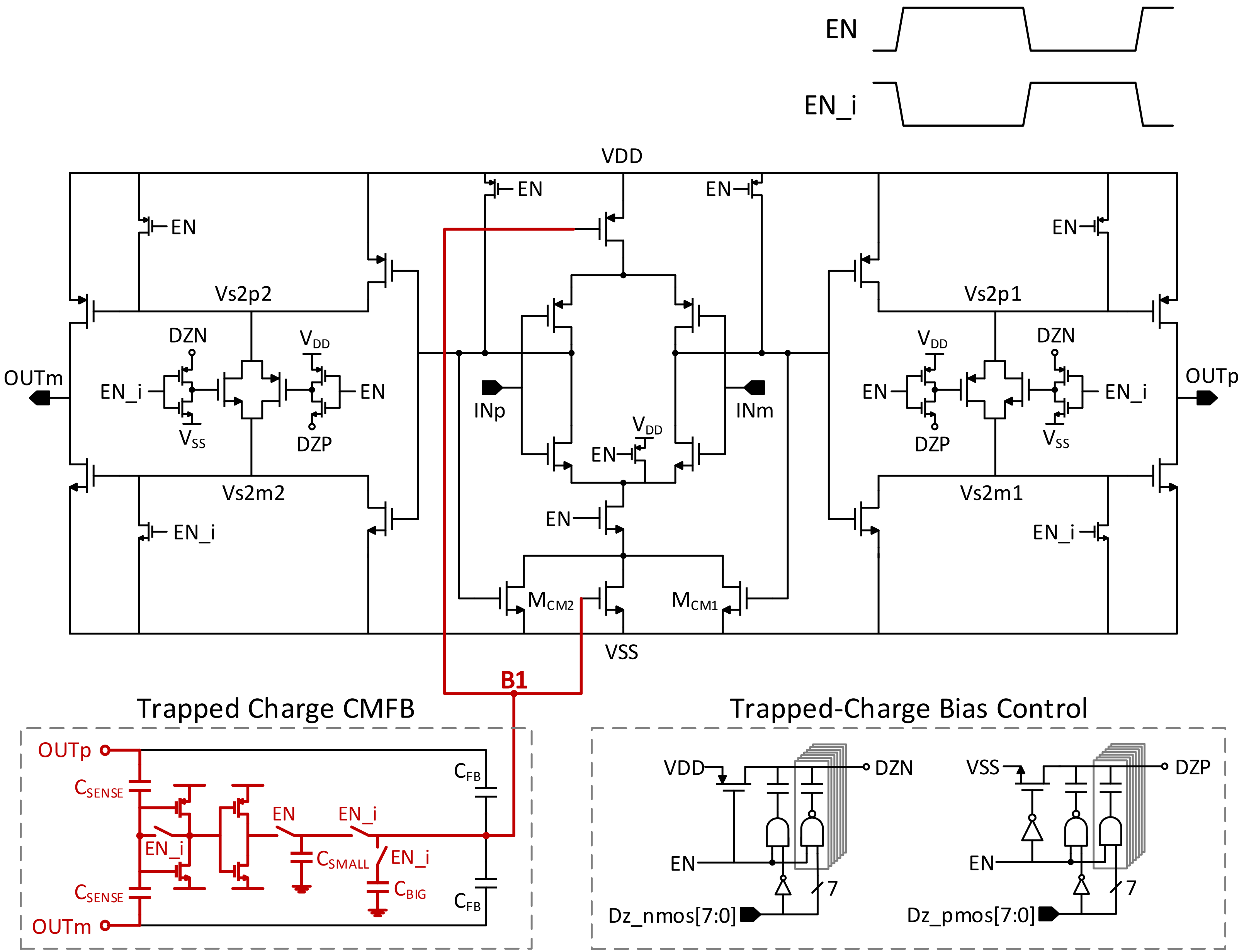

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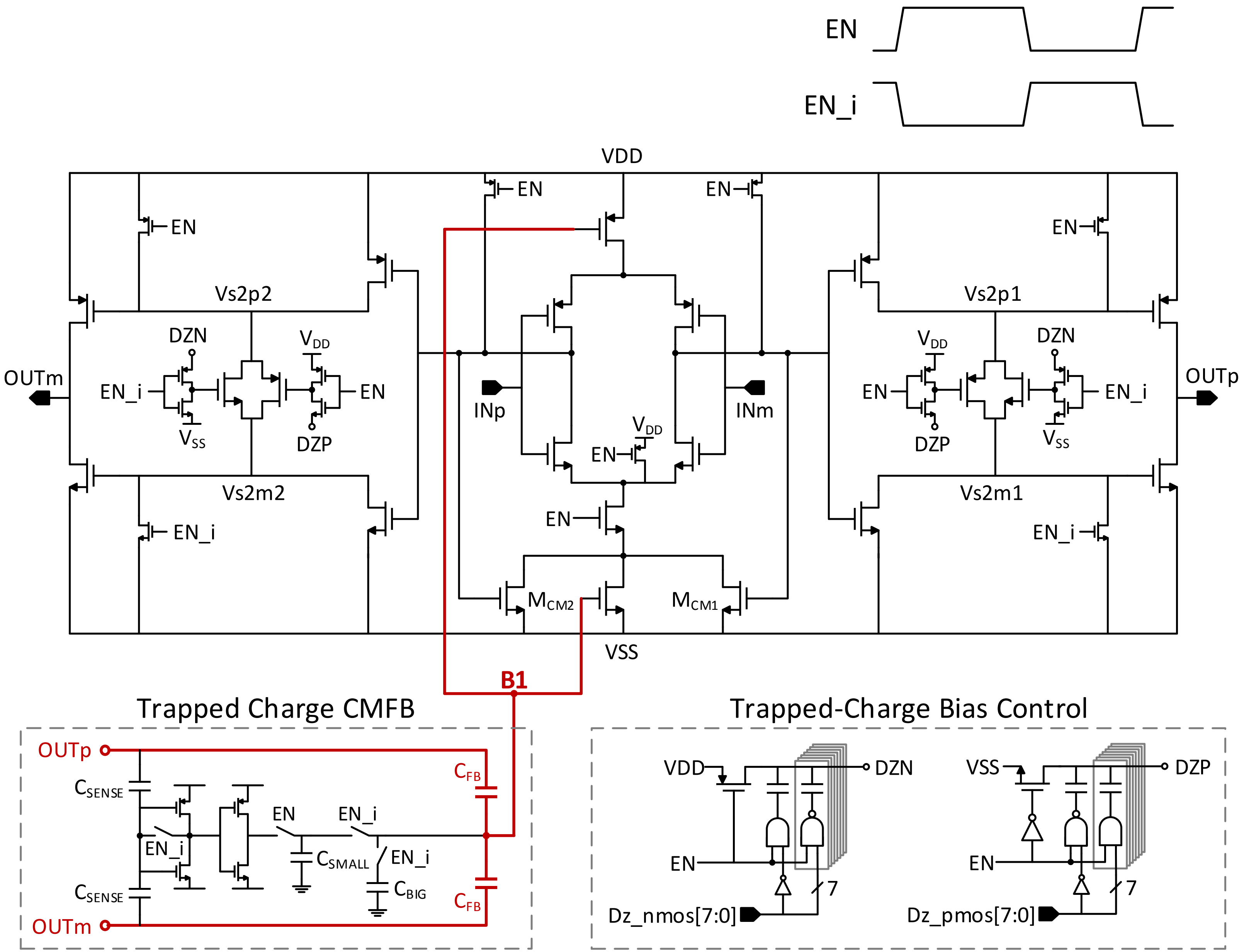

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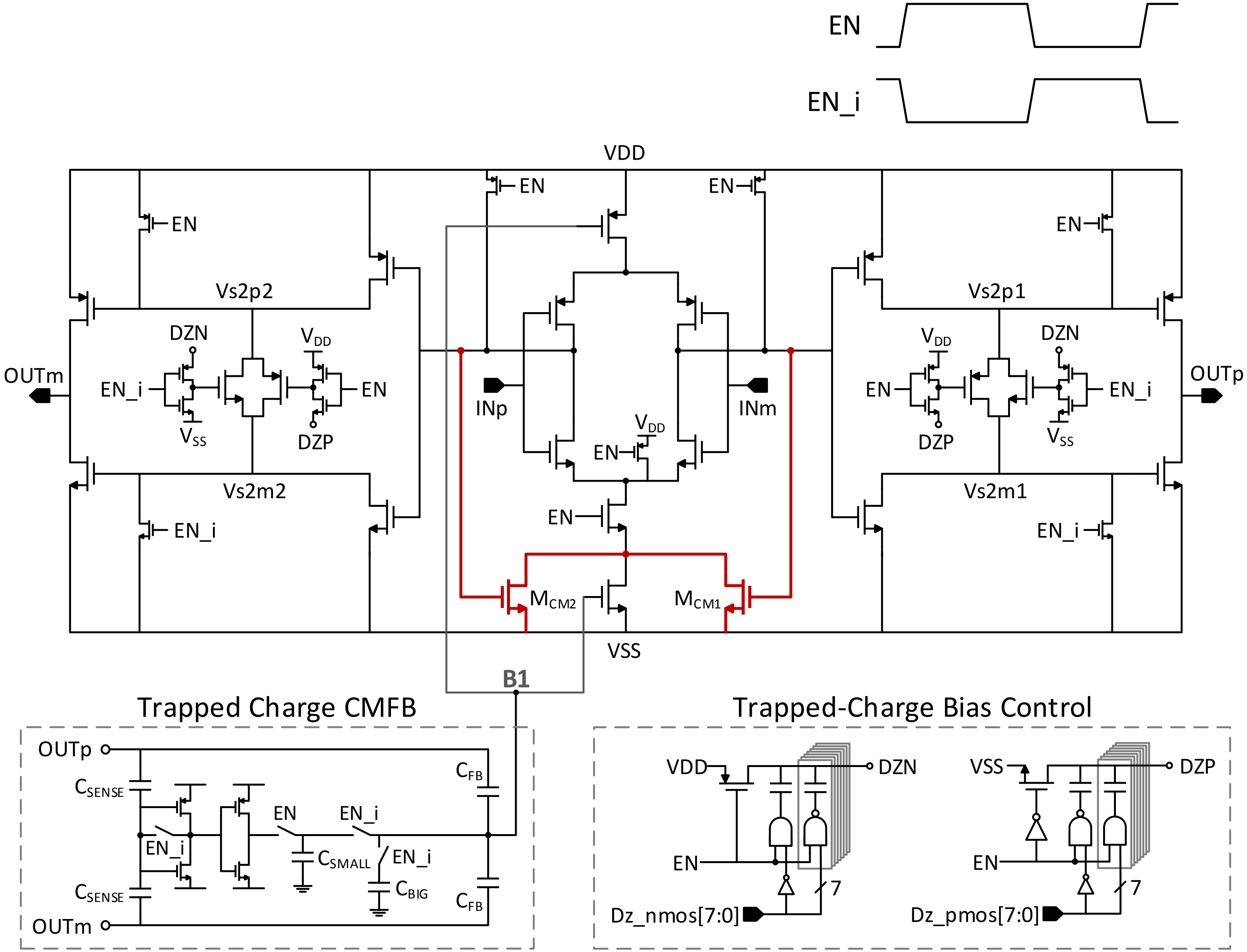

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MOTIVATION

SDR MONITORING

- Digitally controlled ringamp biasing
  - What is the optimal code?
  - How to track across PVT?

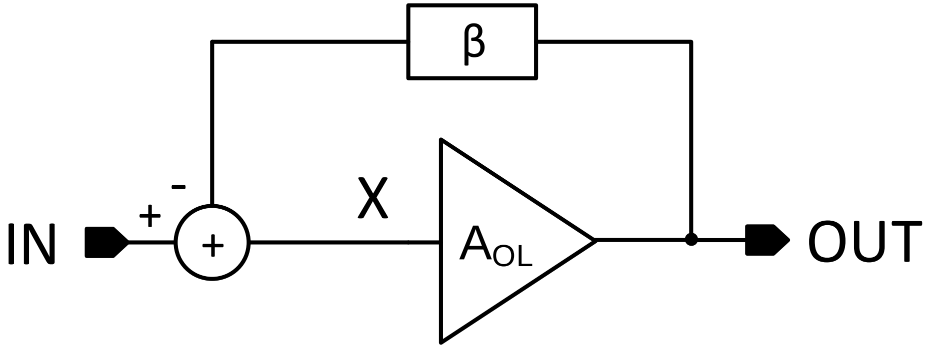
- Approach: measure the ringamp-related error and minimize
  - Interested in higher-order error terms
  - First-order gain error we can already correct with well known methods

CONCEPT

SDR MONITORING

- Residual error at V_X consists of two components:

$$V_X = \frac{V_{OUT}}{A_{OL}} + \varepsilon_{ND}$$



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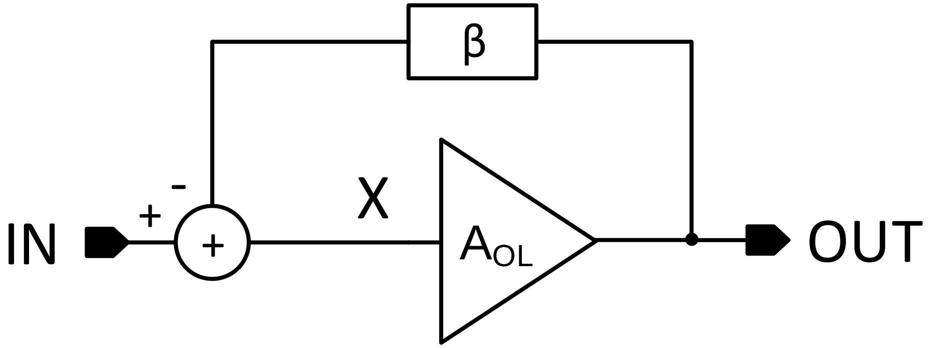
finite gain error



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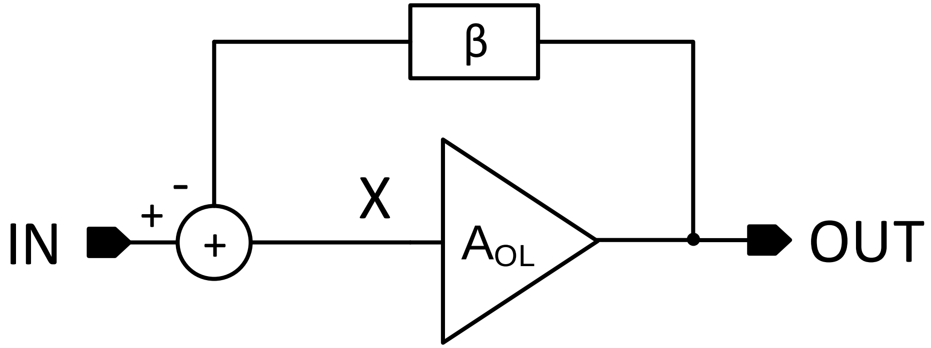
finite gain error

noise & distortion



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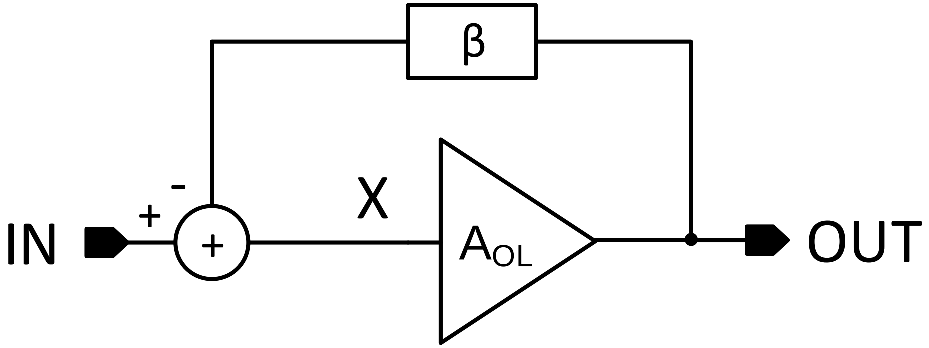

$$V_X = \frac{V_{OUT}}{A_{OL}} + \varepsilon_{ND}$$

...rearranging: $\varepsilon_{ND} = V_X - \frac{V_{OUT}}{A_{OL}}$

finite gain error ↗ (first term)

noise & distortion ↑

CONCEPT

SDR MONITORING

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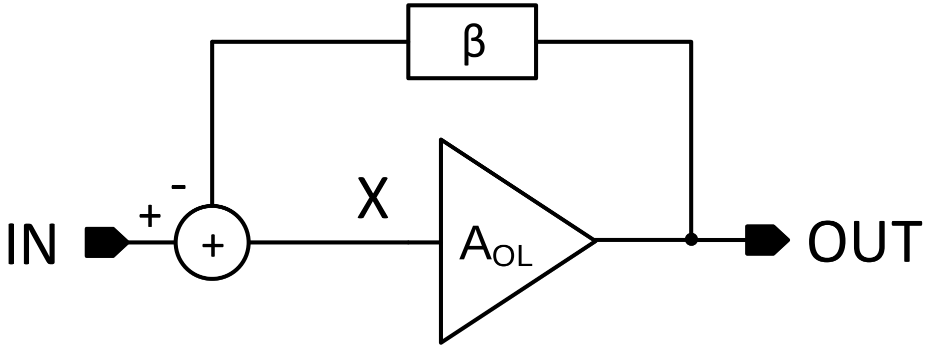

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finite gain error

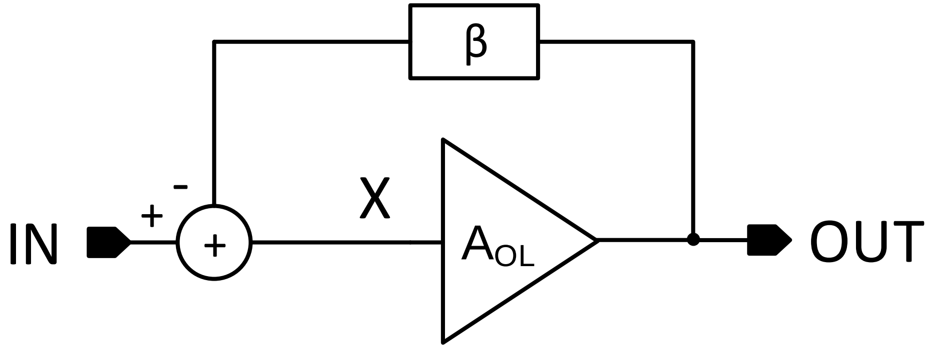
noise & distortion

...rearranging: $$\varepsilon_{ND} = V_X - \frac{V_{OUT}}{A_{OL}}$$

where: $$A_{OL} = avg\left(\frac{V_{OUT}}{V_X}\right)$$

CONCEPT

SDR MONITORING



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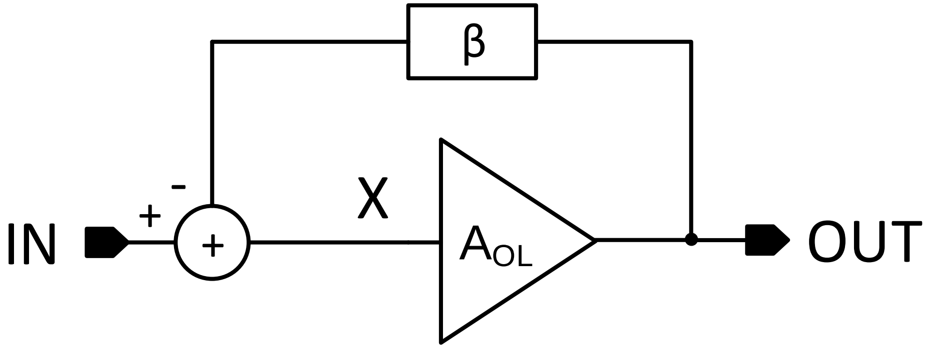
...rearranging: $$\varepsilon_{ND} = V_X - \frac{V_{OUT}}{A_{OL}}$$

- SNDR can be computed as:

$$SNDR_{dB} = 10\ log_{10}\left(\frac{\beta^2 \cdot var(V_{OUT})}{var(\varepsilon_{ND})}\right)$$

CONCEPT

SDR MONITORING



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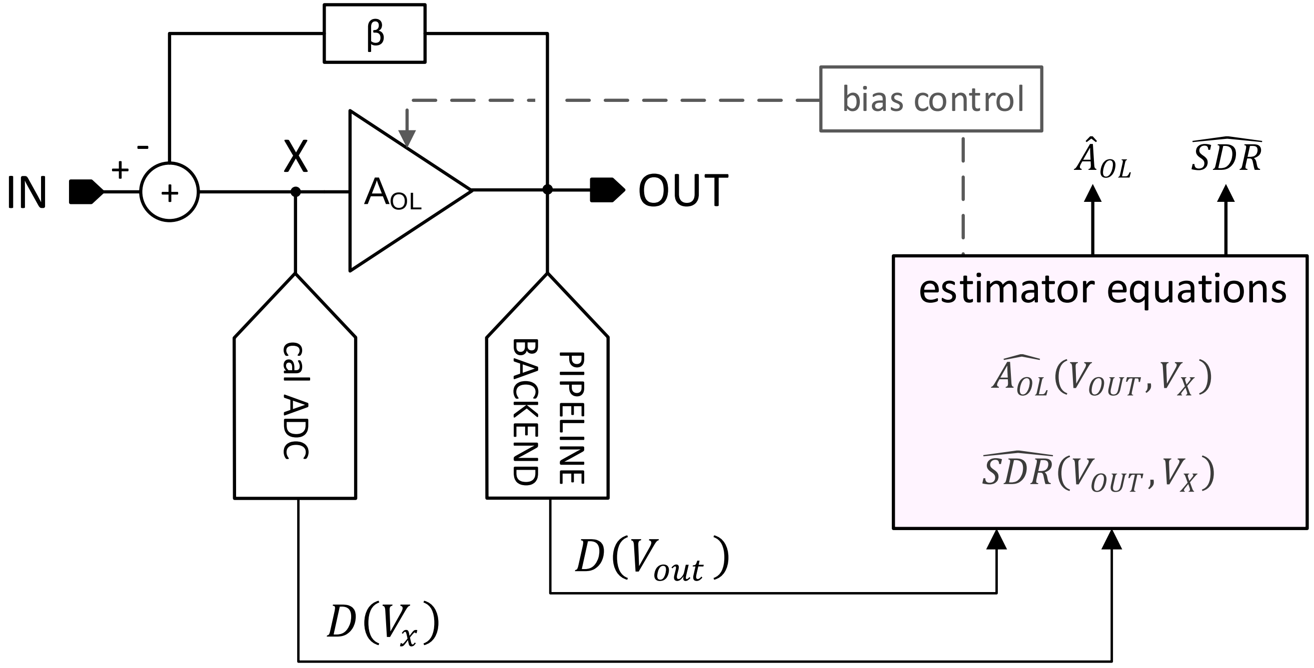
- SNDR can be computed as:

$$SNDR_{dB} = 10\ log_{10}\left(\frac{\beta^2 \cdot var(V_{OUT})}{var(\varepsilon_{ND})}\right) = 10\ log_{10}\left(\frac{\beta^2 \cdot var(V_{OUT})}{var(V_X - V_{OUT}/A_{OL})}\right)$$

CONCEPT

SDR MONITORING

- Need to know voltages at nodes X and OUT
  - OUT: pipeline backend
  - X: extra ADC needed



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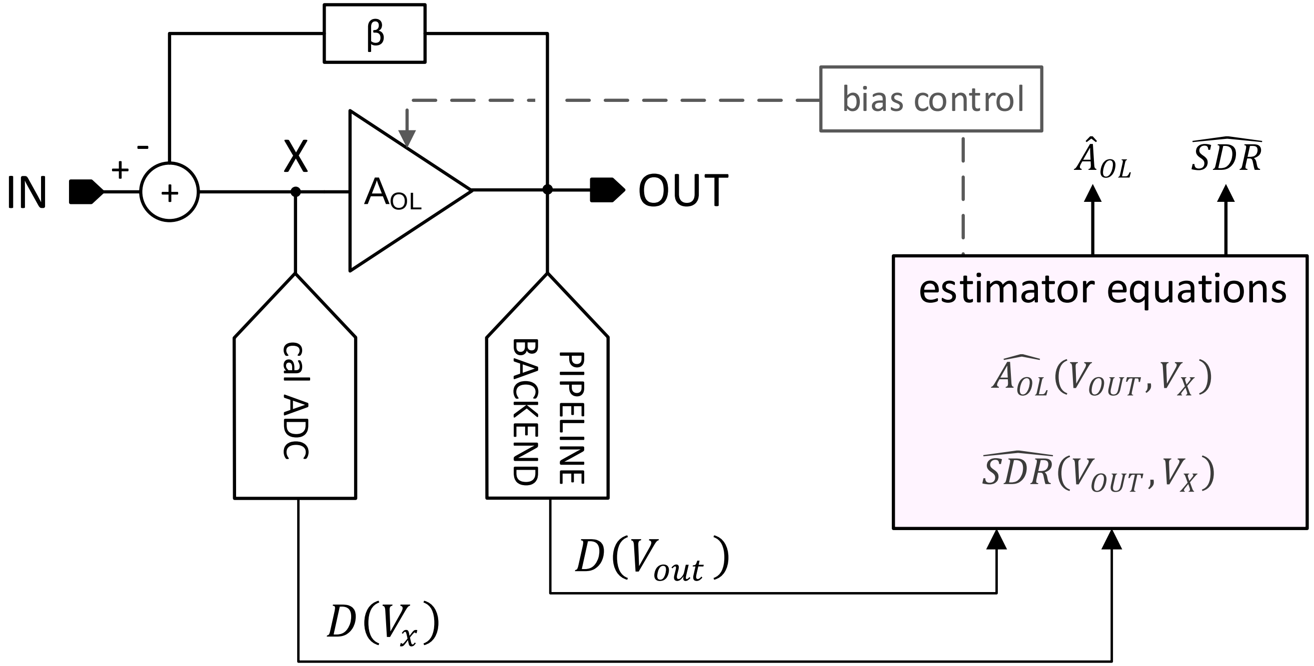
    - small input signal range (~1mV)
    - high accuracy
    - small hardware footprint



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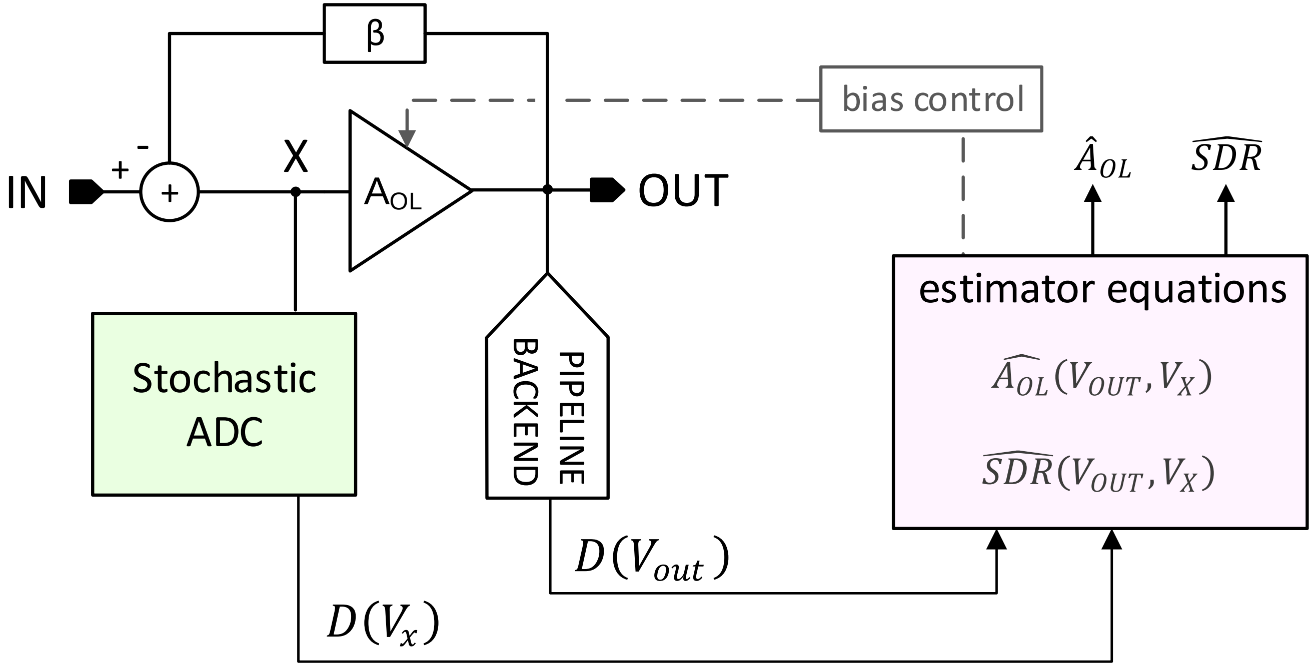


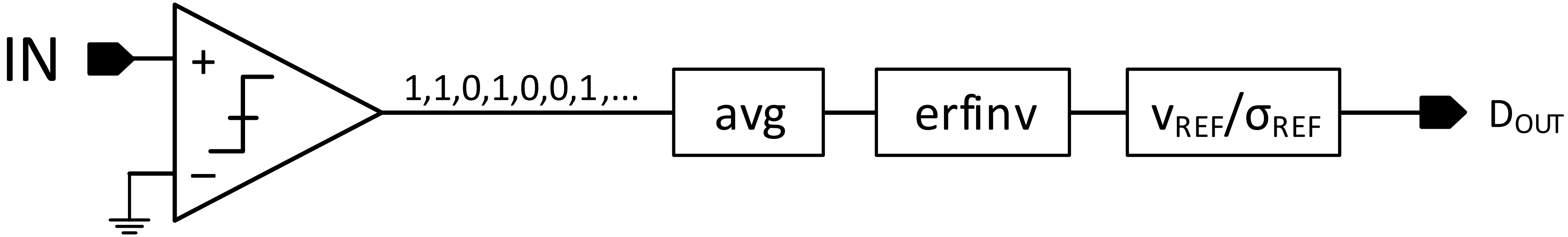
Single comparator stochastic ADC!

3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

CONCEPT

STOCHASTIC ADC

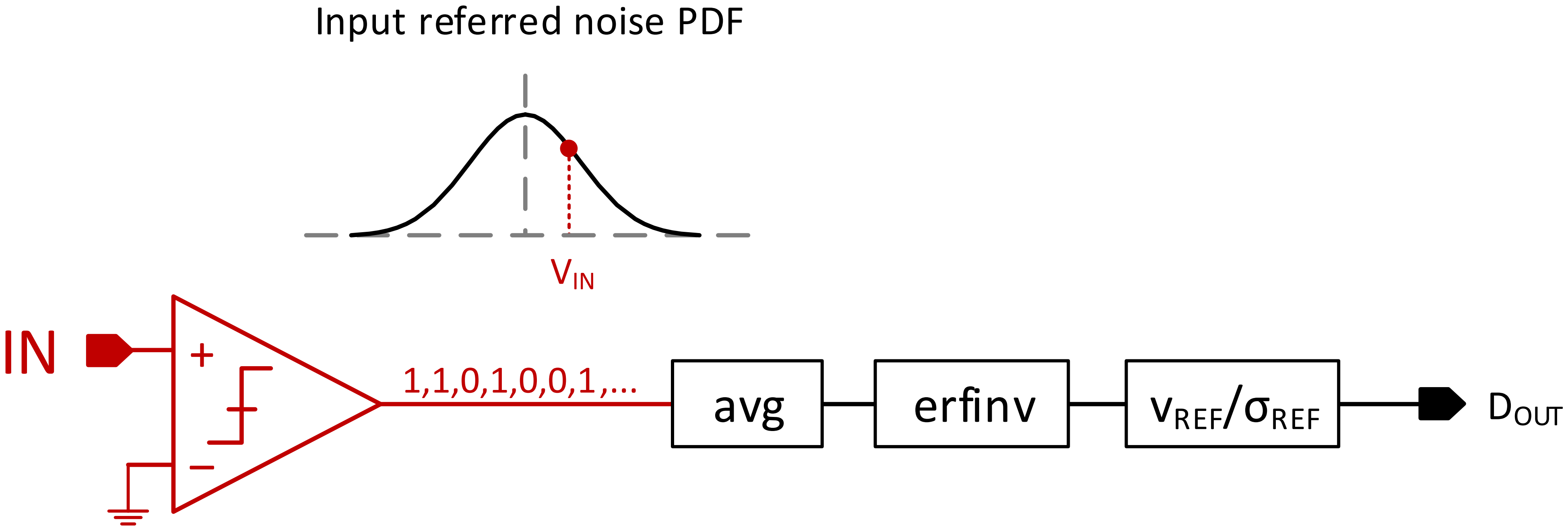
- Basic idea: use comparator's gaussian noise distribution to quantize



[B. Verbruggen, JSSC, Sept. 2015]

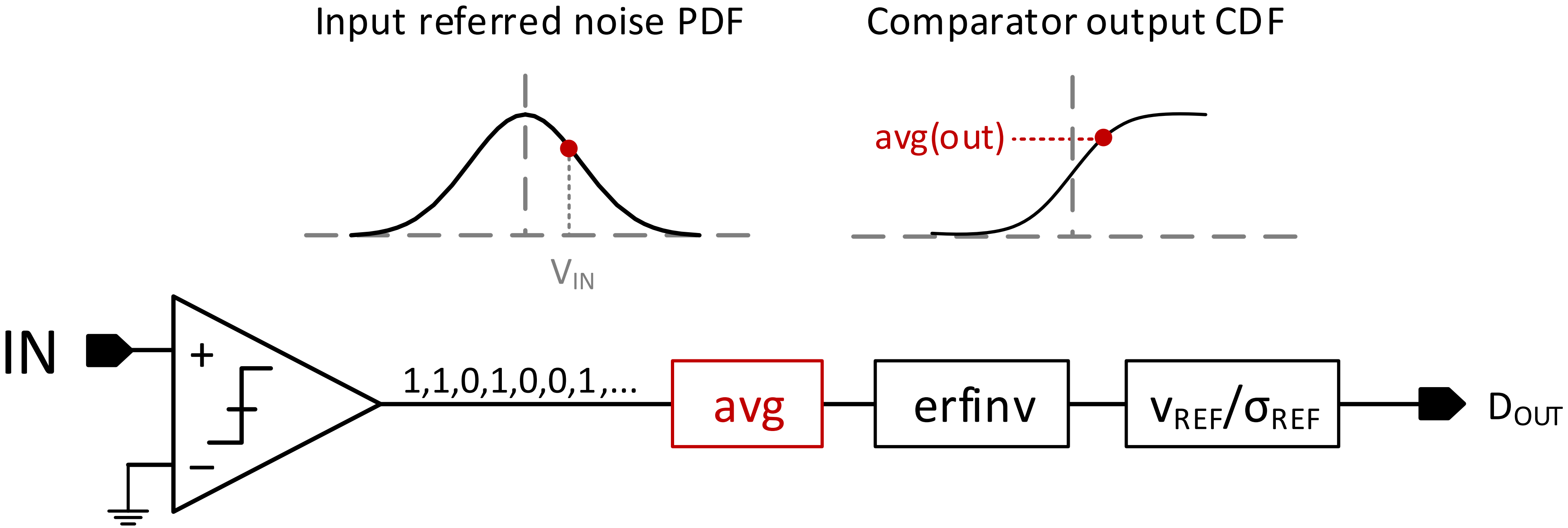
CONCEPT

STOCHASTIC ADC



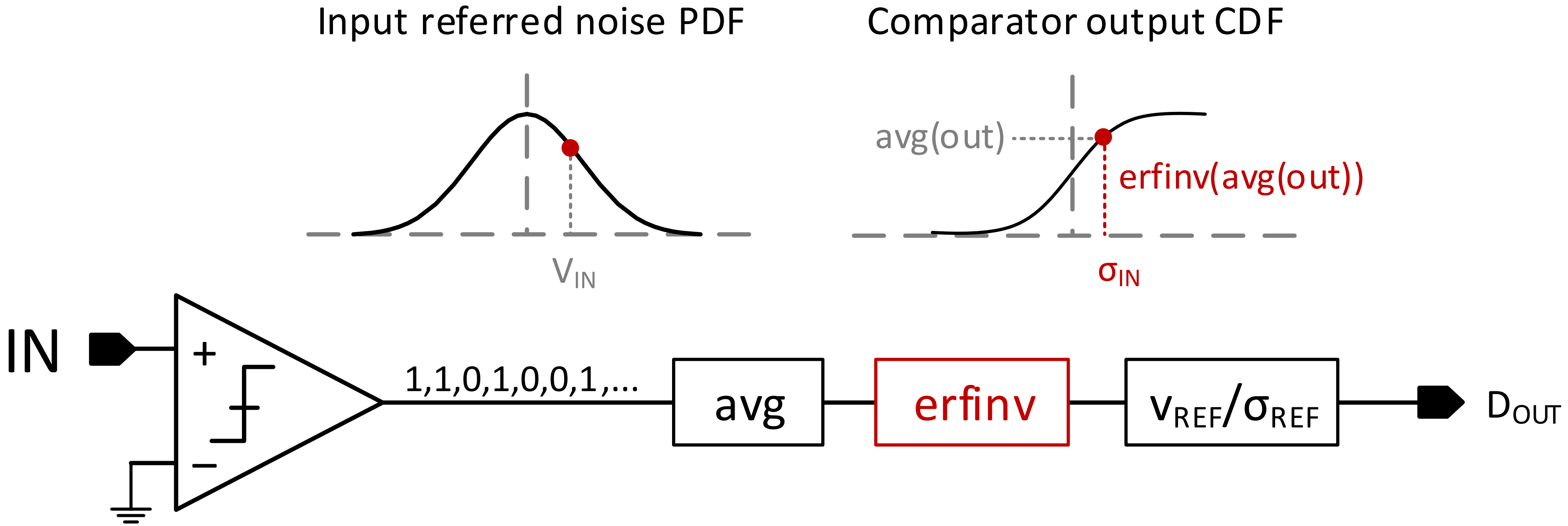
CONCEPT

STOCHASTIC ADC



CONCEPT

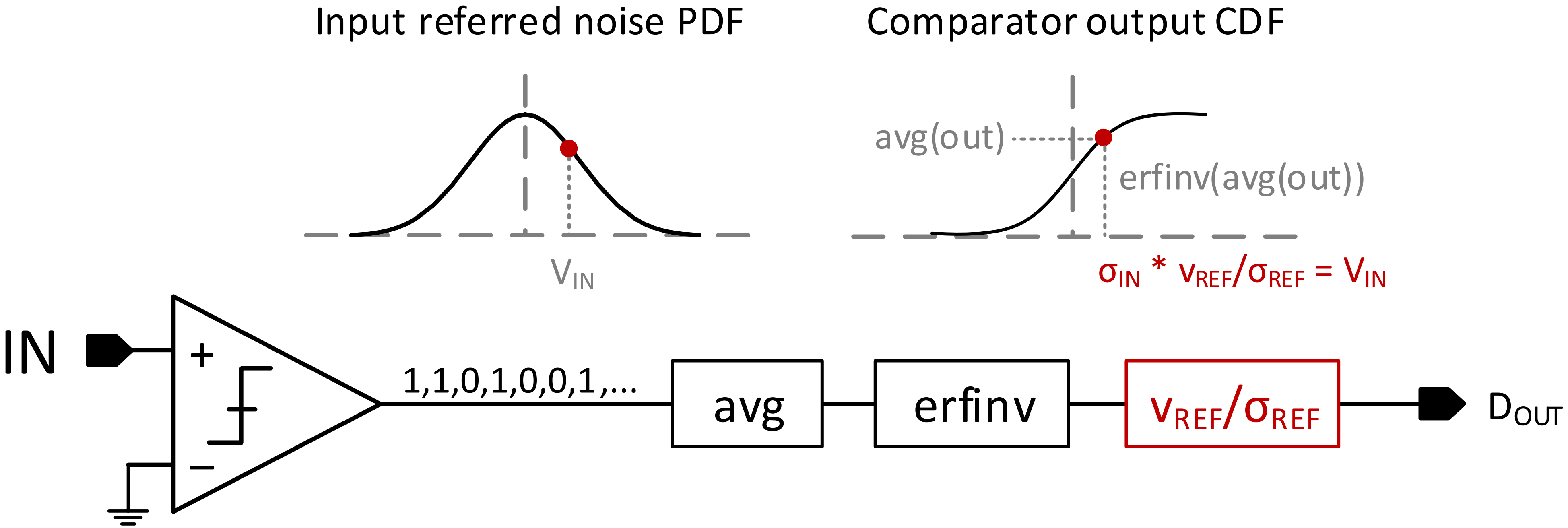
STOCHASTIC ADC



3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

CONCEPT

STOCHASTIC ADC



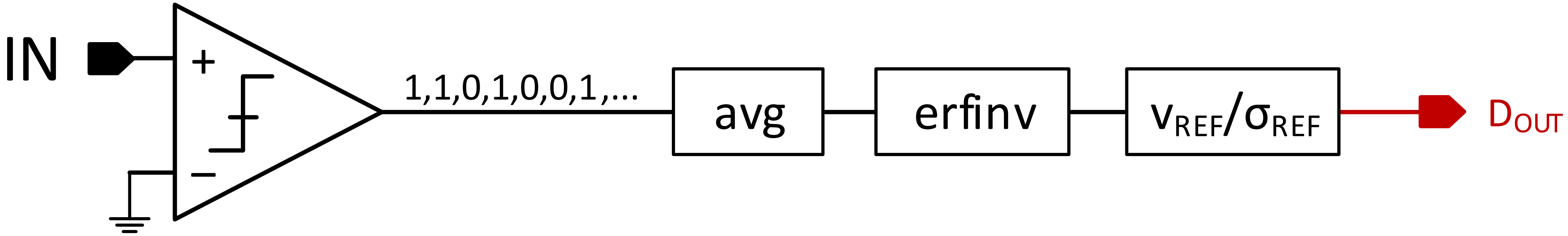
3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

CONCEPT

STOCHASTIC ADC

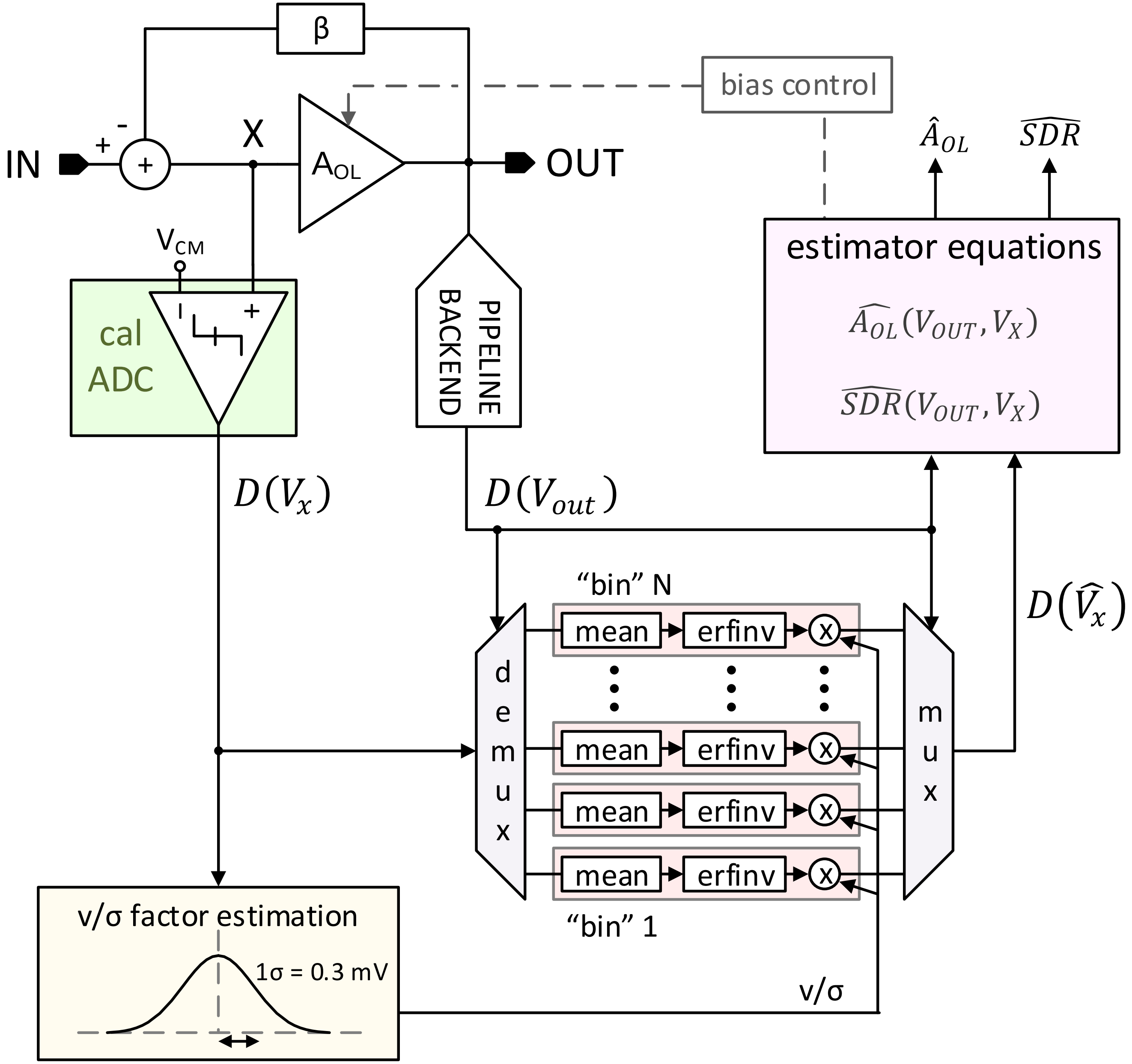
- Digital output represents the *average* value of V_{IN}
  - Noise in V_{IN} is attenuated

- Our SNDR estimator, stripped of noise, becomes an SDR measurement



OPERATION

SDR MONITORING

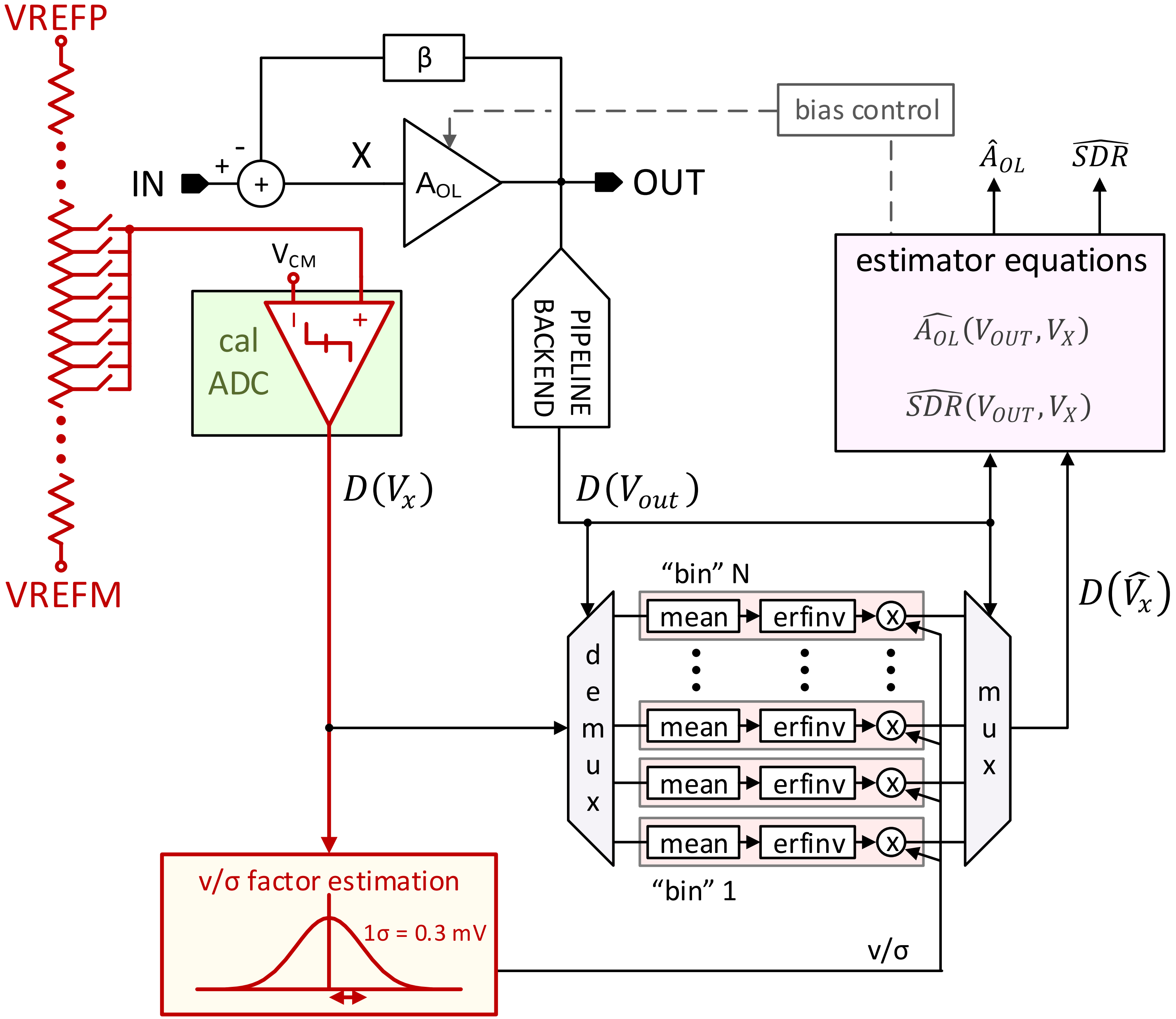


3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

OPERATION

SDR MONITORING

- Preparation step #1
  - Measure comparator's noise sigma in terms of known reference voltages
  - Provides volts-per-sigma conversion factor needed later

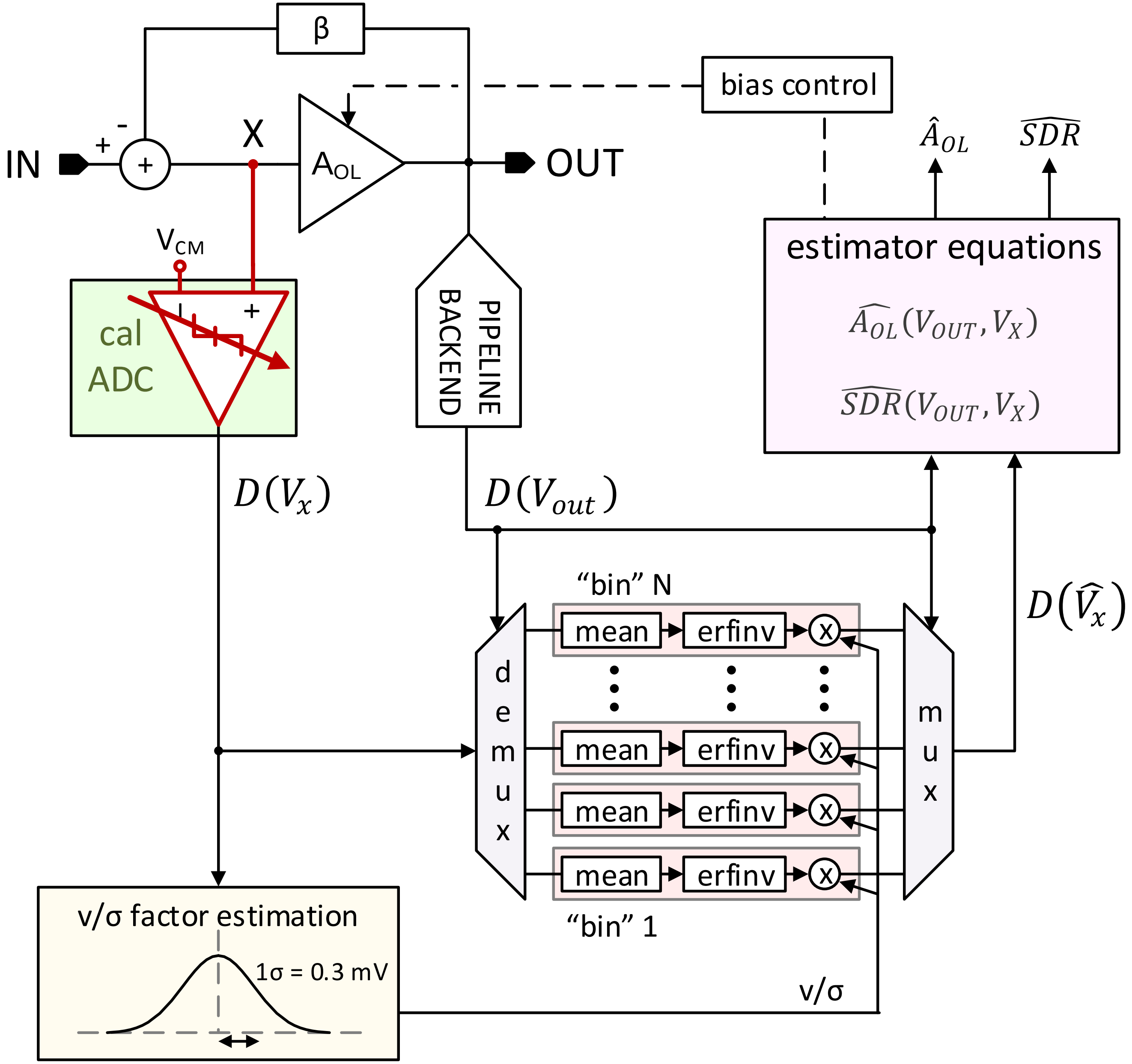


3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

OPERATION

SDR MONITORING

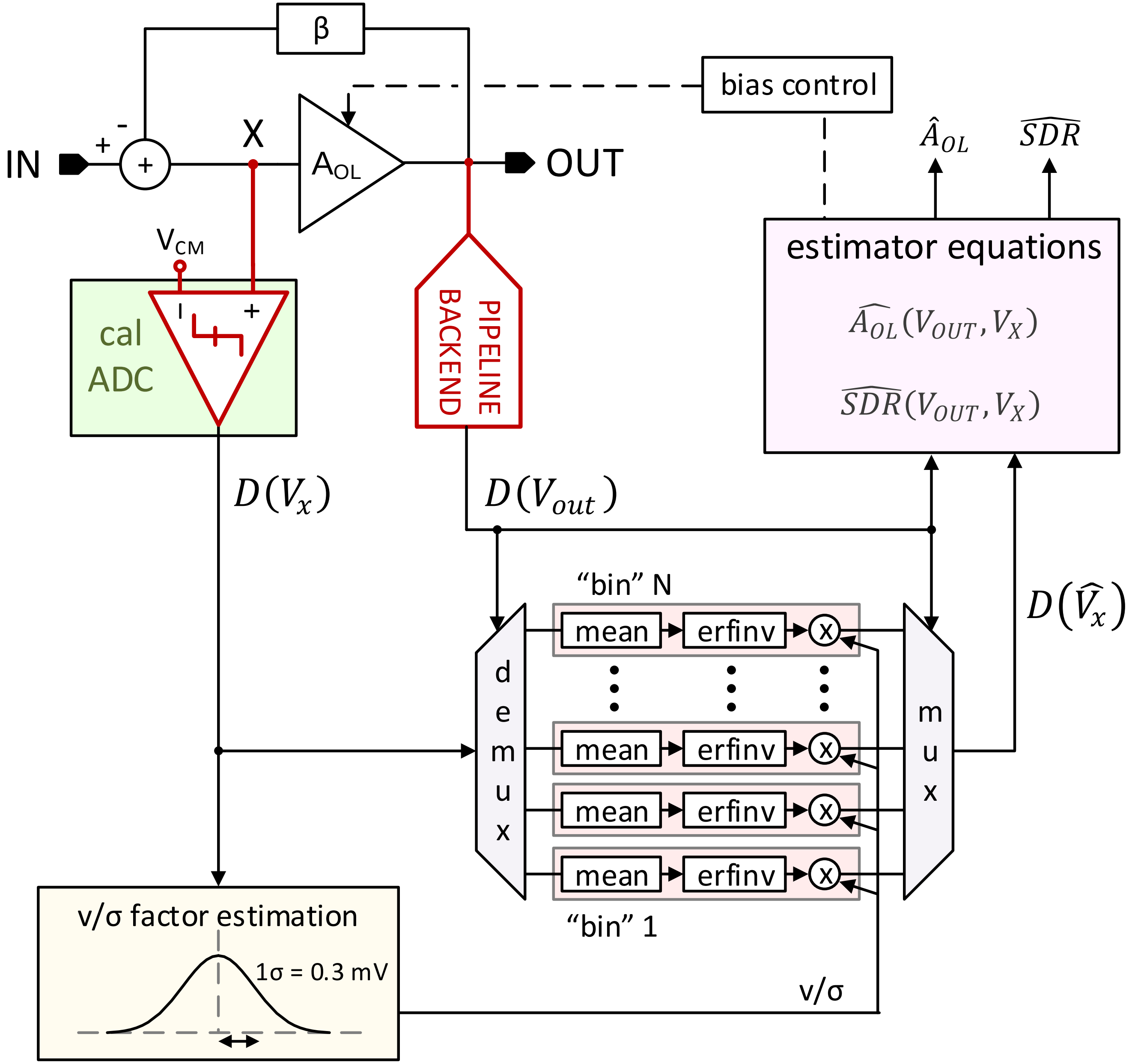
- Preparation step #1
  - Measure comparator’s noise sigma in terms of known reference voltages
  - Provides volts-per-sigma conversion factor needed later
- Preparation step #2
  - Null the comparator’s own offset



OPERATION

SDR MONITORING

- The two ADCs output $D(V_x)$ and $D(V_{out})$

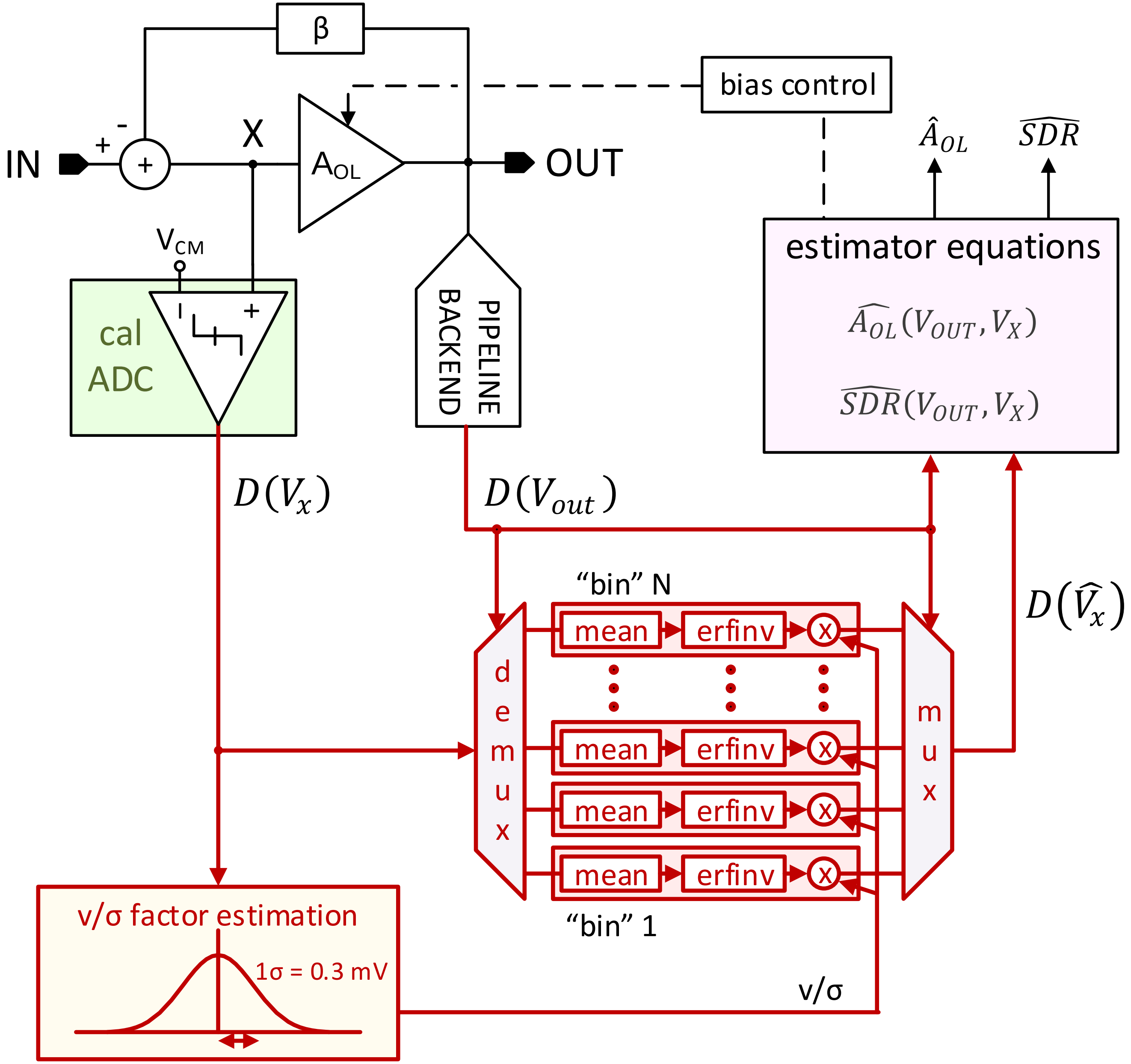


3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

OPERATION

SDR MONITORING

- Data is accumulated by sorting D(V_X) w.r.t. D(V_{out}) into “bins”



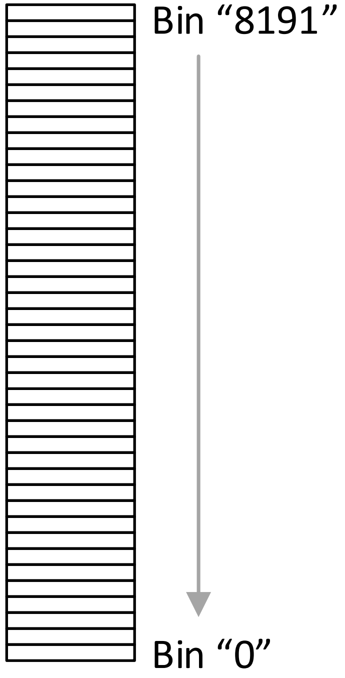
OPERATION

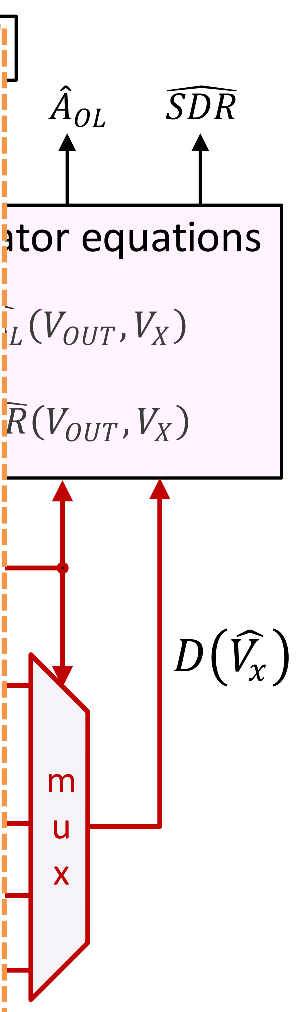
SDR M

- Data
  sortin
  into “

Data “binning” concept

D(V_{OUT})	321	421	6123	2931	5421	7216	3328
D(V_X)	1	1	0	1	0	0	1



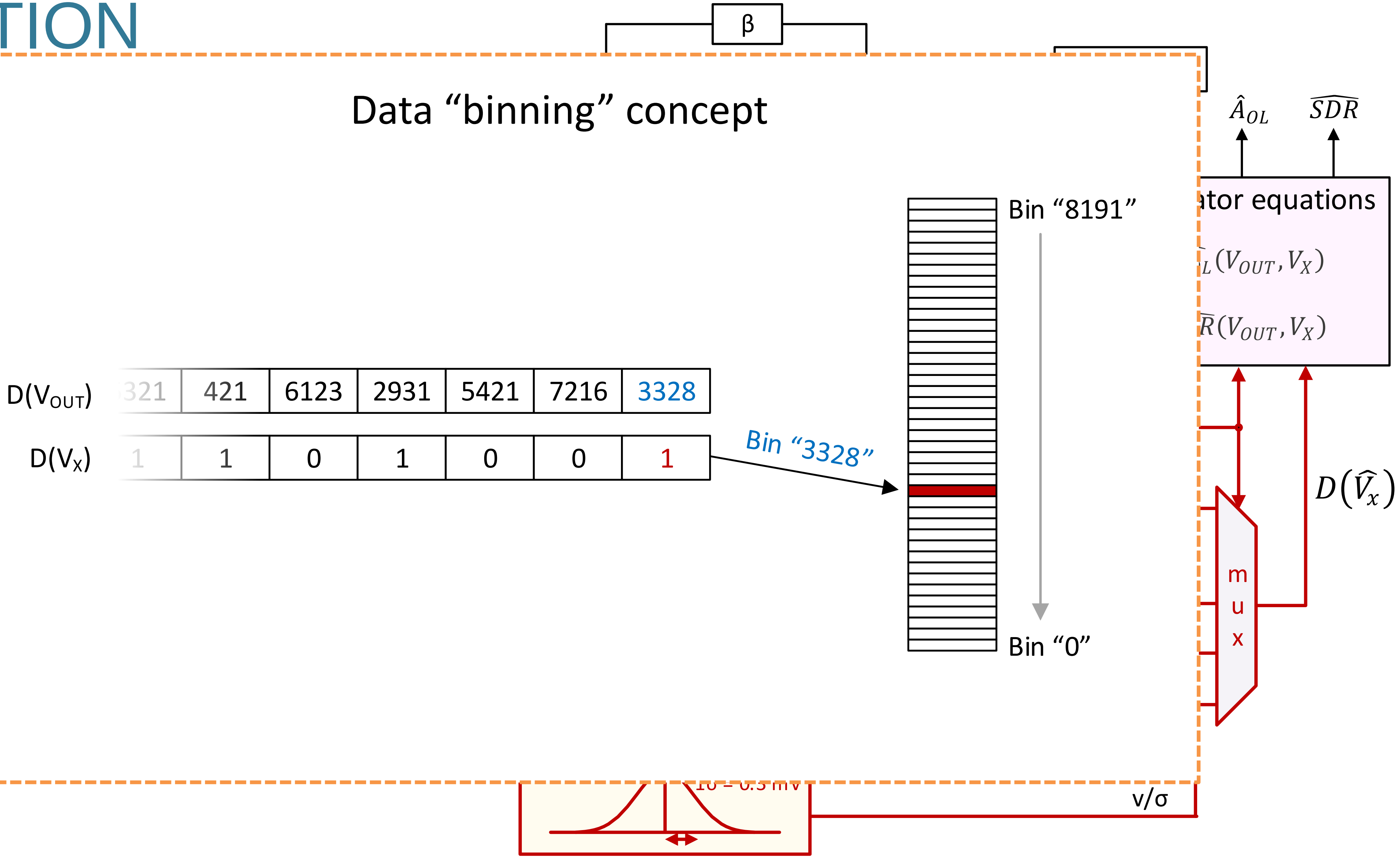


OPERATION

SDR M

- Data
sortin
into “

Data “binning” concept



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OPERATION

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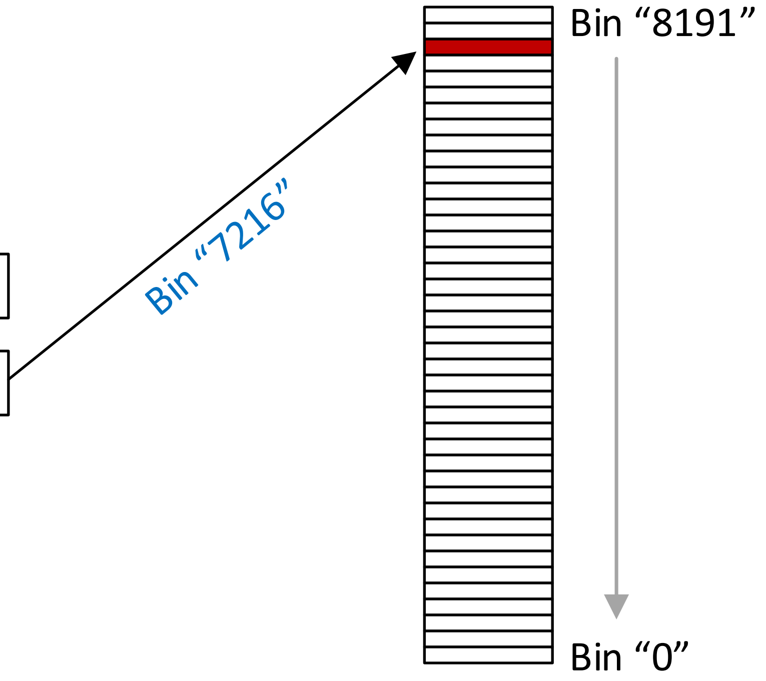
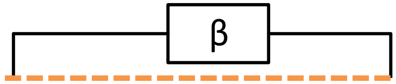
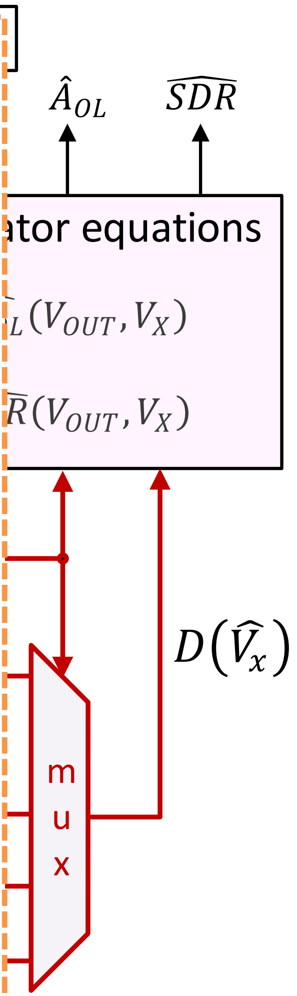
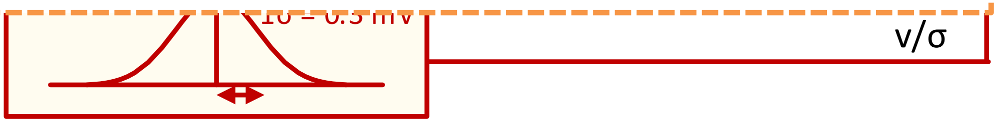




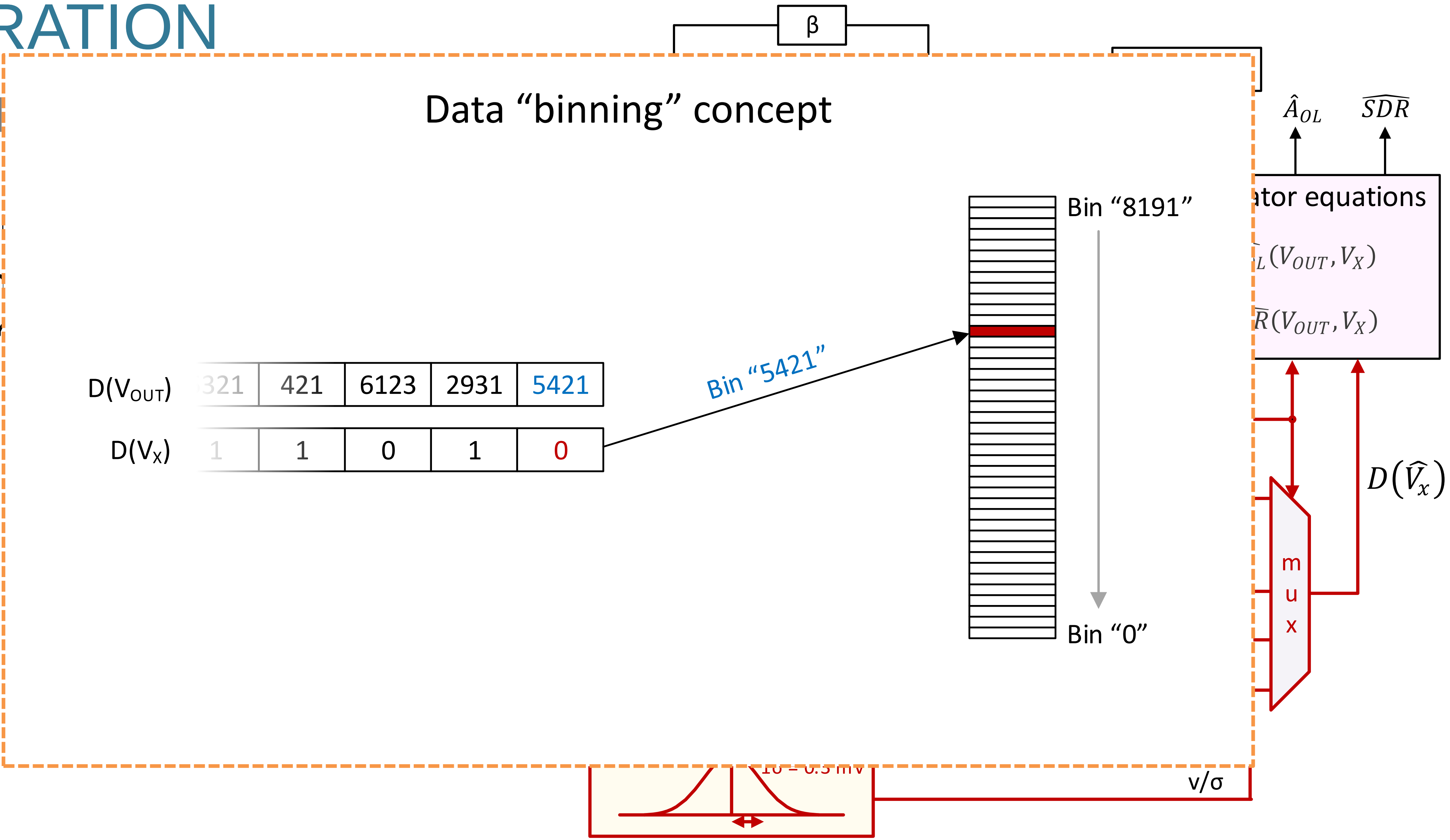




OPERATION

SDR M

- Data sortin into “



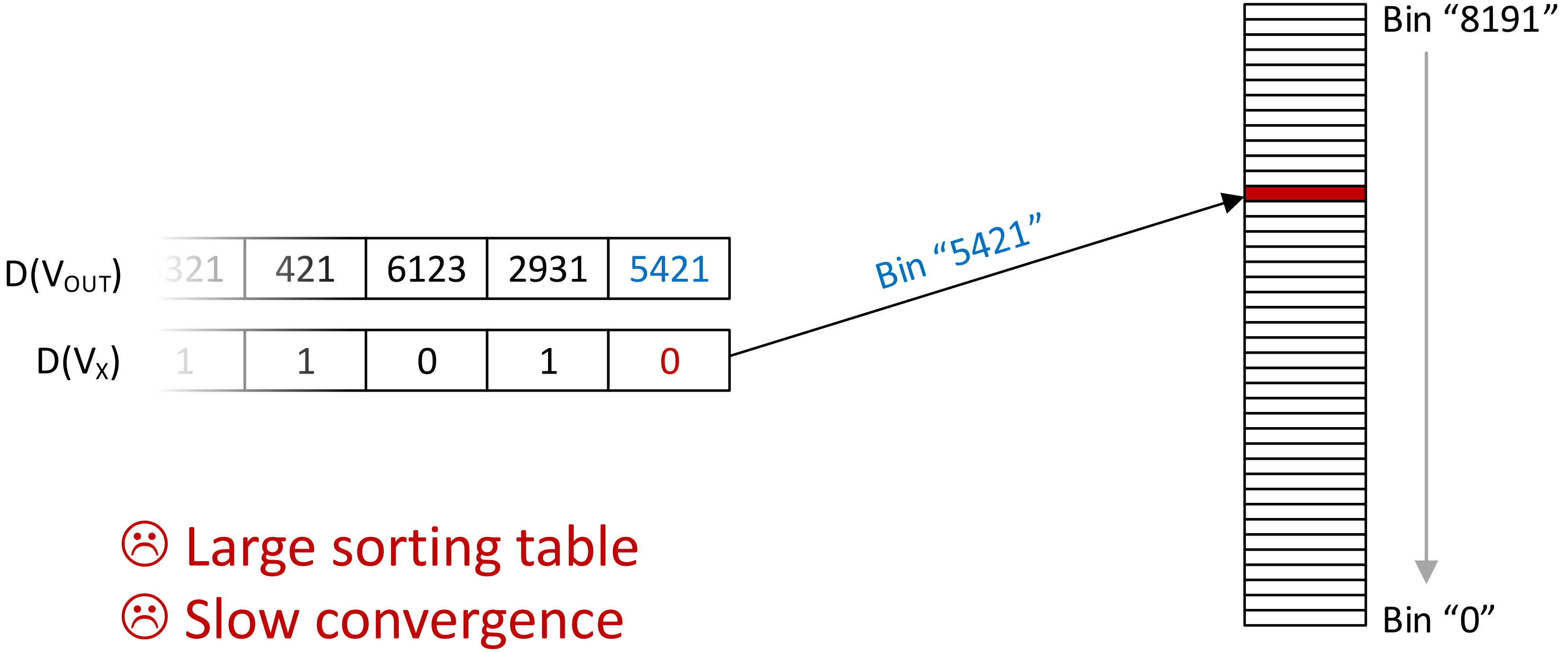
Data “binning” concept

OPERATION

SDR M

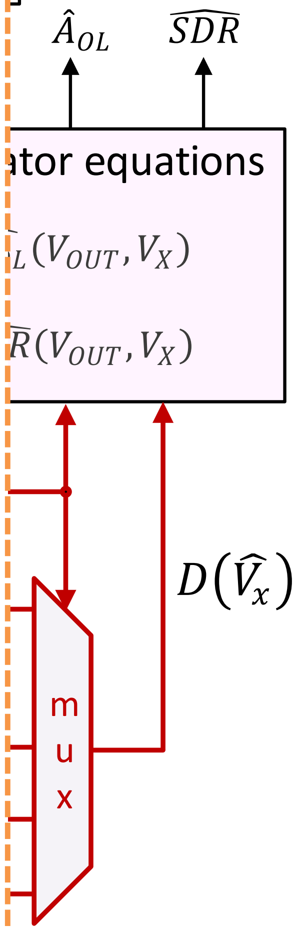
- Data sortin into “

Data “binning” concept



☹ Large sorting table

☹ Slow convergence



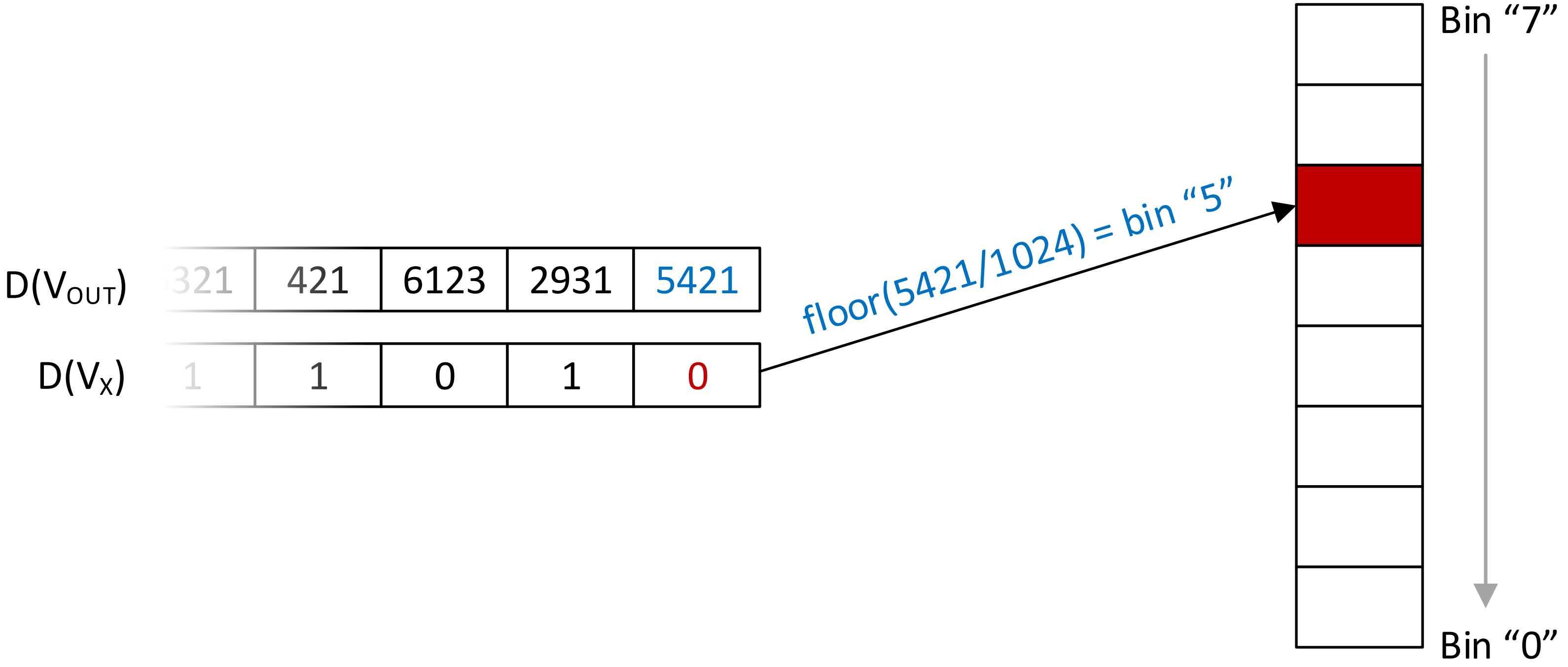
v/σ

OPERATION

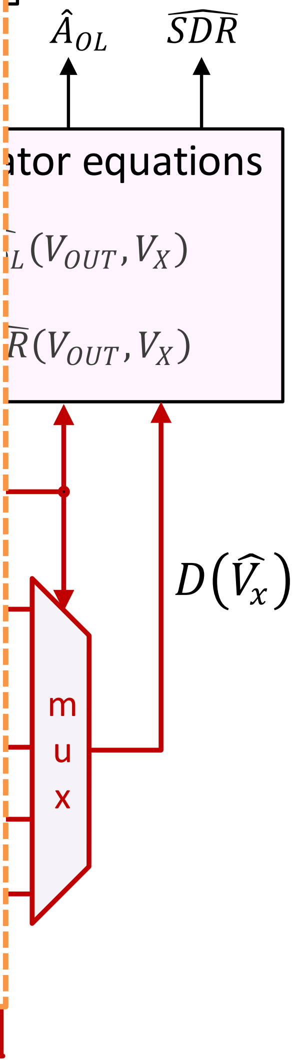
SDR M

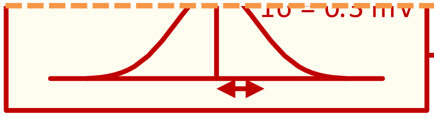
- Data
  sortin
  into “

Data “binning” concept



D(V)					
$D(V_{OUT})$	321	421	6123	2931	5421
$D(V_X)$	1	1	0	1	0





OPERATION

SDR M

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Data “binning” concept

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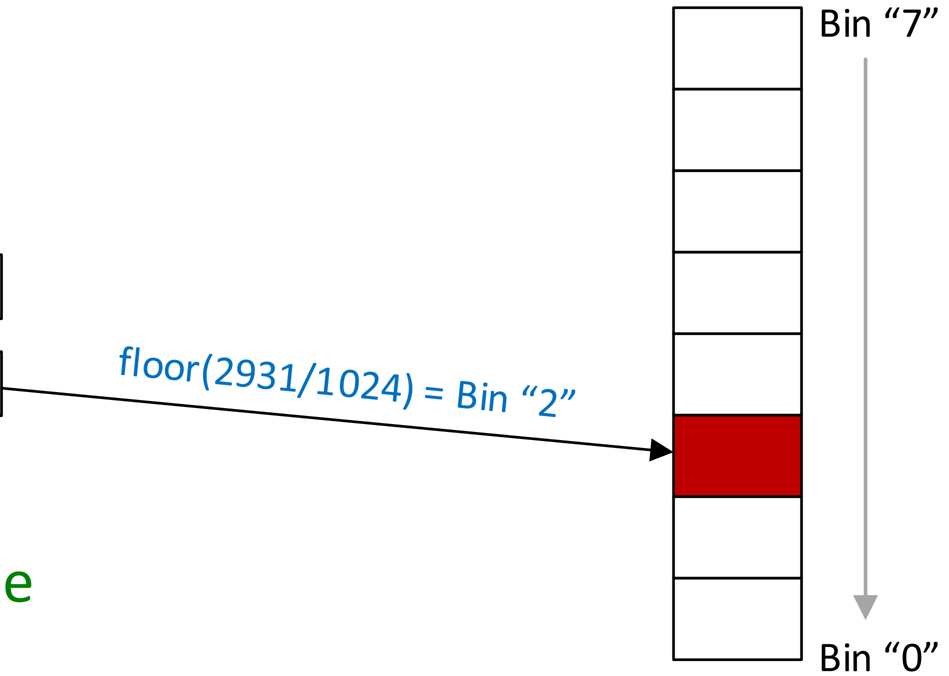
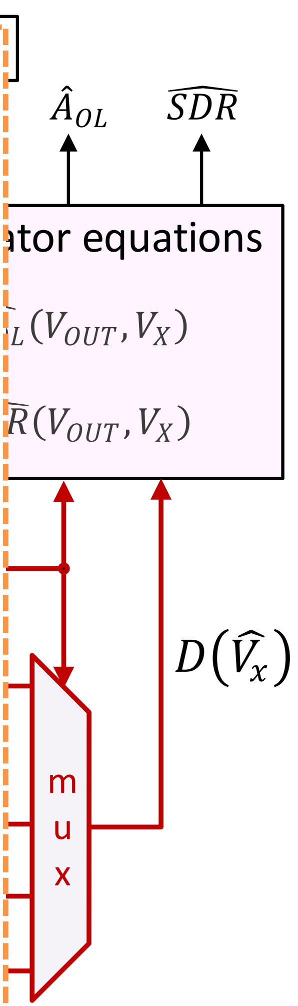
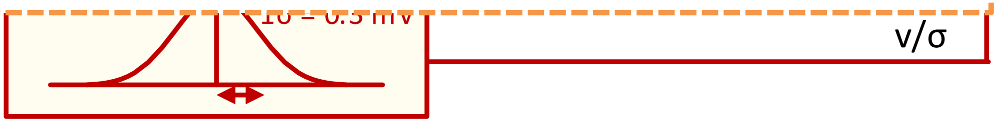


☺ Small sorting table
☺ Fast convergence
☺ Minimal impact on overall accuracy



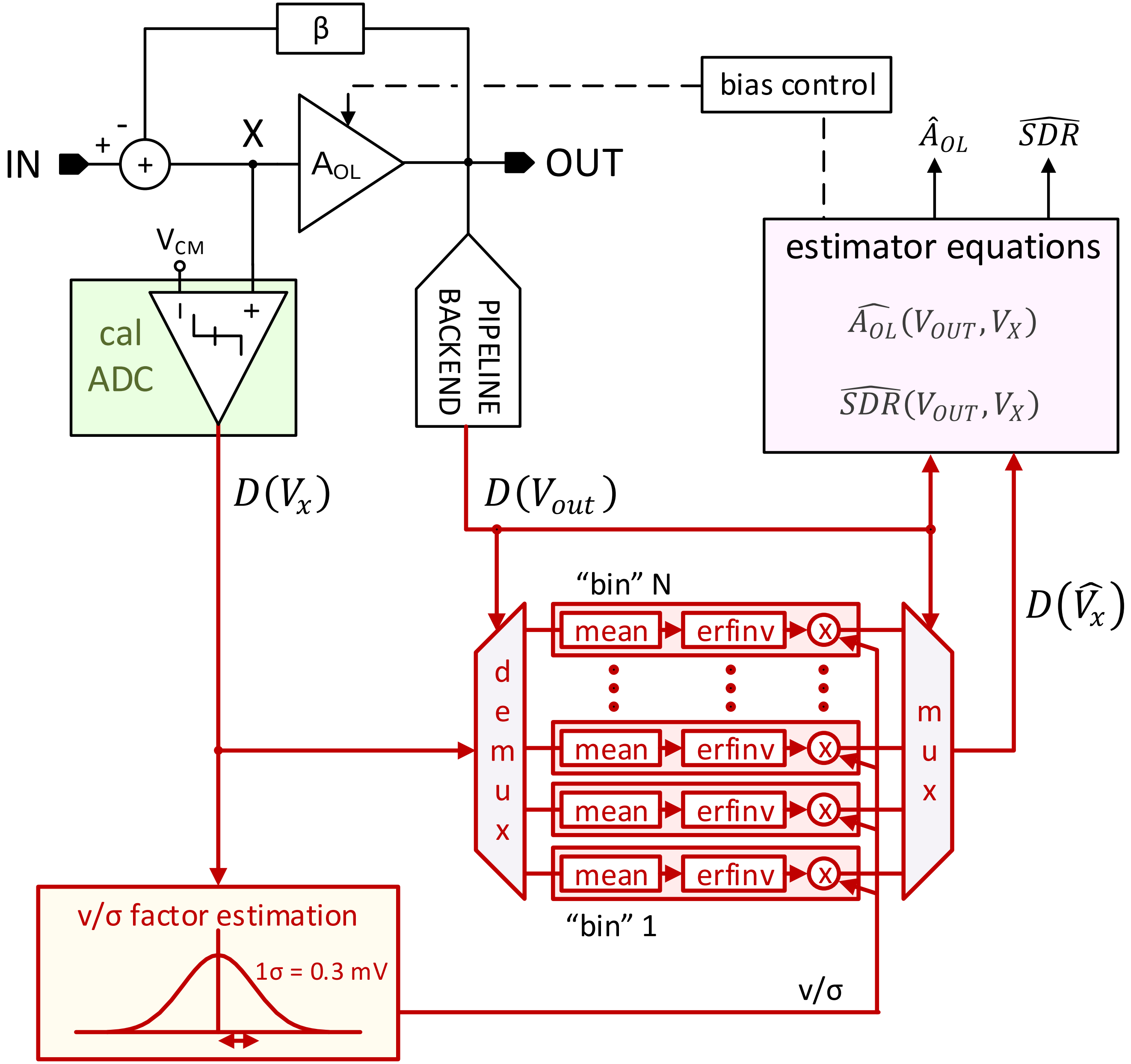


3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

OPERATION

SDR MONITORING

- Each bin performs the stochastic ADC quantization procedure described earlier

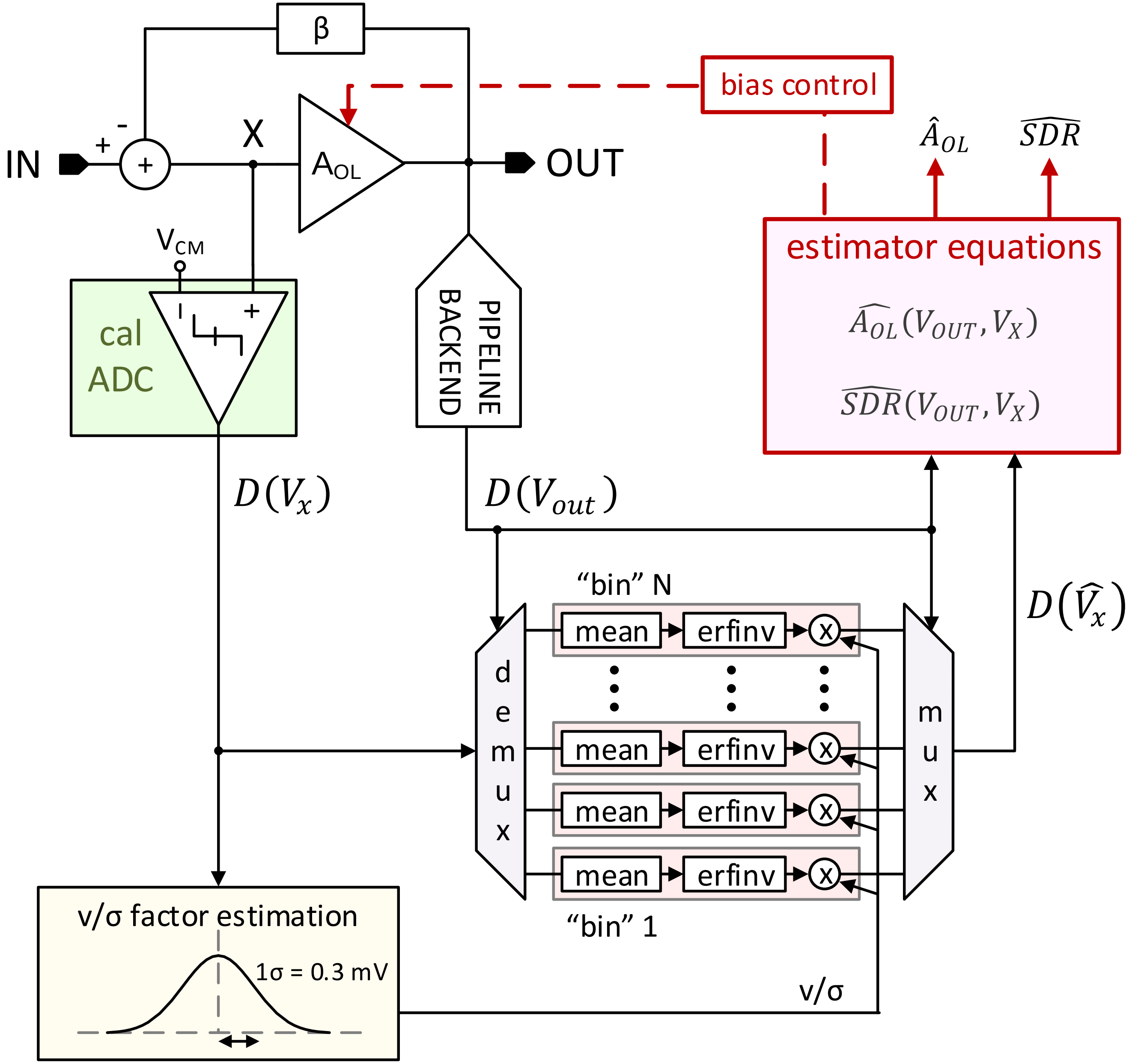


3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

OPERATION

SDR MONITORING

- Data-stream fed into estimator equations
- A biasing control block closes the control loop



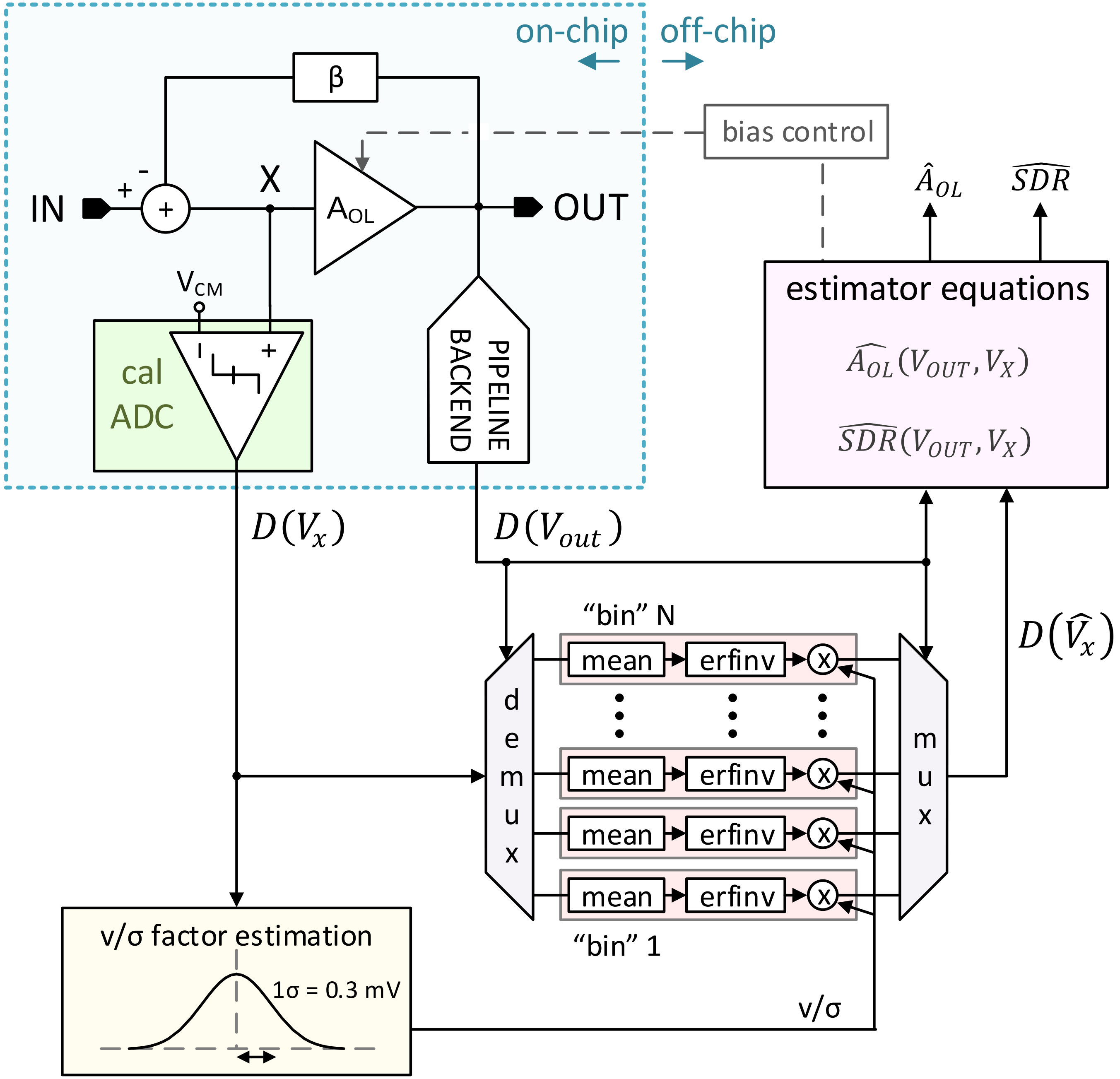
3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

OPERATION

SDR MONITORING

- Analog hardware implemented on-chip
- Digital processing implemented off-chip

- Can operate at low speeds with under-sampling
  - Total power cost negligible



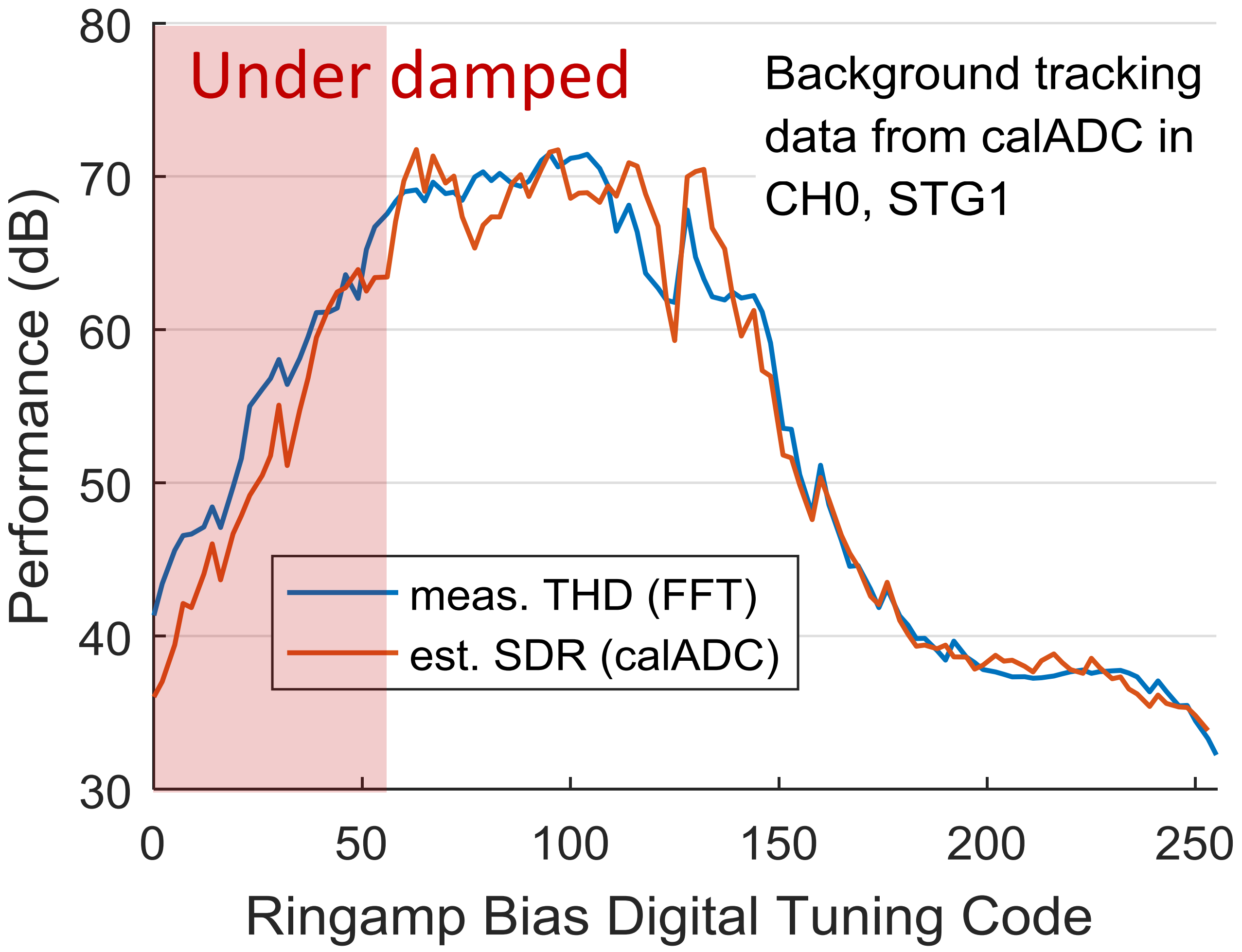
3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

DISTORTION TRACKING

MEASURED PERFORMANCE

- Baseline: Channel THD
    - Not the same as Stage SDR, but similar…

Evaluation of SDR estimation accuracy



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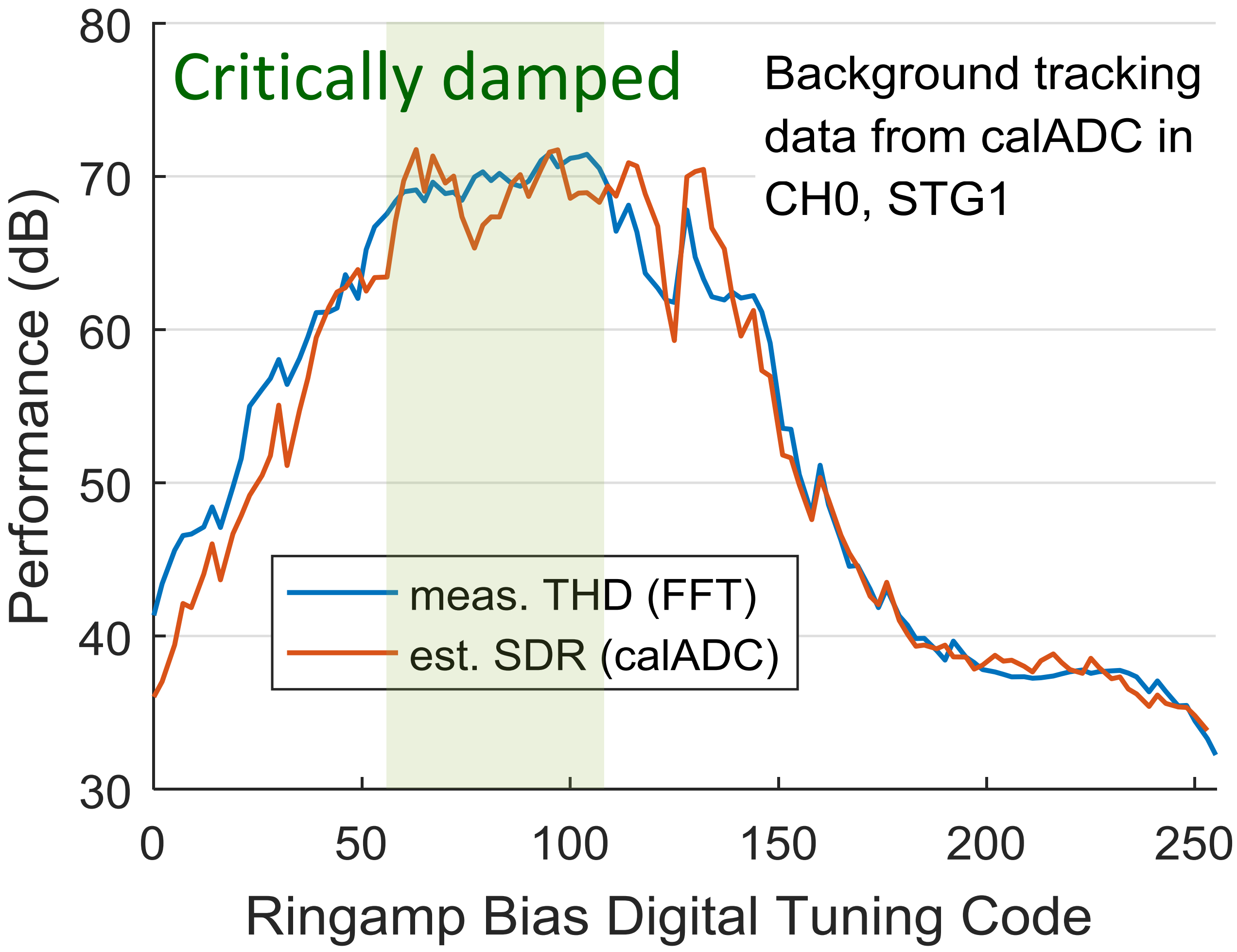

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DISTORTION TRACKING

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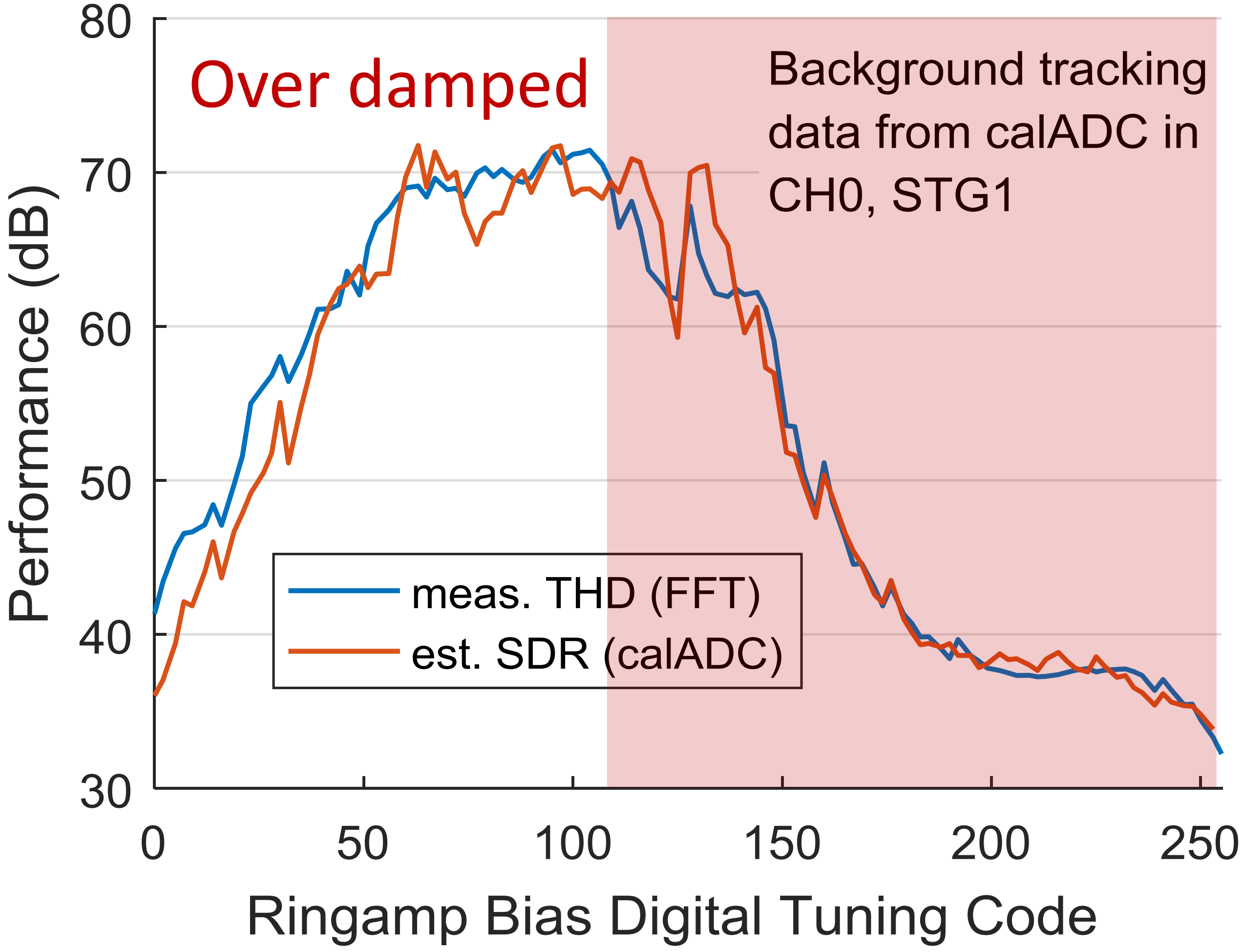


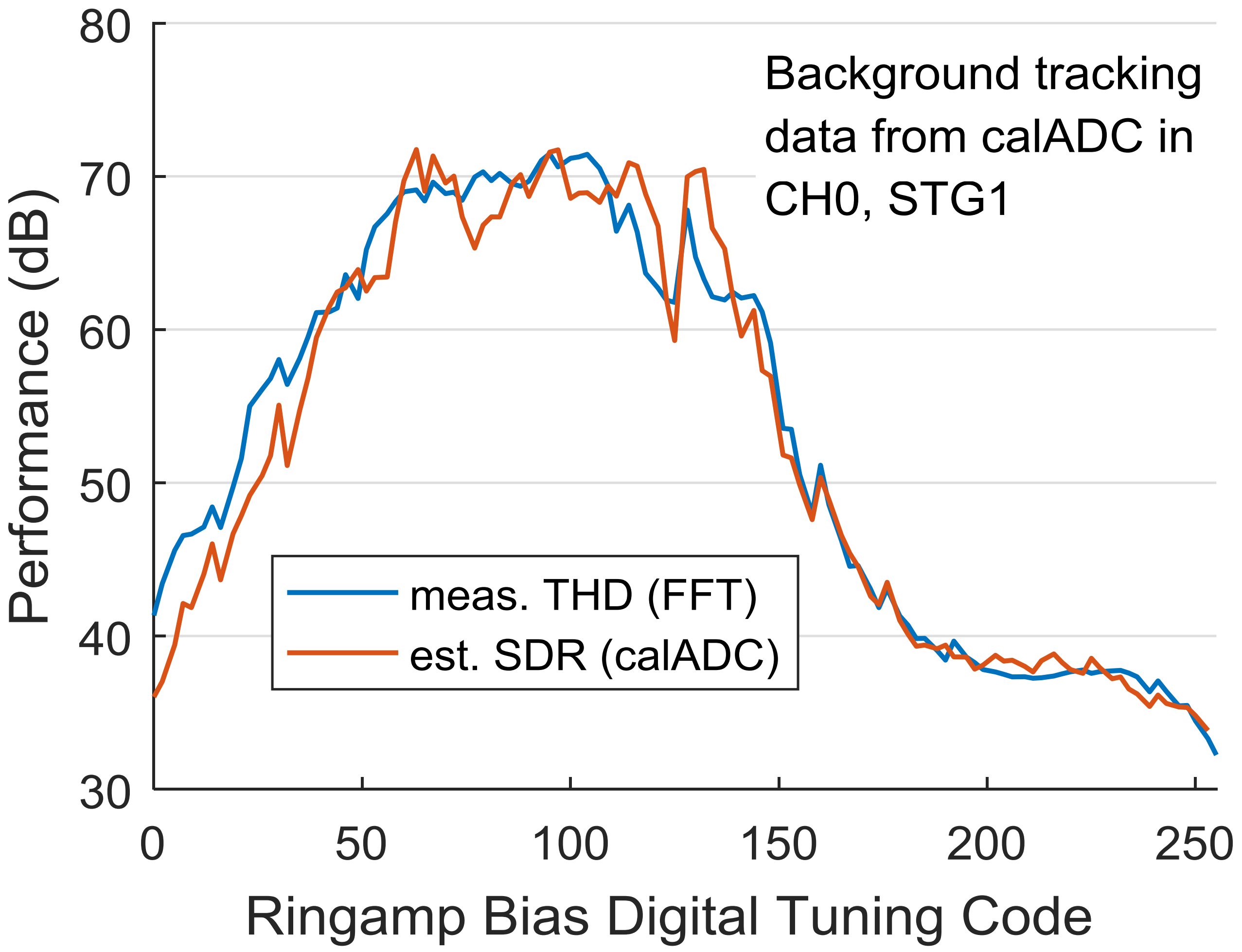
DISTORTION TRACKING

MEASURED PERFORMANCE

- Baseline: Channel THD
    - Not the same as Stage SDR, but similar...

- Successful proof-of-concept

Evaluation of SDR estimation accuracy



Background tracking data from calADC in CH0, STG1

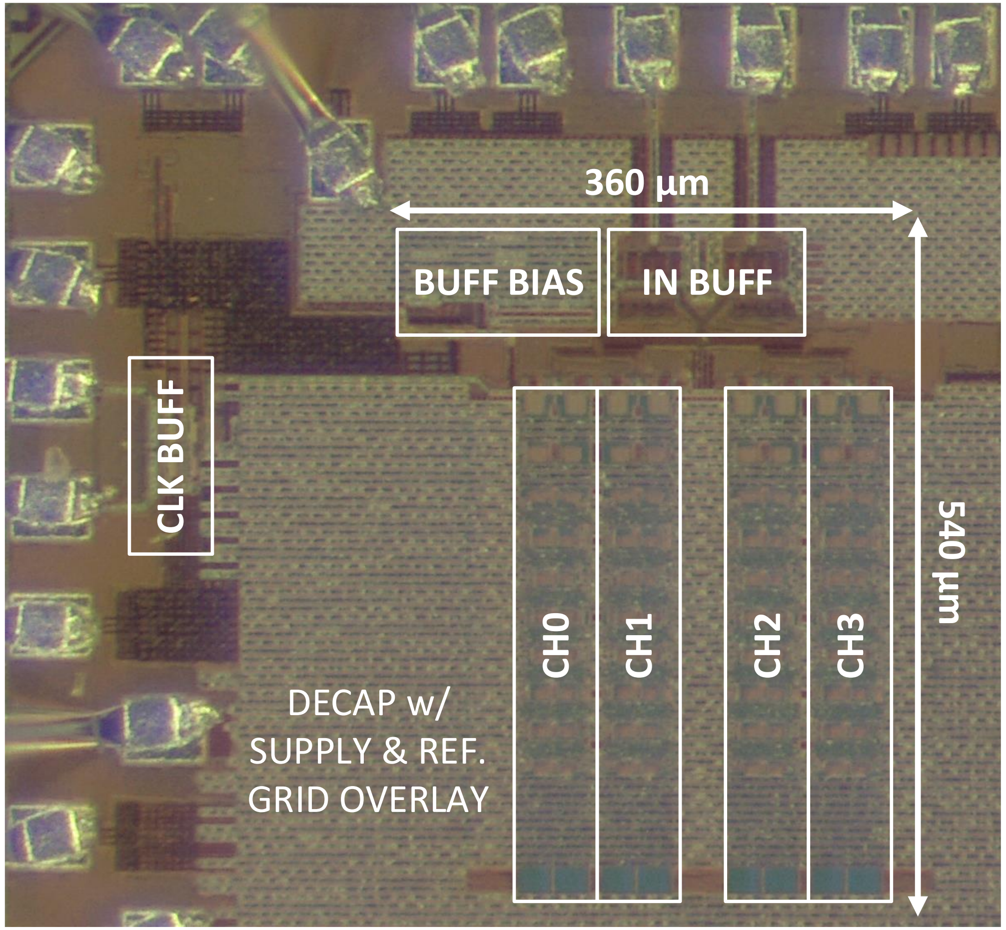
3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

IMPLEMENTATION IN 16NM CMOS

MEASURED PERFORMANCE

- 0.194mm^2 active area

- Single configuration used for all measurements reported
  - Digital controls
  - Analog levels

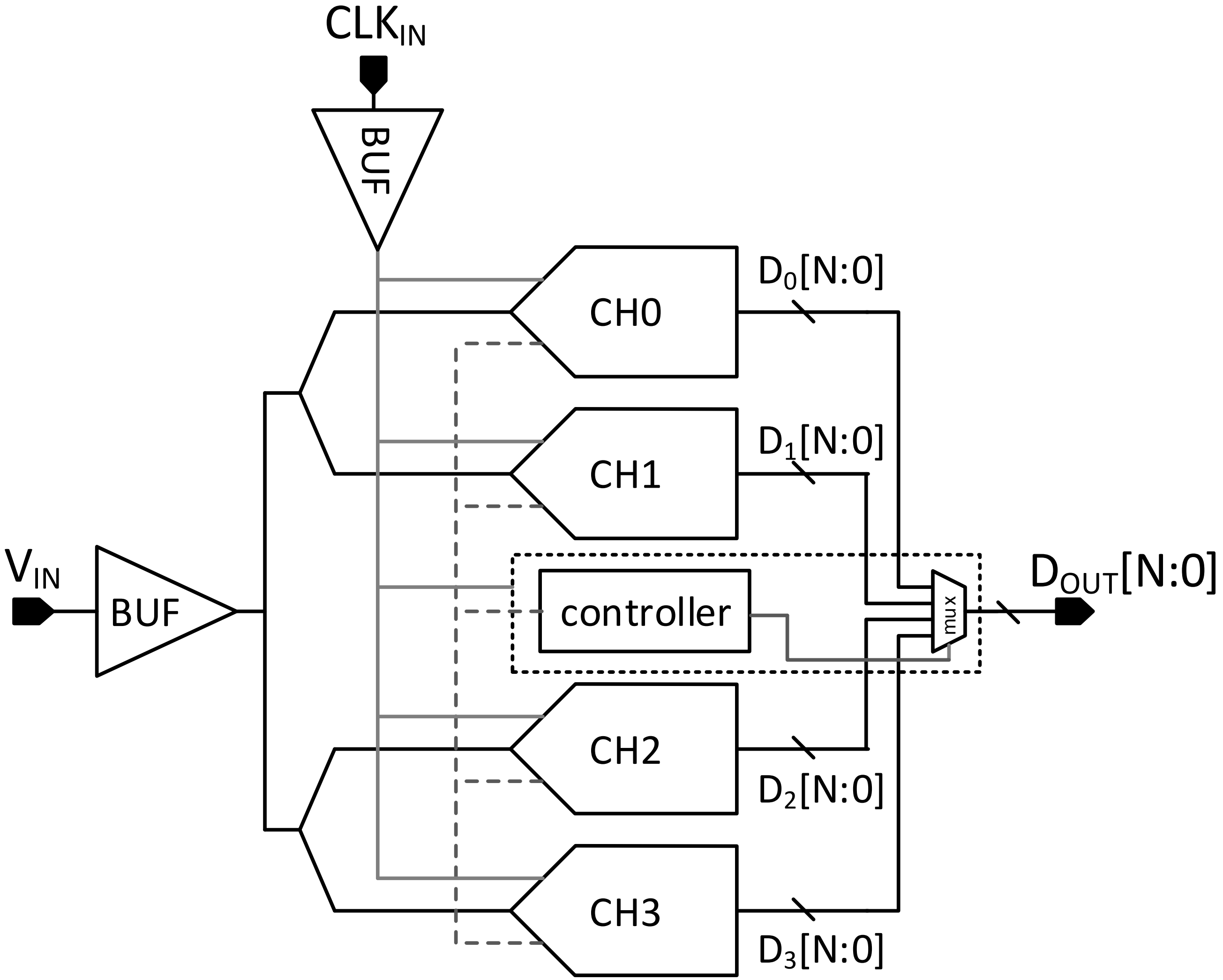


POWER BREAKDOWN

MEASURED PERFORMANCE

- V_{DD} = 850mV
- $V_{REFM/P}$ = 50mV / 800mV
  - Ringamps utilize 88% of supply

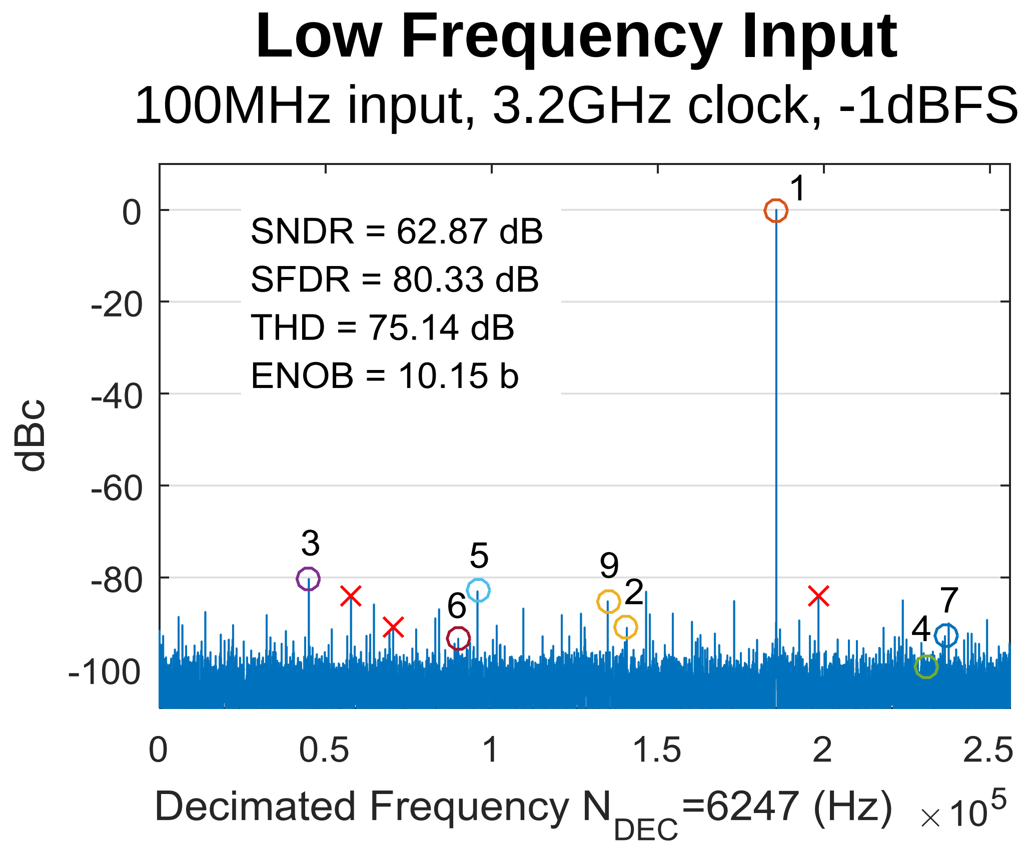
- 61.3mW total power
  - Input buffer = 11.2mW
  - Clock buffer = 2.4mW
  - Each channel = 11.9mW



3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

FFT

MEASURED PERFORMANCE



- 62.9dB SNDR
- 80.3dB SFDR

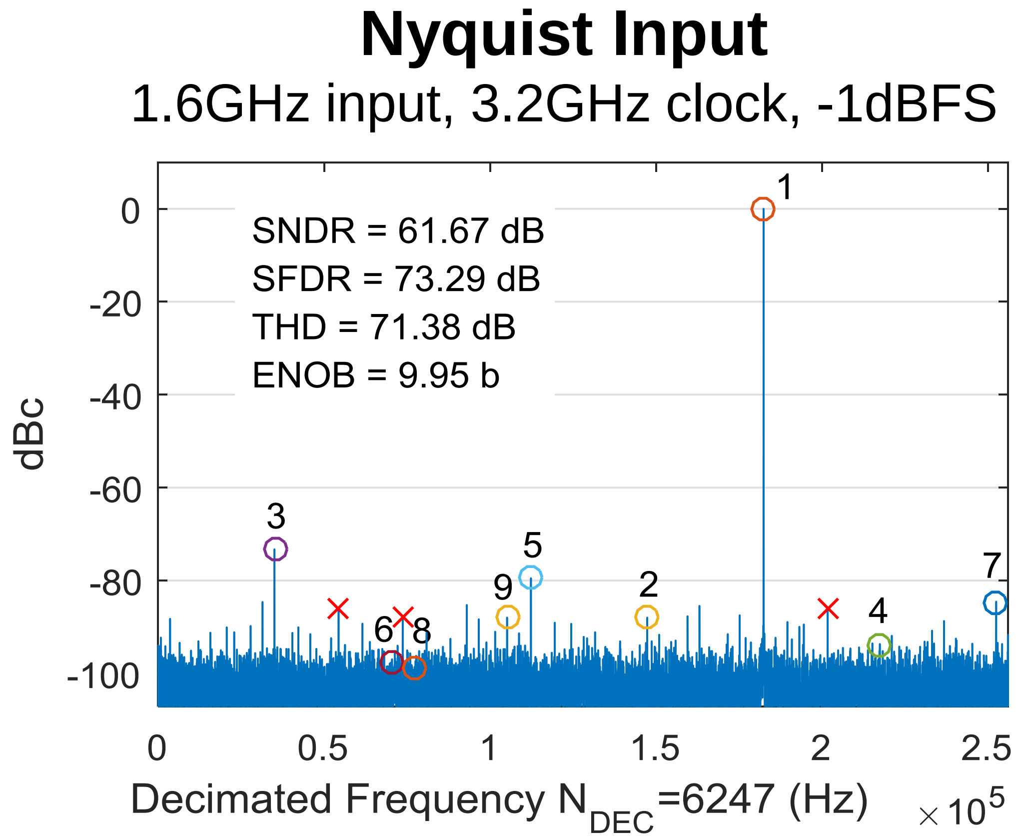
- Decimated by 6247

(Spurs labelled with X are due to interleaving mismatch)

3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

FFT

MEASURED PERFORMANCE



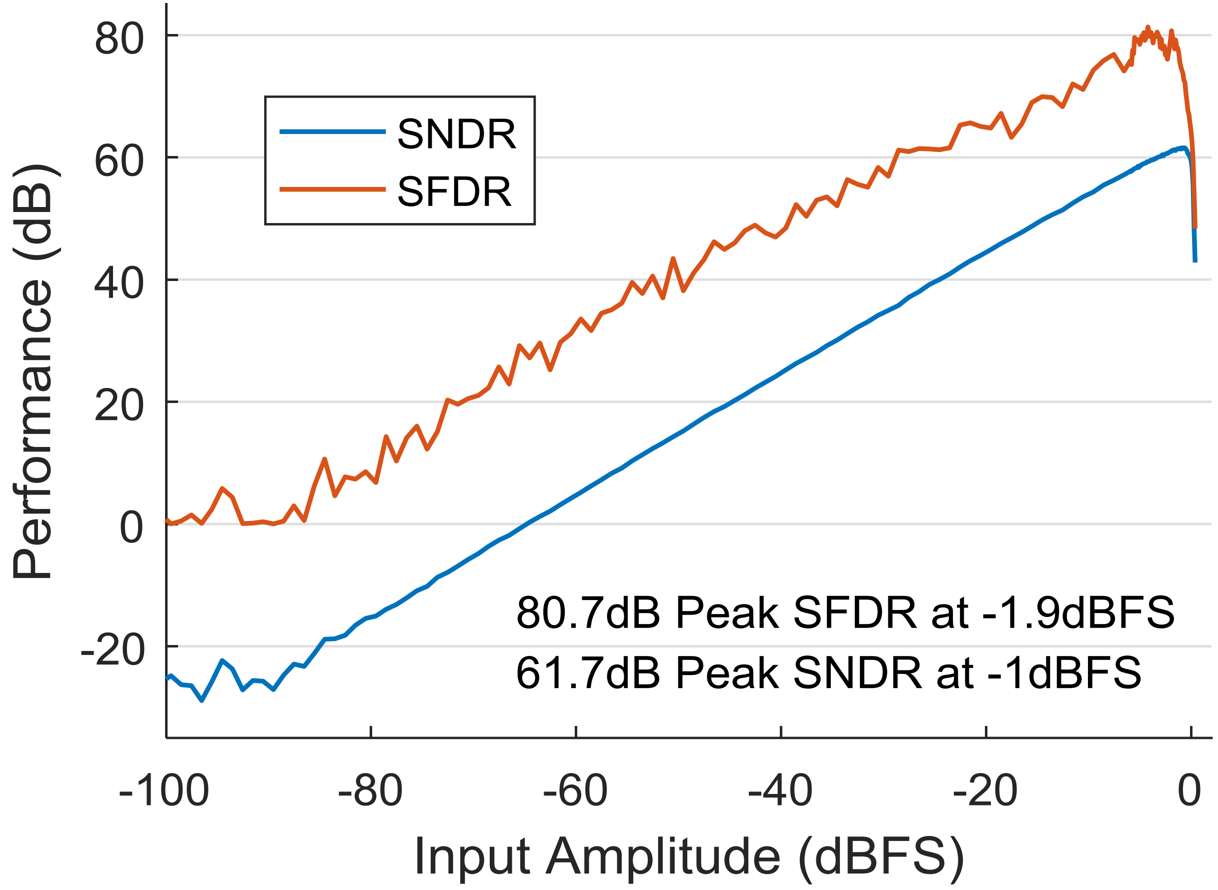
- 61.7dB SNDR
- 73.3dB SFDR

- Interleaving spurs remain <80dB
  - Tunable sampling edges with better than 5fs precision

(Spurs labelled with X are due to interleaving mismatch)

SWEEP: INPUT AMPLITUDE

MEASURED PERFORMANCE

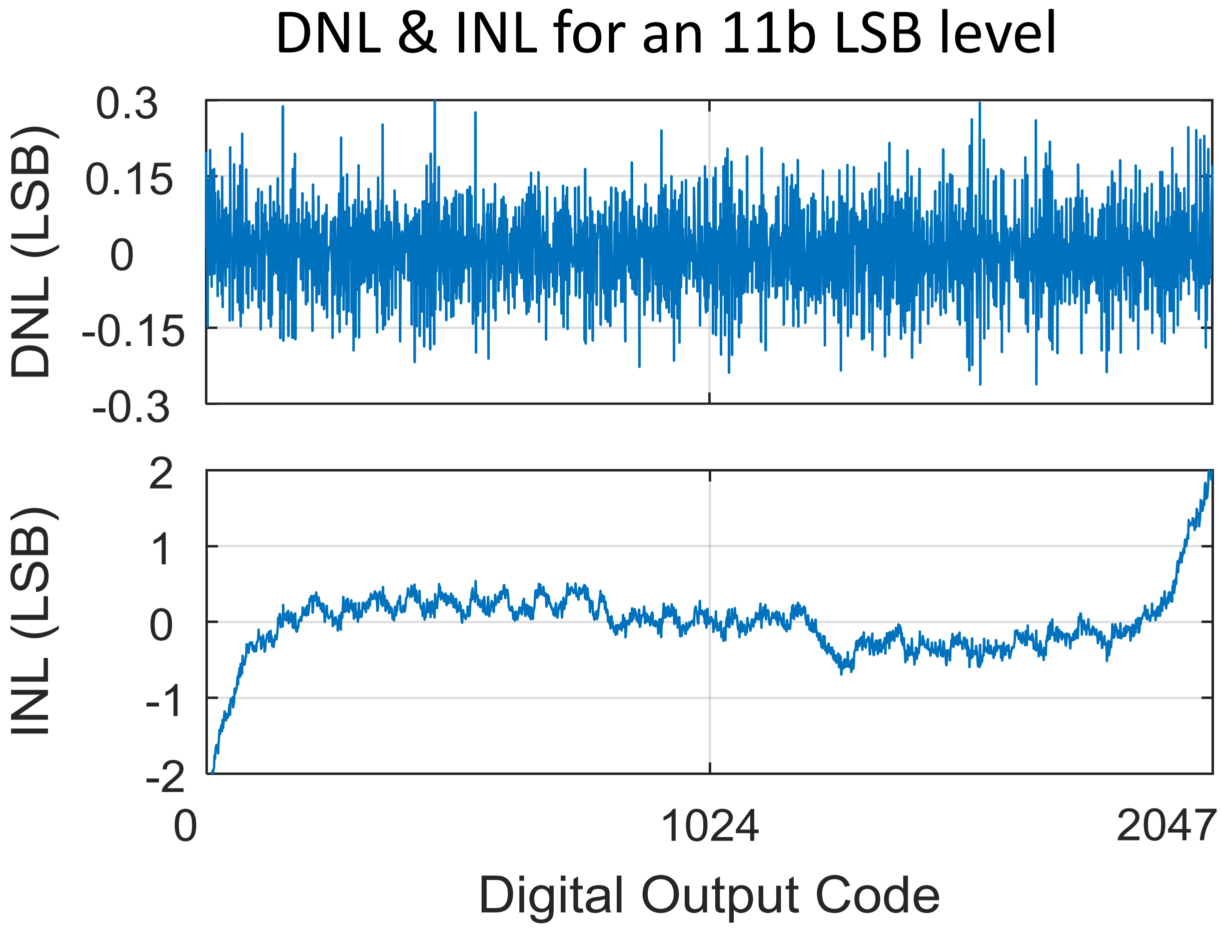


- 80.7dB Peak SFDR at -1.9dBFS
- 61.7dB Peak SNDR at -1dBFS

- Compression above -1dBFS due to HD3 from input buffer

DNL / INL

MEASURED PERFORMANCE

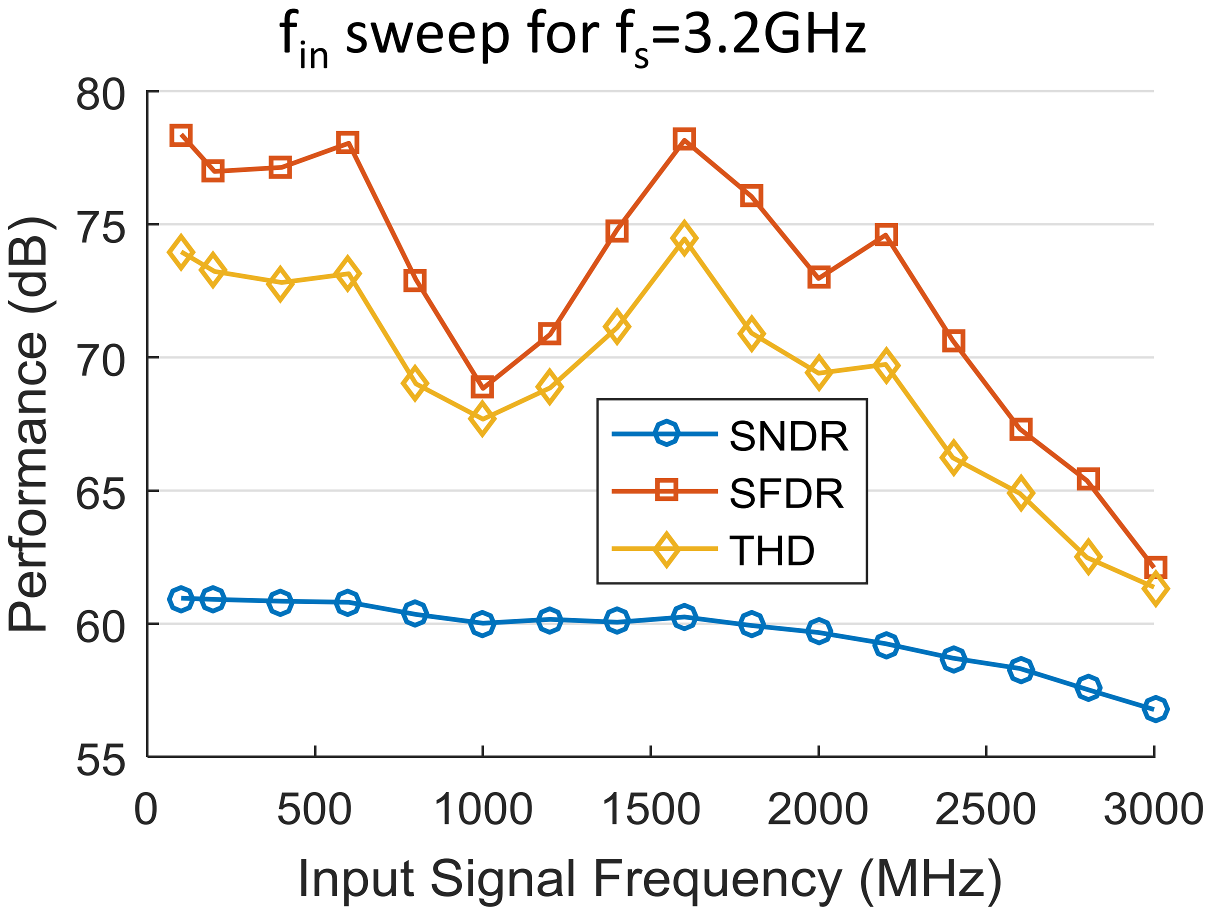


- Compression at edge codes also due to HD3 of input buffer

3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

SWEEP: INPUT FREQUENCY

MEASURED PERFORMANCE



- Drop in HD3 around f_{in}=1GHz related to bond-wires / PCB

3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

COMPARISON WITH SOTA

MEASURED PERFORMANCE

- SoTA for direct-RF sampling ADCs

	This work	Vaz ISSCC 2017	Devarajan ISSCC 2017	Straayer ISSCC 2016	Wu ISSCC 2016	Ali VLSI 2016
Architecture	**Pipeline**	Pipe-SAR	Pipeline	Pipeline	Pipeline	Pipeline
Sampling rate [Gsps]	**3.2**	4	10	4	4	5
Technology [nm]	**16**	16	28	65	16	28
ENOB Nyquist [bit]	**10.0**	9.2	8.8	8.9	9.0	9.3
SFDR Nyquist [dB]	**73.3**	67.0	64	64.0	68.0	70
Power [mW]	**61**	513	2900	2214	300	2300
$\text{FoM}_{\text{Walden}}$ [fJ/c.step]	**19**	214	631	1130	145	709
$\text{FoM}_{\text{Schreier}}$ [dB]	**166**	153	147	145	154	148
Area [mm²]	**0.194**	1.04	20.2	11.0	0.34	14.4

COMPARISON WITH SOTA

MEASURED PERFORMANCE

- SoTA for direct-RF sampling ADCs
  - Highest ENOB

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COMPARISON WITH SOTA

MEASURED PERFORMANCE

- SoTA for direct-RF sampling ADCs
  - Highest ENOB
  - Highest Linearity

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COMPARISON WITH SOTA

MEASURED PERFORMANCE

- SoTA for direct-RF sampling ADCs
  - Highest ENOB
  - Highest Linearity
  - Lowest Power

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COMPARISON WITH SOTA

MEASURED PERFORMANCE

- SoTA for direct-RF sampling ADCs
  - Highest ENOB
  - Highest Linearity
  - Lowest Power
  - Best FoM

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Area [mm²]	**0.194**	1.04	20.2	11.0	0.34	14.4

COMPARISON WITH SOTA

MEASURED PERFORMANCE

- SoTA for direct-RF sampling ADCs
  - Highest ENOB
  - Highest Linearity
  - Lowest Power
  - Best FoM

- Major advance in SoTA

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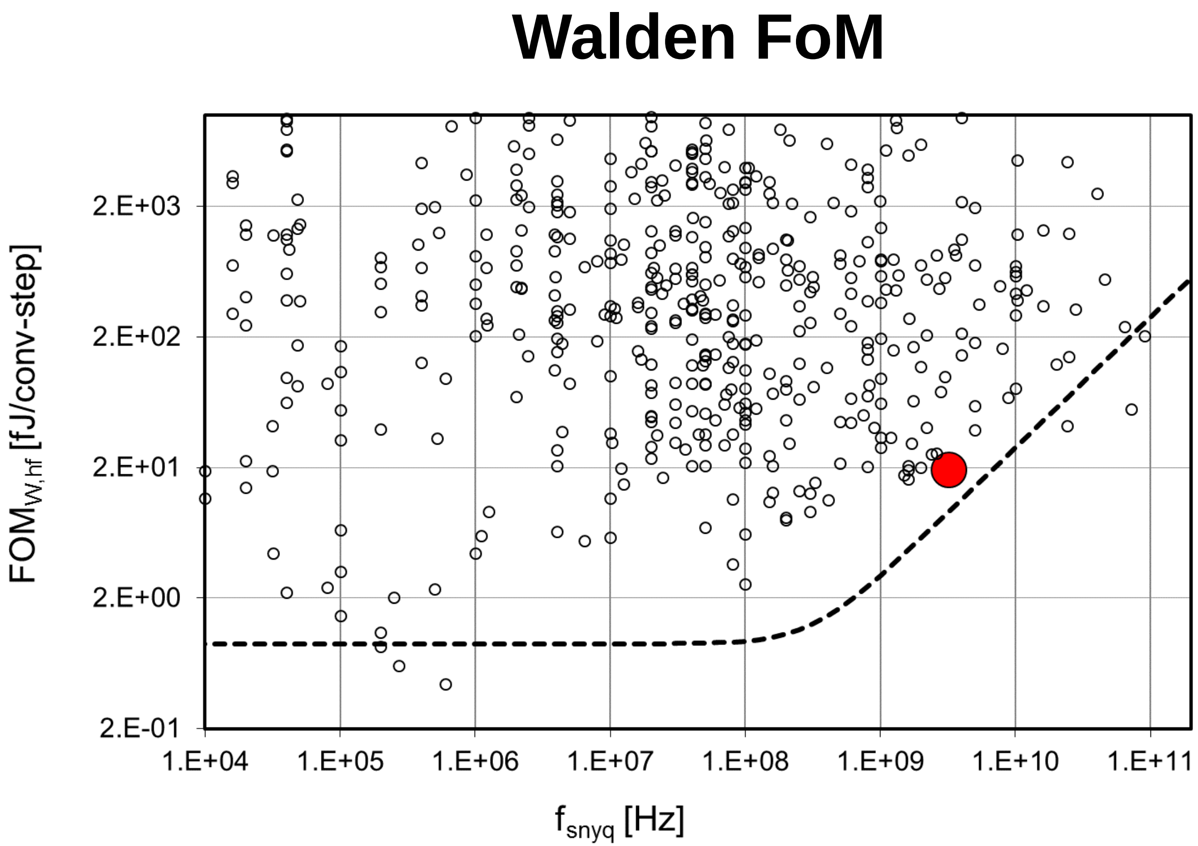
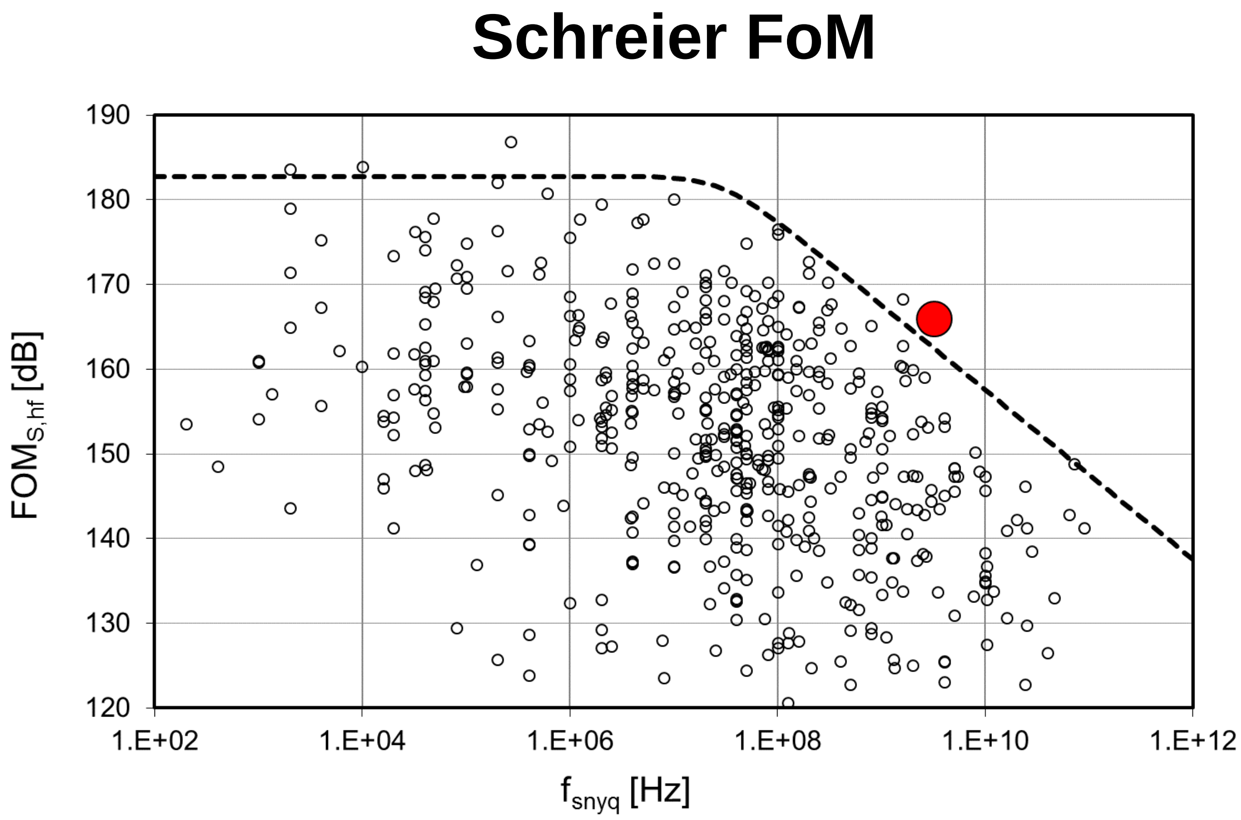
Power [mW]	**61**	513	2900	2214	300	2300
$\text{FoM}_{\text{Walden}}$ [fJ/c.step]	**19**	214	631	1130	145	709
$\text{FoM}_{\text{Schreier}}$ [dB]	**166**	153	147	145	154	148
Area [mm²]	**0.194**	1.04	20.2	11.0	0.34	14.4

COMPARISON WITH SOTA

MEASURED PERFORMANCE





B. Murmann, "ADC Performance Survey 1997-2018," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

THE BIG PICTURE

HOW DID WE DO IT?

- Solved a block-level problem to “change the rules”

THE BIG PICTURE

HOW DID WE DO IT?

- Solved a block-level problem to “change the rules”

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- Re-evaluated the system design based on these new rules
    - Amplifier-intensive architecture “ok”
    - E.g. 1.5b/stage pipeline

THE BIG PICTURE

HOW DID WE DO IT?

- Solved a block-level problem to “change the rules”

- Re-evaluated the system design based on these new rules

- Broader message for *all* circuit designers
  - Can ringamps change the rules in *your* application too?
  - Pipeline, SAR, Pipelined-SAR, Delta-Sigma, Active Filters, VGAs, etc..

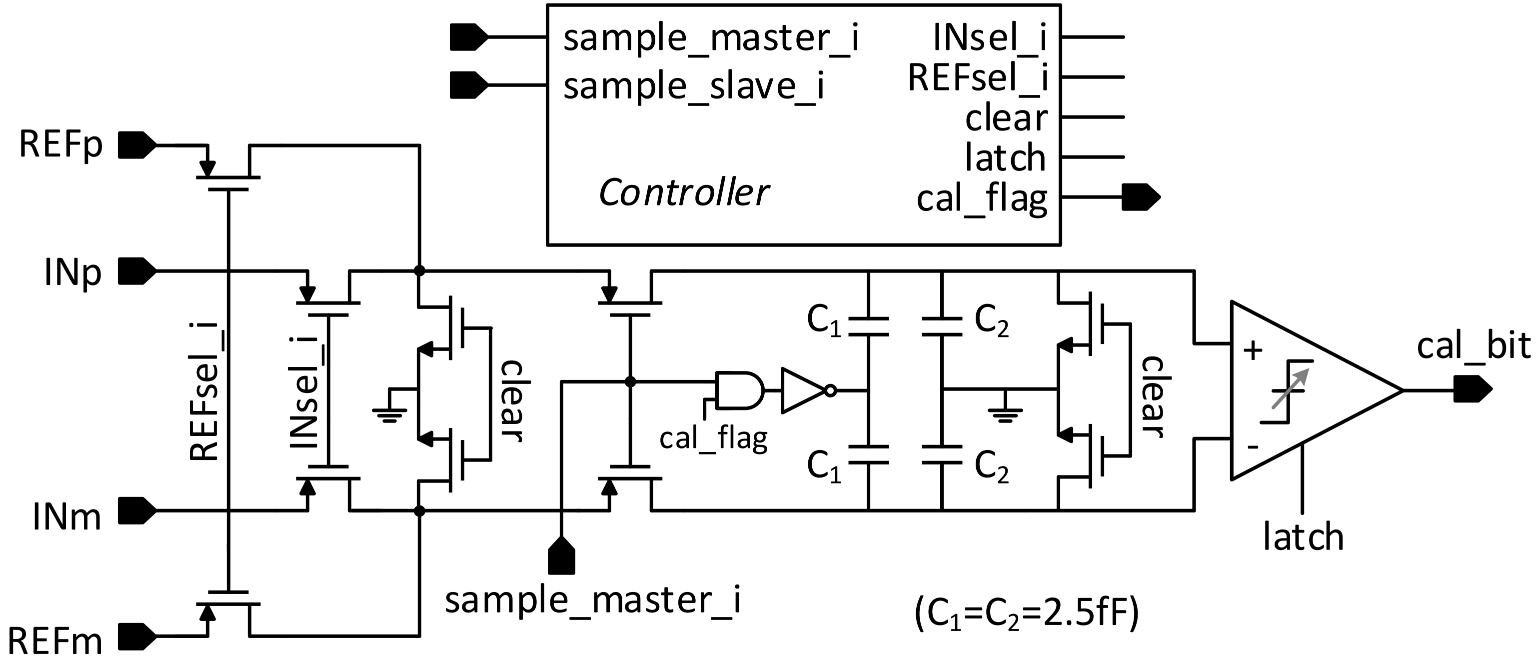
THANK YOU FOR YOUR ATTENTION!

ADDITIONAL MATERIALS...

DISTORTION TRACKING

“CAL ADC” CIRCUIT

- On-chip stochastic ADC circuit (calADC)
  - Compact layout
- 4 modes of operation
  - Disable
  - Self-calibration
  - Regular operation
  - Dummy operation



3.1: A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion