A 6-to-600MS/s Fully Dynamic Ringamp Pipelined ADC with Asynchronous Event-Driven Clocking in 16nm

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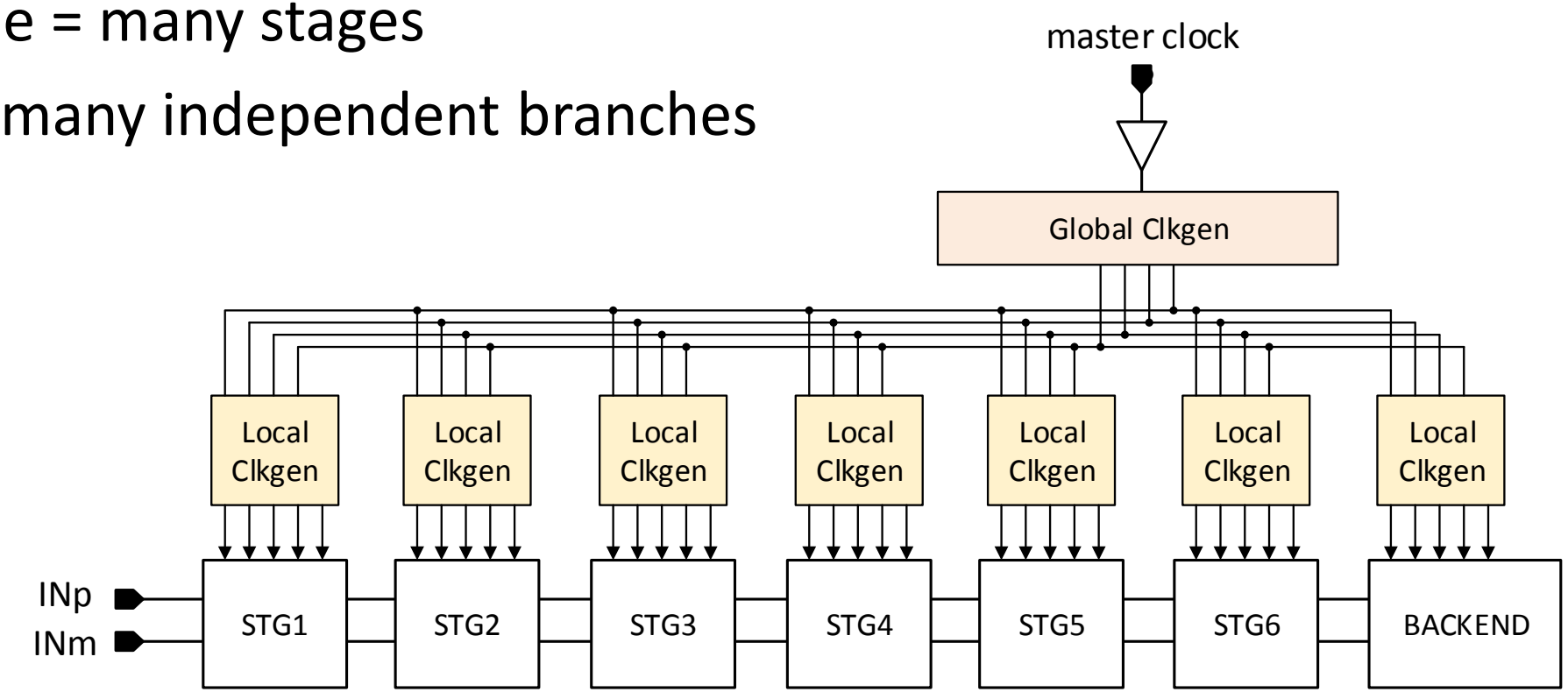
imec, Leuven, Belgium

HIGH SPEED PIPELINED ADC CLOCKING

MOTIVATION

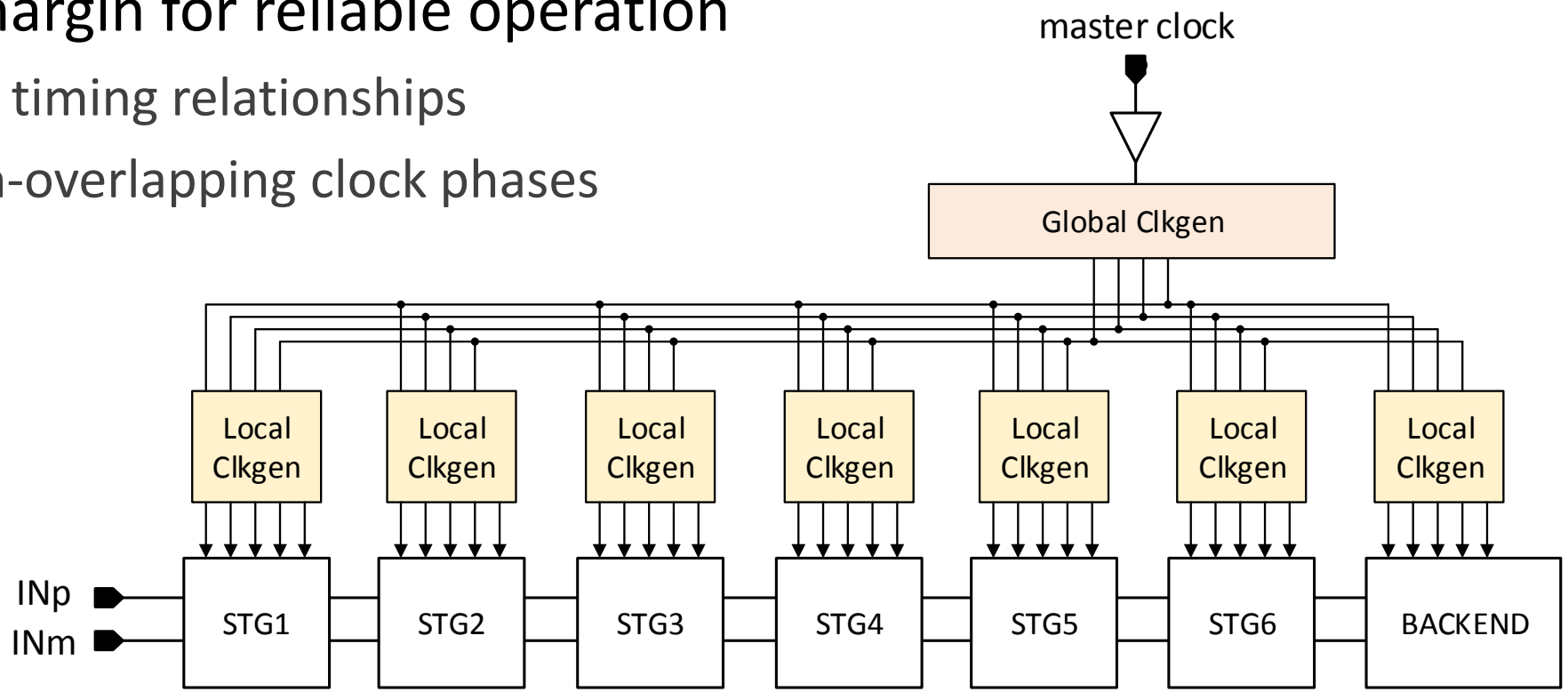
- "Deep" pipeline = many stages
- Clock tree has many independent branches
  - Mismatch
  - Parasitics
  - Skew



HIGH SPEED PIPELINED ADC CLOCKING

MOTIVATION

- Needs timing margin for reliable operation
  - Respect causal timing relationships
  - Guarantee non-overlapping clock phases



HIGH SPEED PIPELINED ADC CLOCKING

MOTIVATION

- Becomes exponentially more difficult at high speeds
  - Absolute timing overheads don’t scale with relative clock speeds
- Difficult design tradeoffs
  - Power
  - Speed
  - Jitter
  - Reliability

HIGH SPEED PIPELINED ADC CLOCKING

MOTIVATION

- Residue amplification typically dominates power
  - Ring amplifiers have begun to change this
  - Now clock power can even dominate...

HIGH SPEED PIPELINED ADC CLOCKING

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J. Lagos, et al.
"A Single-Channel, 600-MS/s, 12-b, Ringamp-Based Pipelined ADC in 28-nm CMOS"
JSSC, Feb. 2019

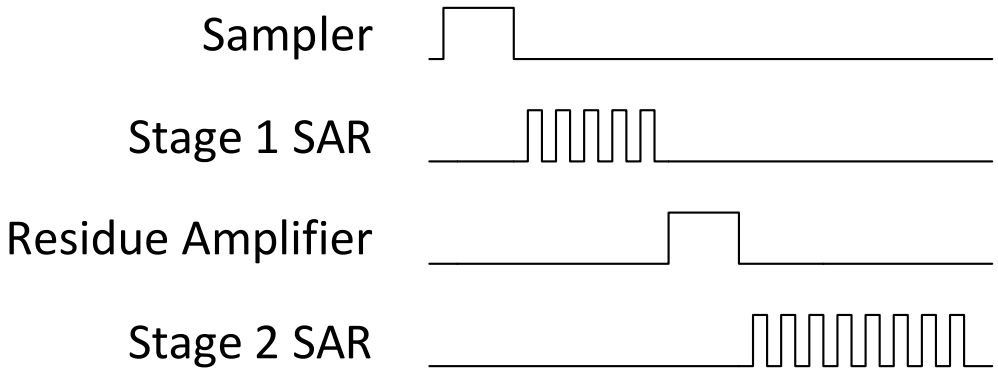
J. Lagos, et al.
"A 1Gsps, 12-bit, Single-Channel Pipelined ADC with Dead-Zone-Degenerated Ring Amplifiers"
JSSC, Mar. 2019

ASYNCHRONOUS TIMING CONTROL

MOTIVATION

- Asynchronous, event-driven timing control
  - Widely used in SAR and pipelined SAR
  - Still unexplored in “deep” pipeline ADCs

Typical Pipelined-SAR clocking scheme



IN THIS TALK

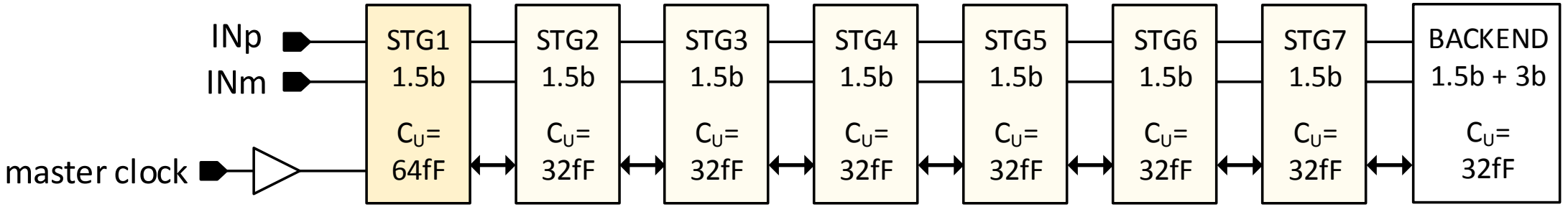
PREVIEW

- Asynchronous, event-driven timing for “deep” pipelined ADCs

- 60dB SNDR, 78dB SFDR single-channel ringamp-based pipelined ADC
  - Fully dynamic power consumption
  - FOM_W < 13fJ/conv-step from 6MS/s to 600 MS/s

TOP LEVEL

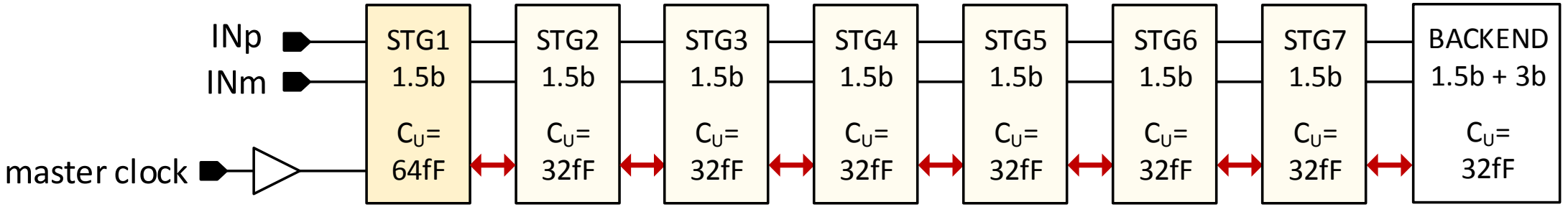
SYSTEM OVERVIEW



- 7 x 1.5b/stage
- 1.5b + 3b backend flash stage

TOP LEVEL

SYSTEM OVERVIEW

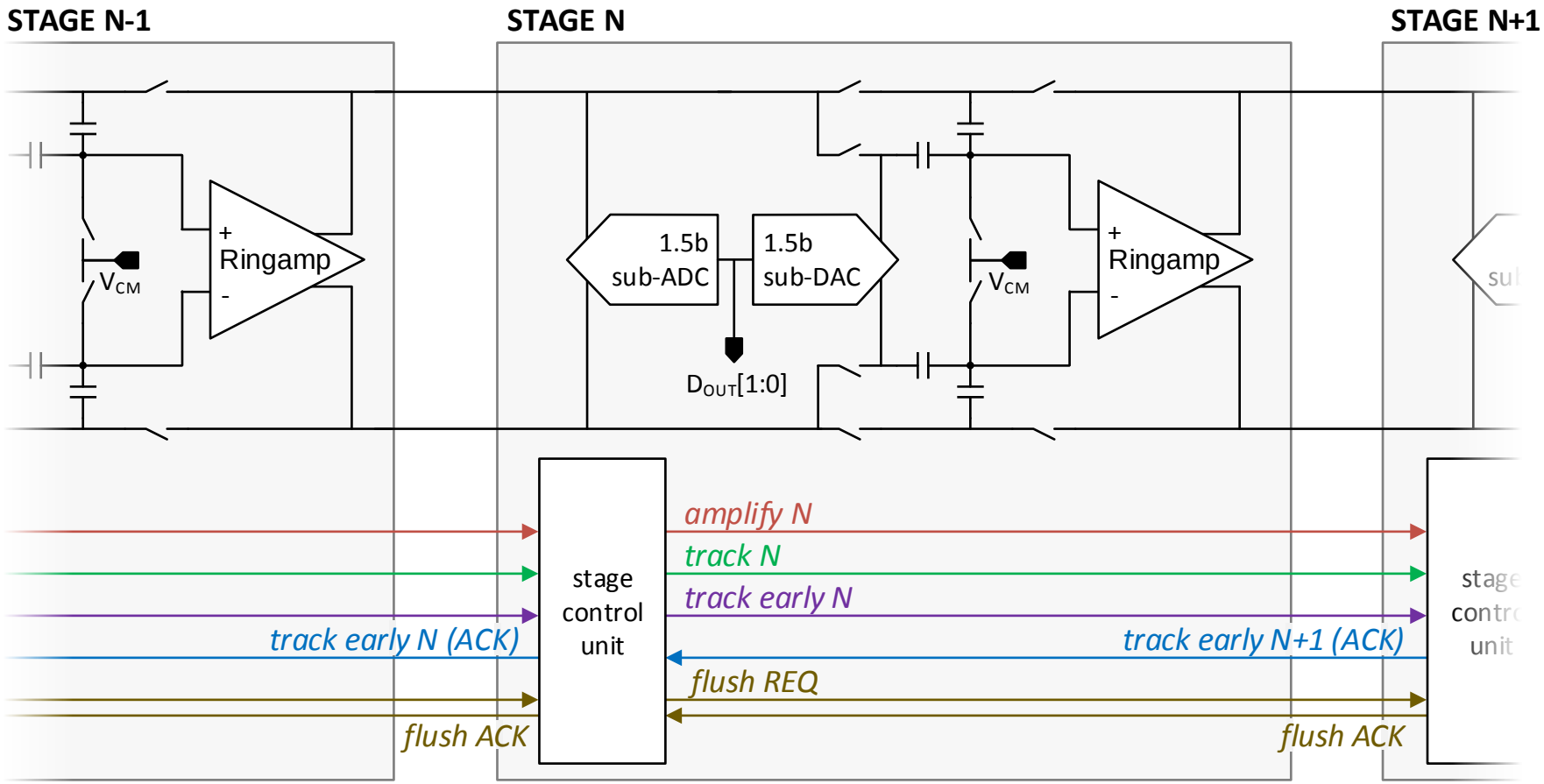


- 7 x 1.5b/stage
- 1.5b + 3b backend flash stage
- Event triggering orchestrated with inter-stage communication busses

CONTROL UNIT COMMUNICATION

SYSTEM OVERVIEW

- Localized control units
  - Send/receive event-driven commands between stages
  - State-machine based

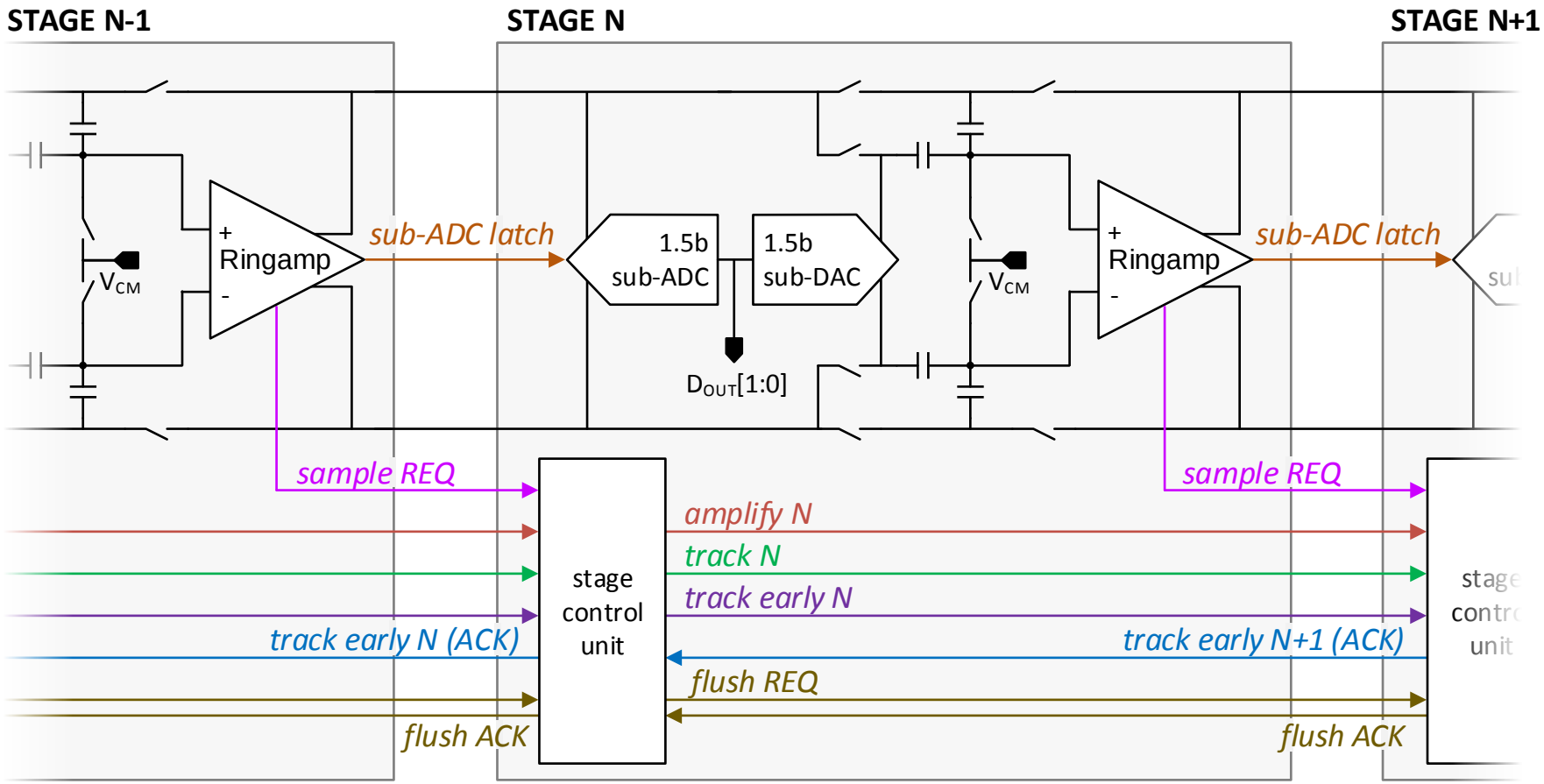


3.6: *A 6-to-600MS/s Fully Dynamic Ringamp Pipelined ADC with Asynchronous Event-Driven Clocking in 16nm*

CONTROL UNIT COMMUNICATION

SYSTEM OVERVIEW

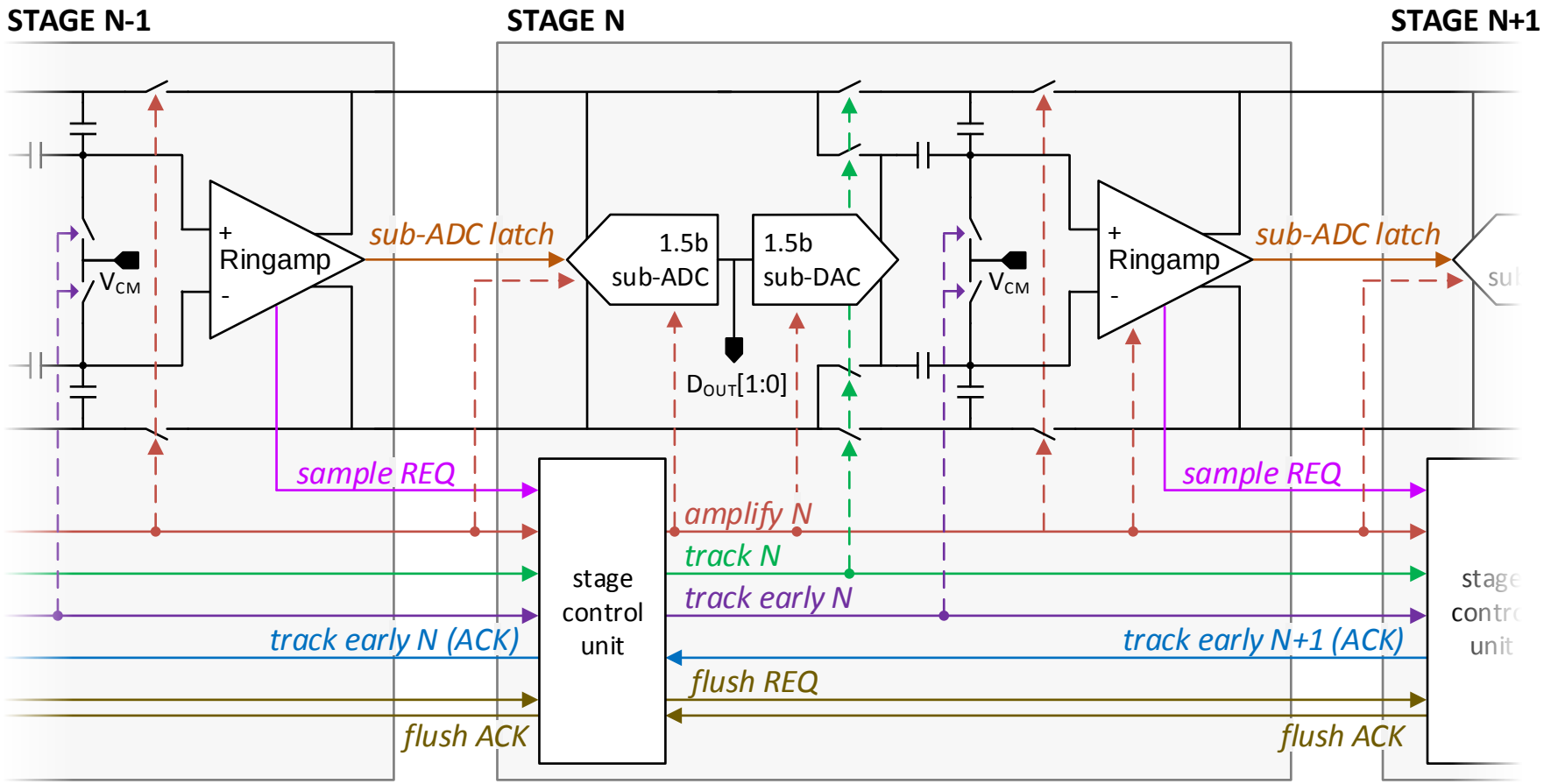
- Some critical event signals are sent directly from analog blocks



CONTROL UNIT COMMUNICATION

SYSTEM OVERVIEW

- Analog blocks driven directly by control bus

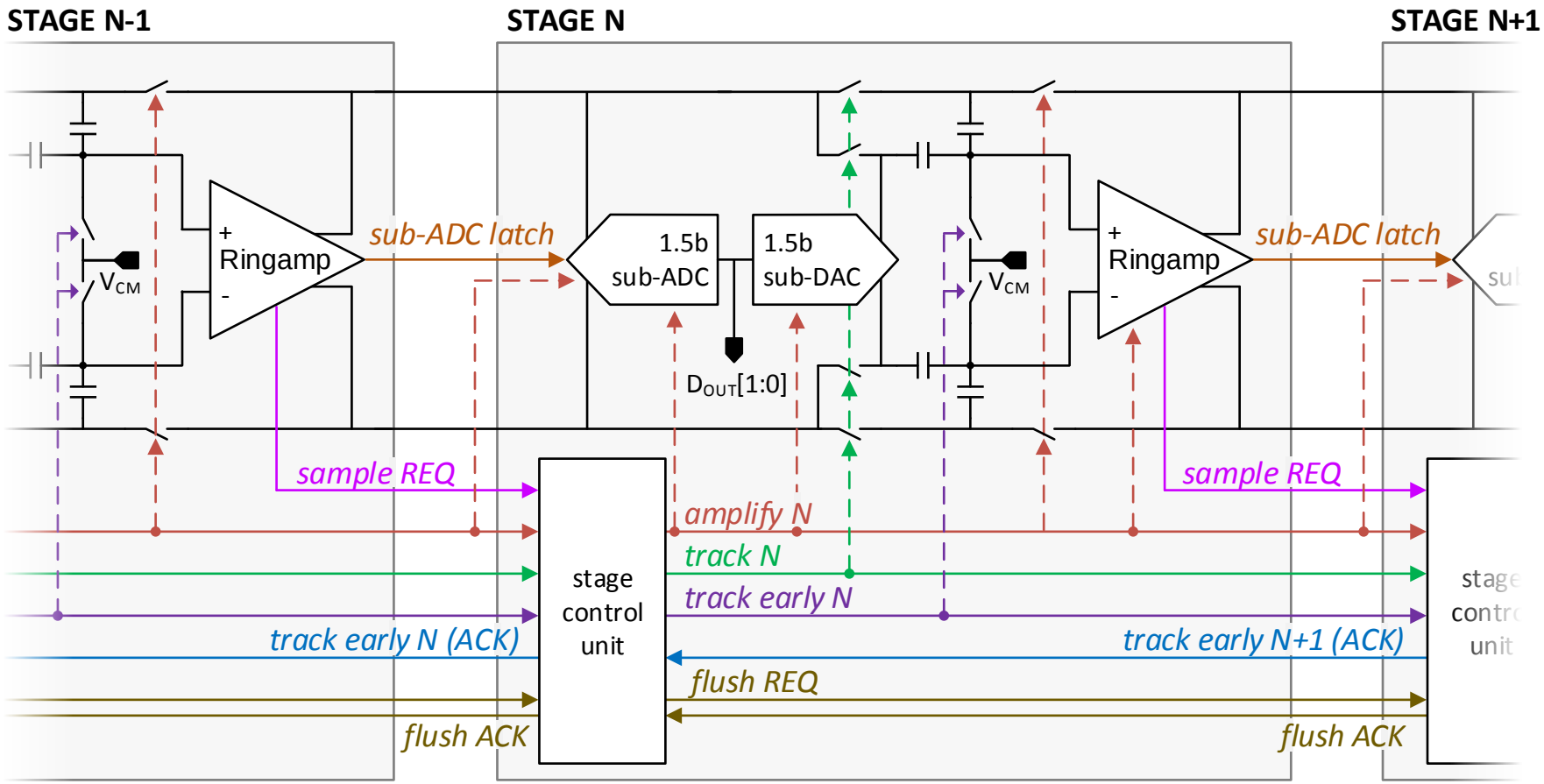


CONTROL UNIT COMMUNICATION

SYSTEM OVERVIEW

- Analog blocks driven directly by control bus

- BENEFIT: Both clock distribution and line driving
  - Lower power
  - Compact layout



3.6: A 6-to-600MS/s Fully Dynamic Ringamp Pipelined ADC with Asynchronous Event-Driven Clocking in 16nm

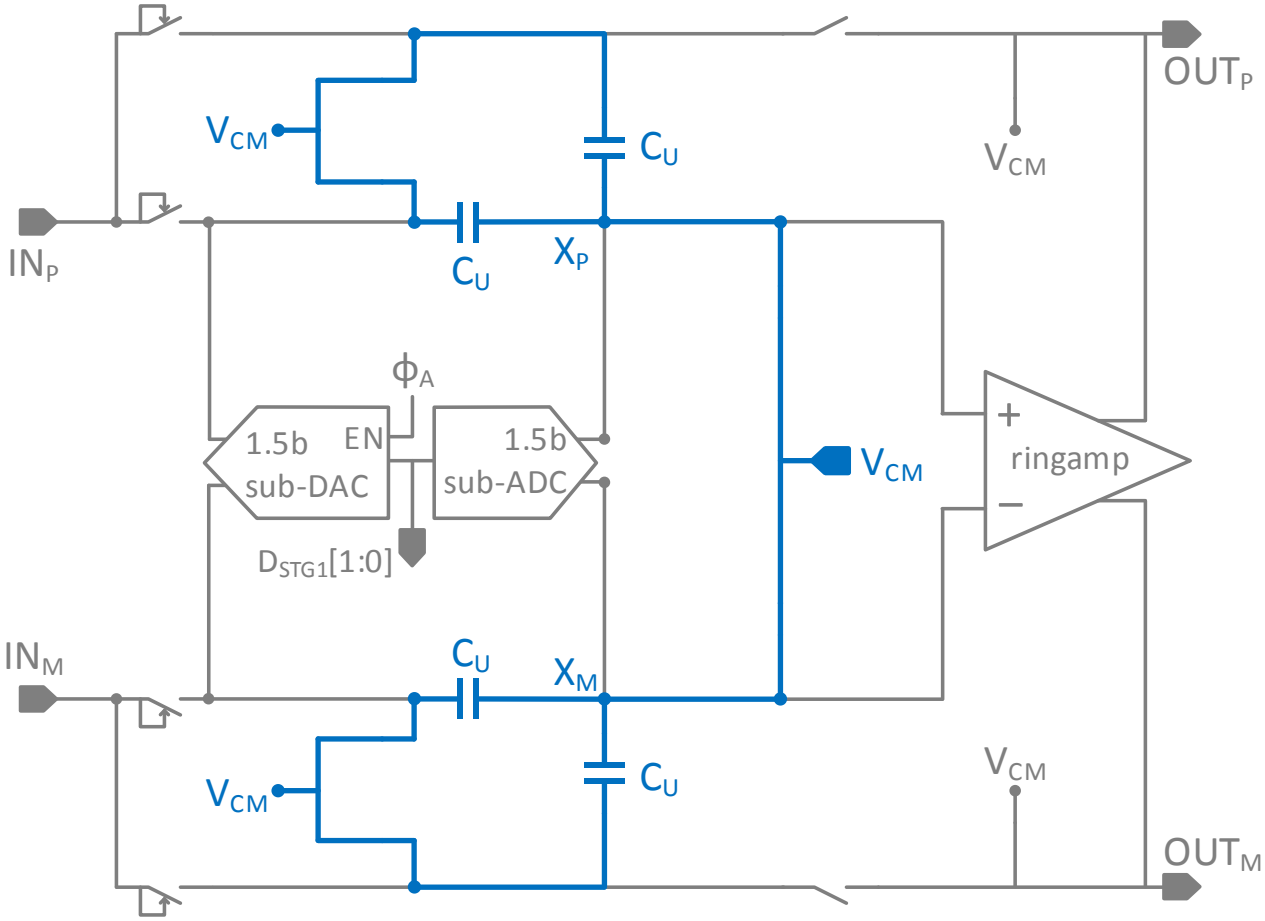
STAGE OPERATION

STAGE 1

SYSTEM OVERVIEW

- Clear (optional)

Stage 1 MDAC
with Passive Hold

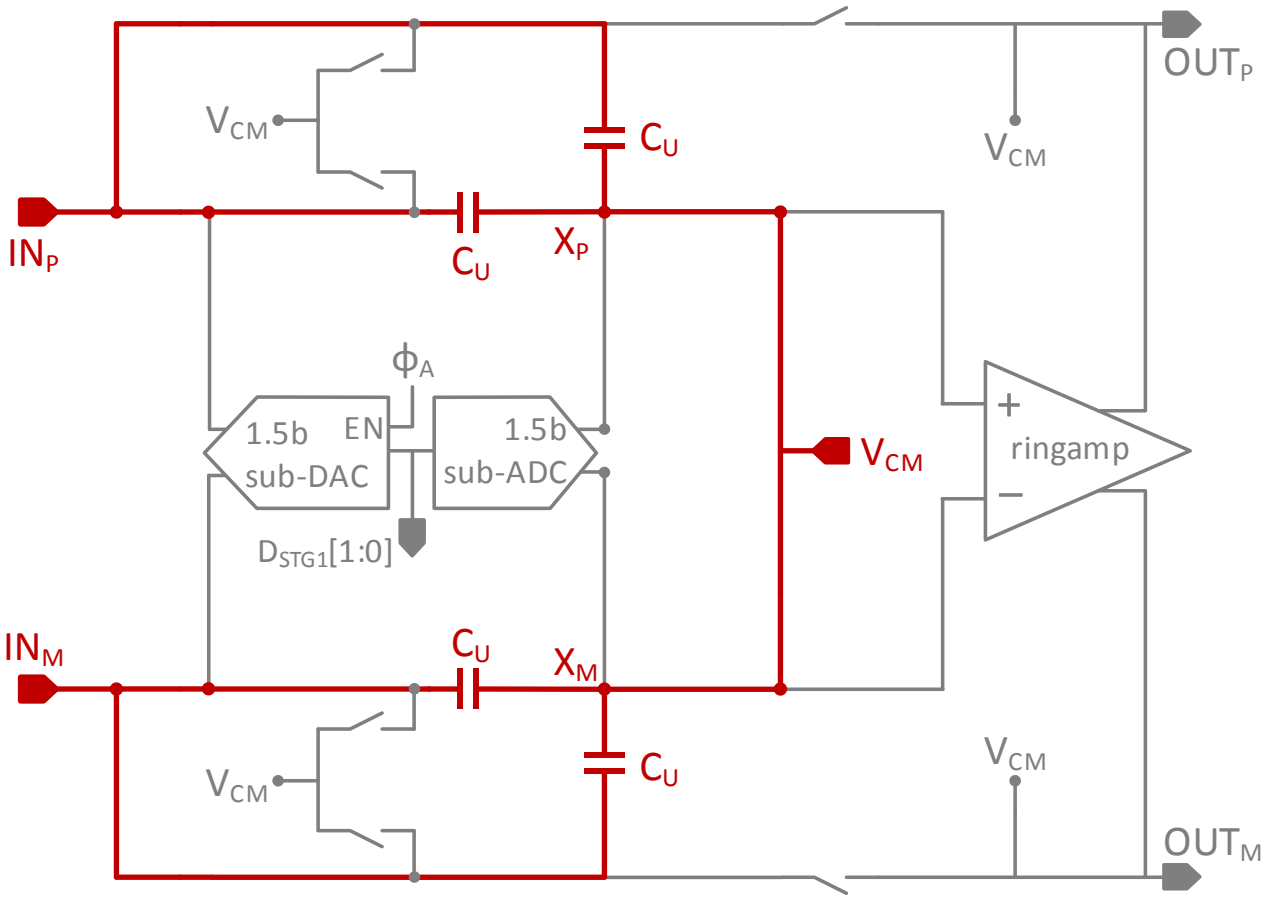


STAGE 1

SYSTEM OVERVIEW

- Clear (optional)
- Track

Stage 1 MDAC with Passive Hold

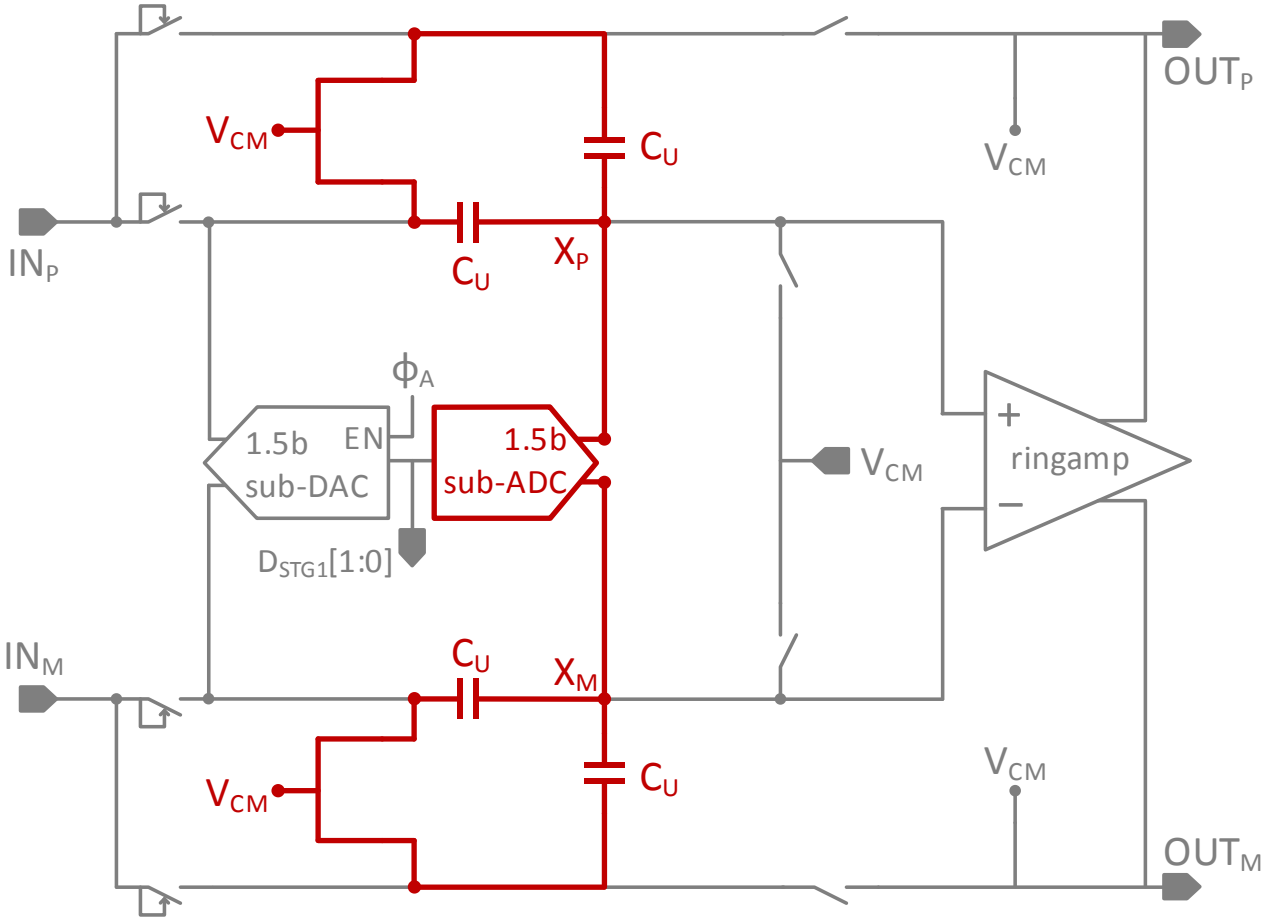


STAGE 1

SYSTEM OVERVIEW

- Clear (optional)
- Track
- Quantize (Passive hold)
  - Explained in talk 3.1

Stage 1 MDAC with Passive Hold

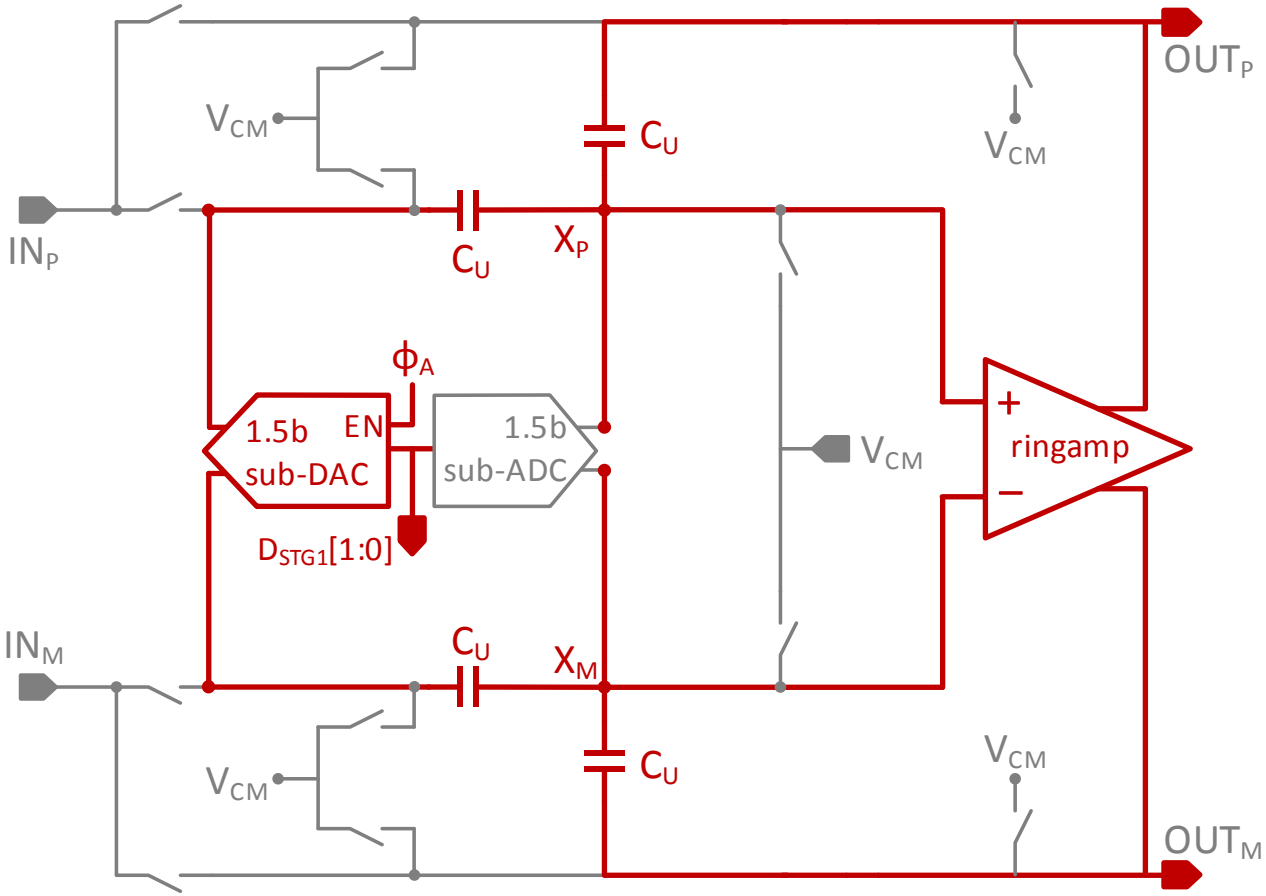


STAGE 1

SYSTEM OVERVIEW

- Clear (optional)
- Track
- Quantize (Passive hold)
- Amplify

Stage 1 MDAC with Passive Hold

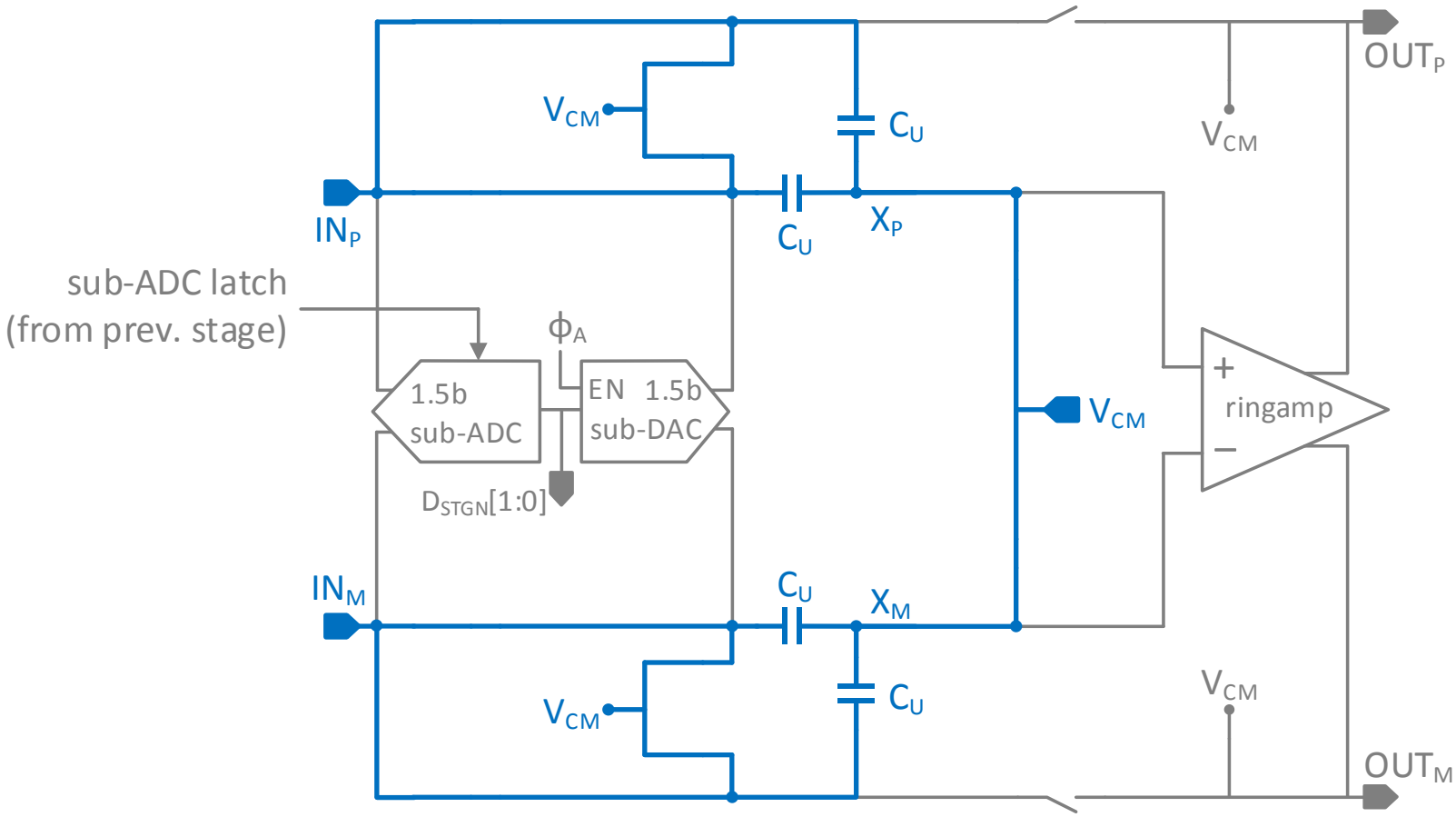


STAGES 2-7

IMPLEMENTATION DETAILS

- Clear (optional)

Stages 2-7 MDAC
with Early Quantization



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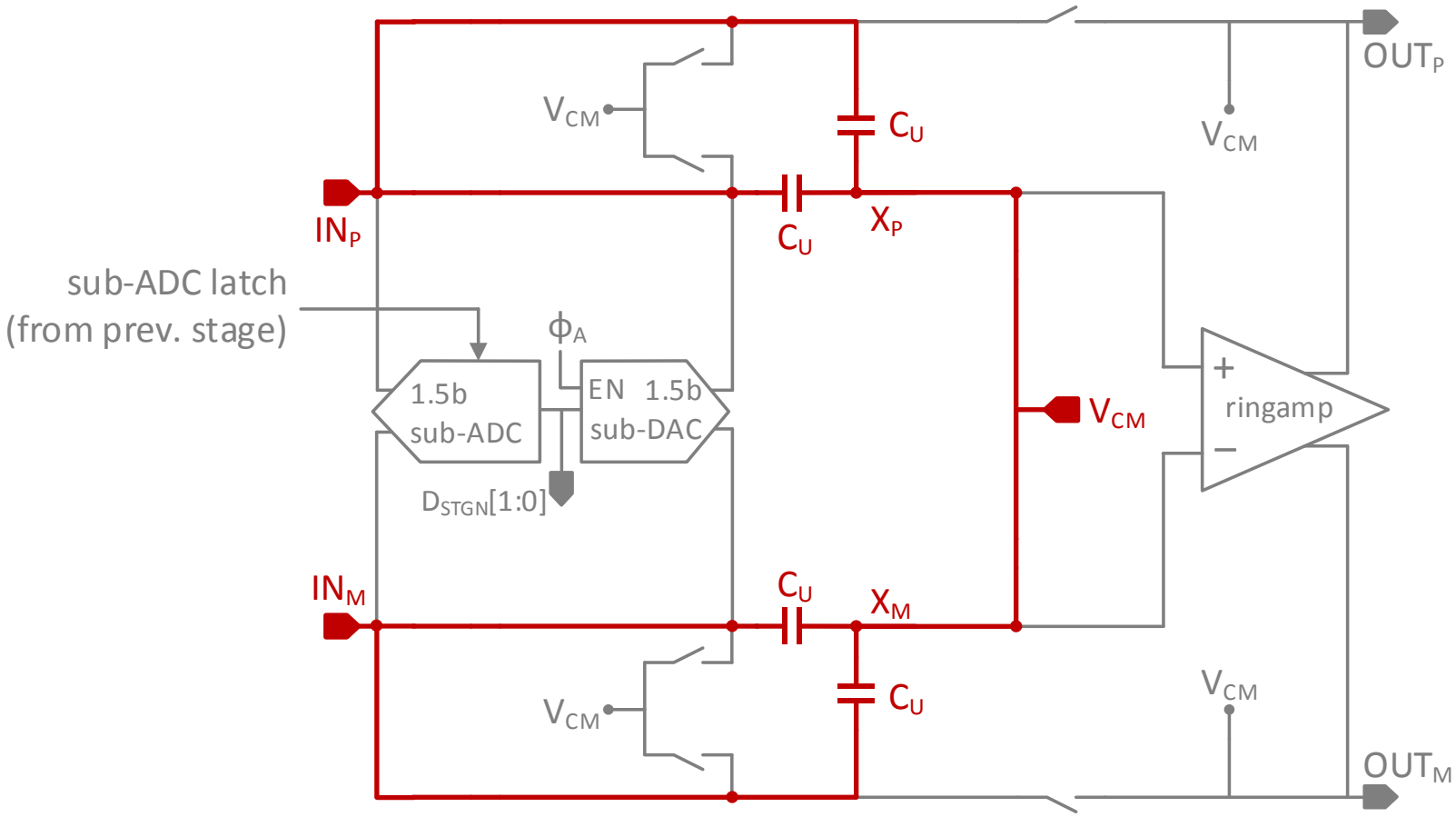
IMPLEMENTATION DETAILS

- Clear (optional)
- Track

Stages 2-7 MDAC with Early Quantization

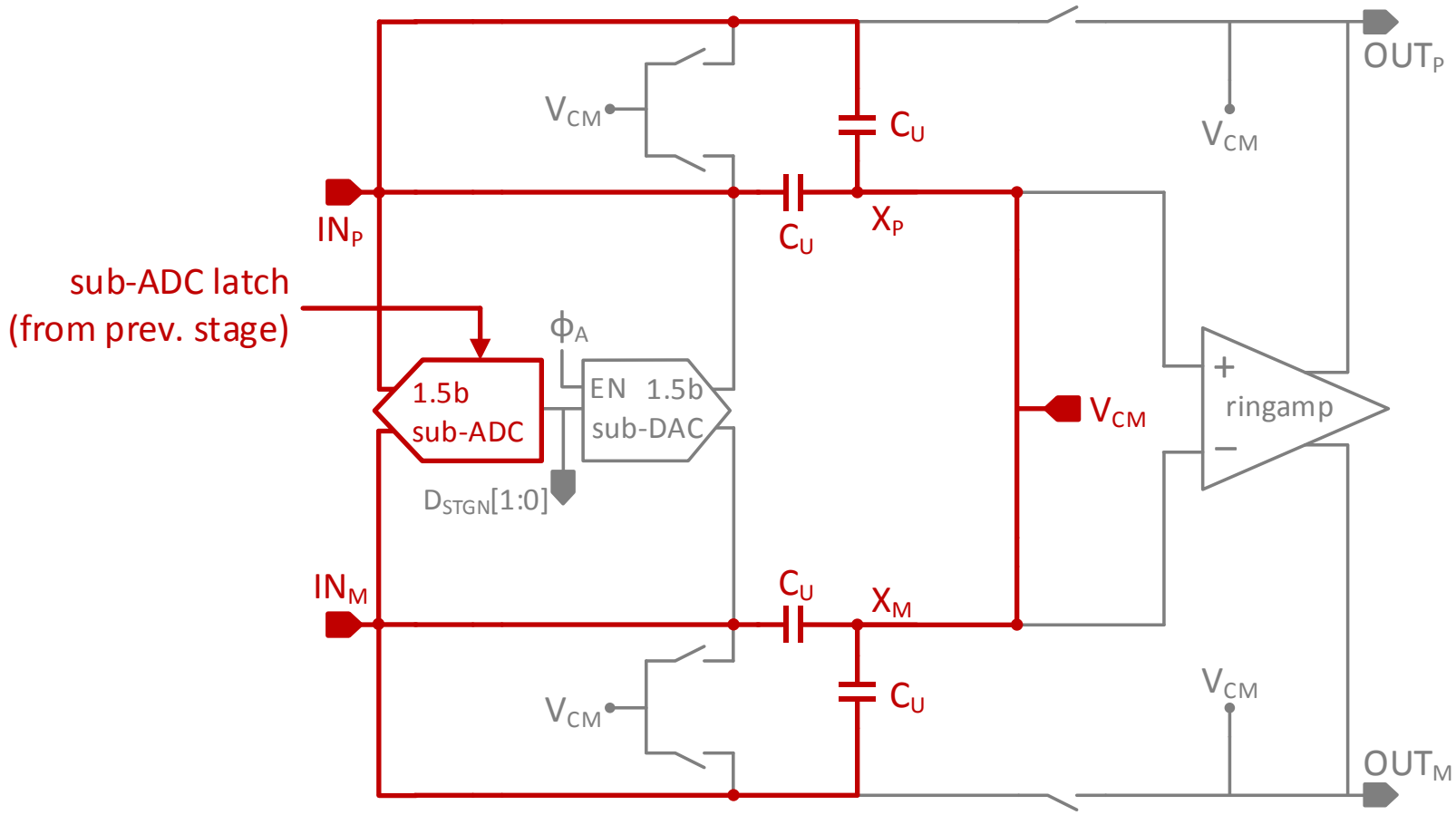


STAGES 2-7

IMPLEMENTATION DETAILS

- Clear (optional)
- Track
  - Early quantize (1.5b)

Stages 2-7 MDAC with Early Quantization



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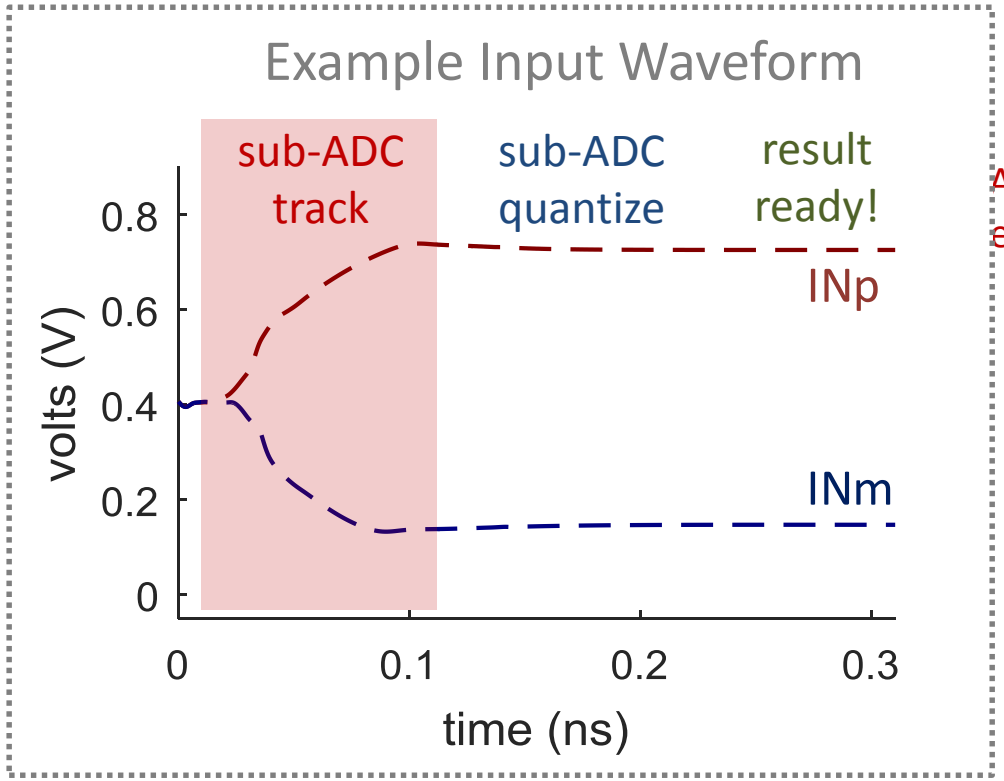
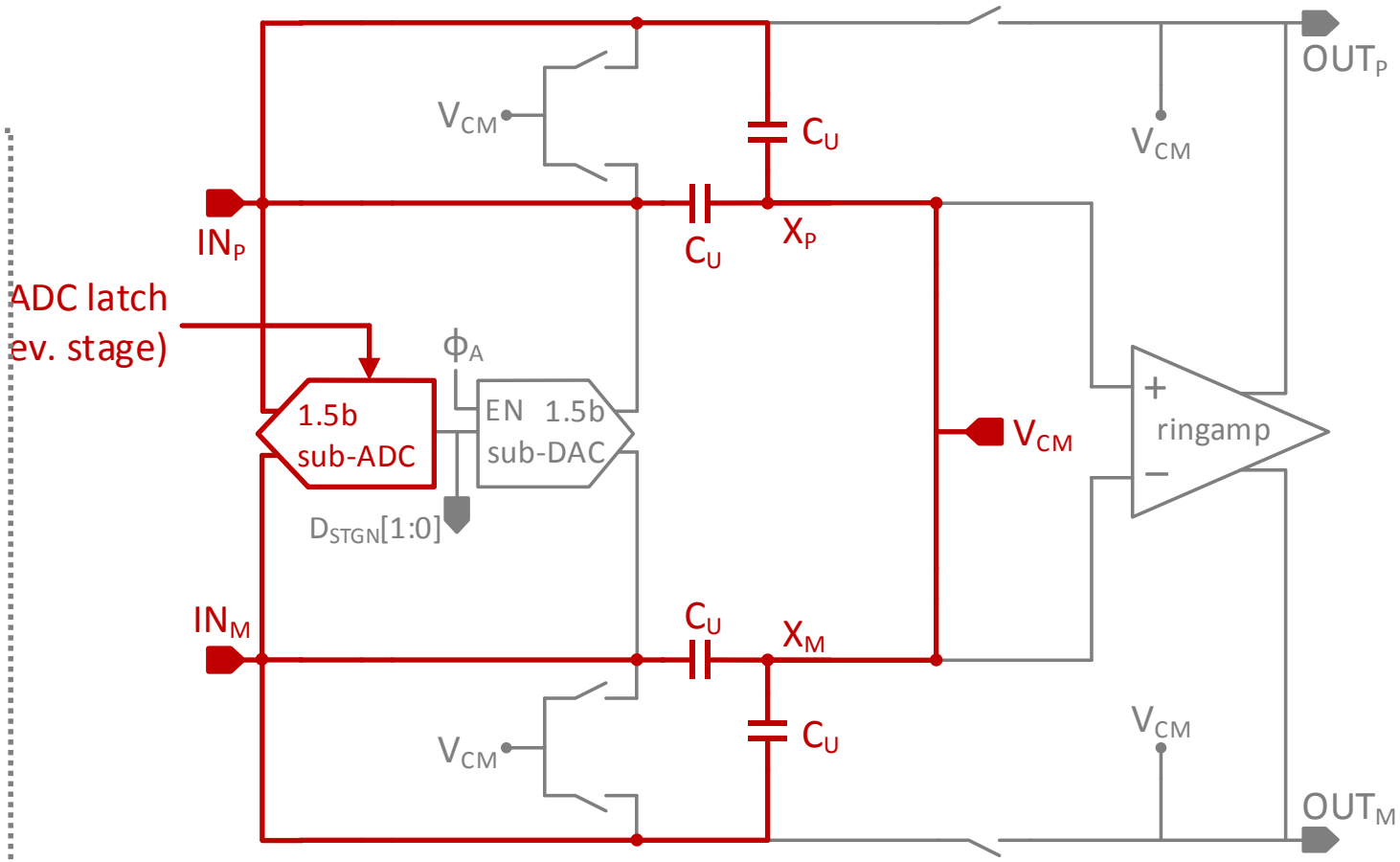


Stages 2-7 MDAC with Early Quantization



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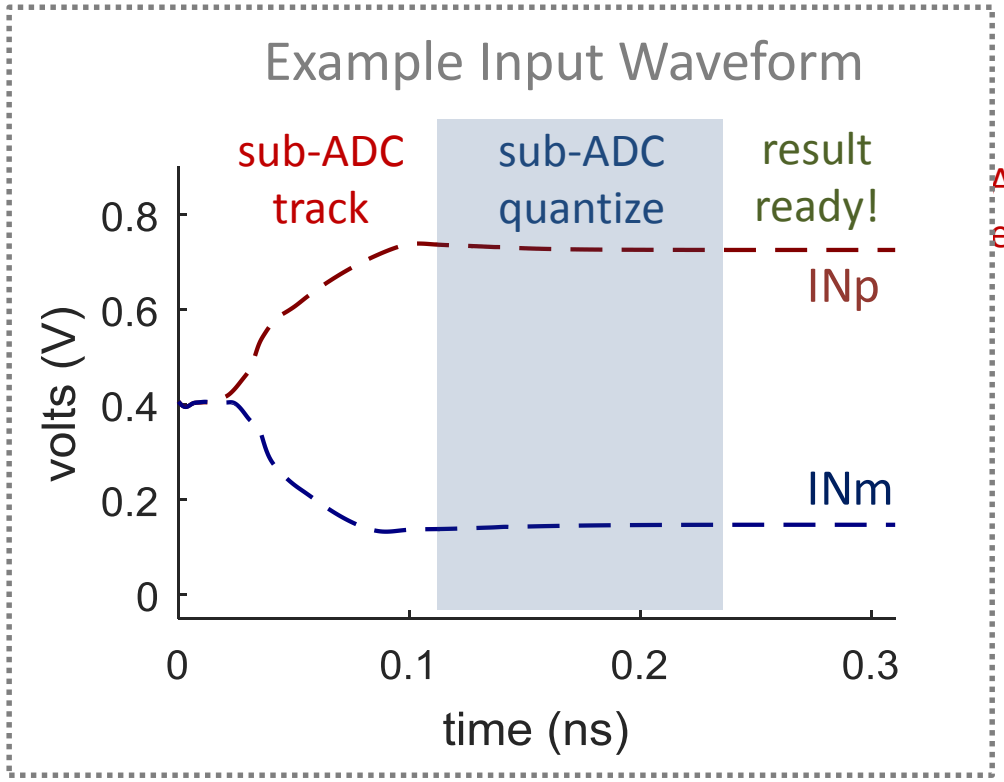

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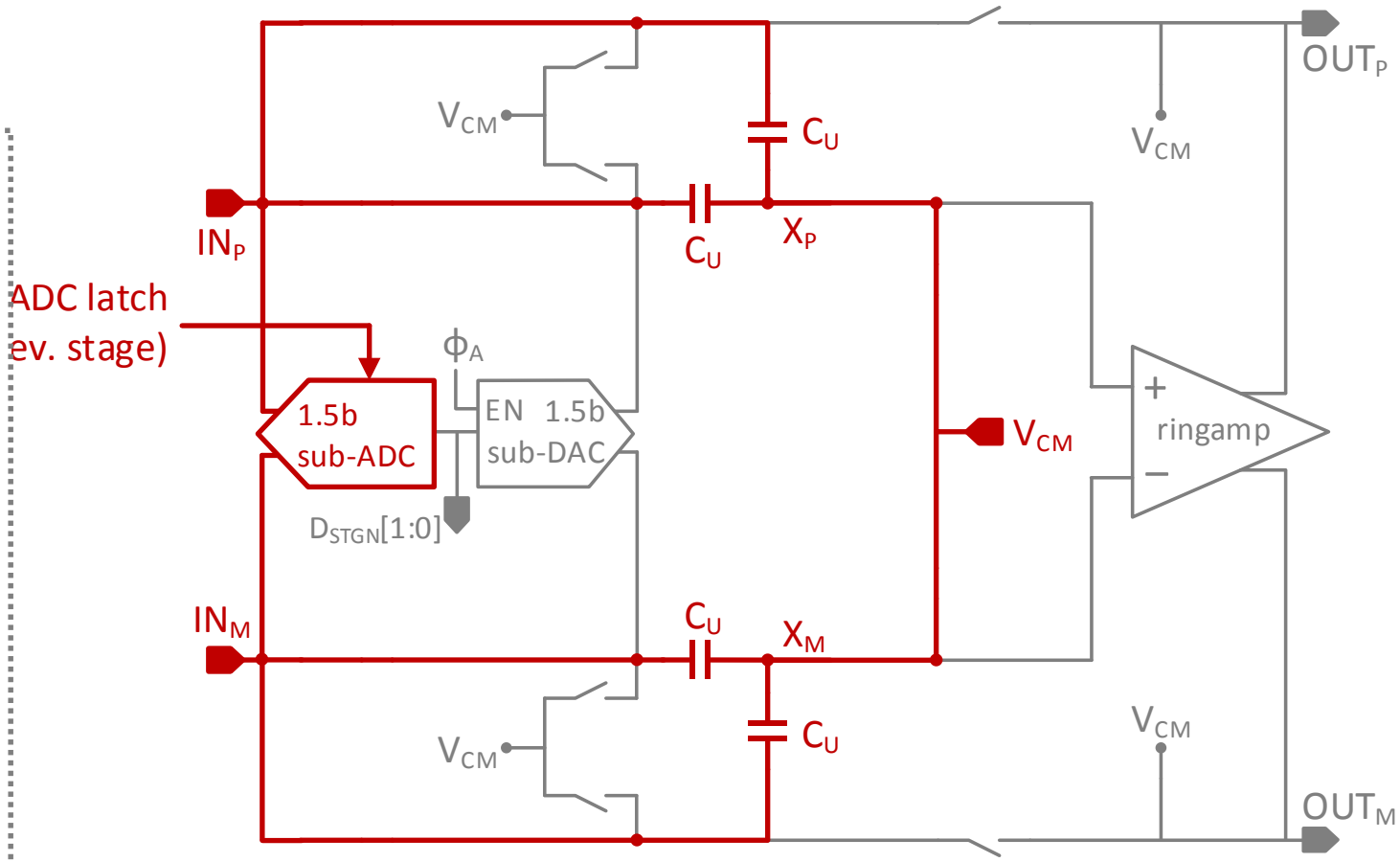

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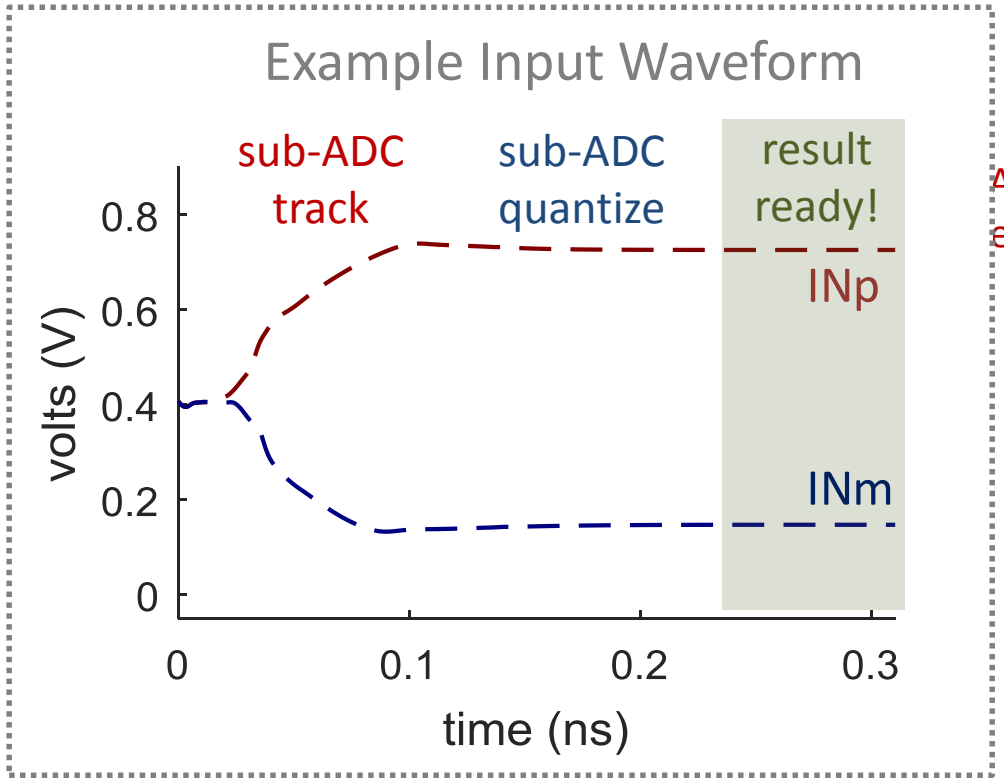
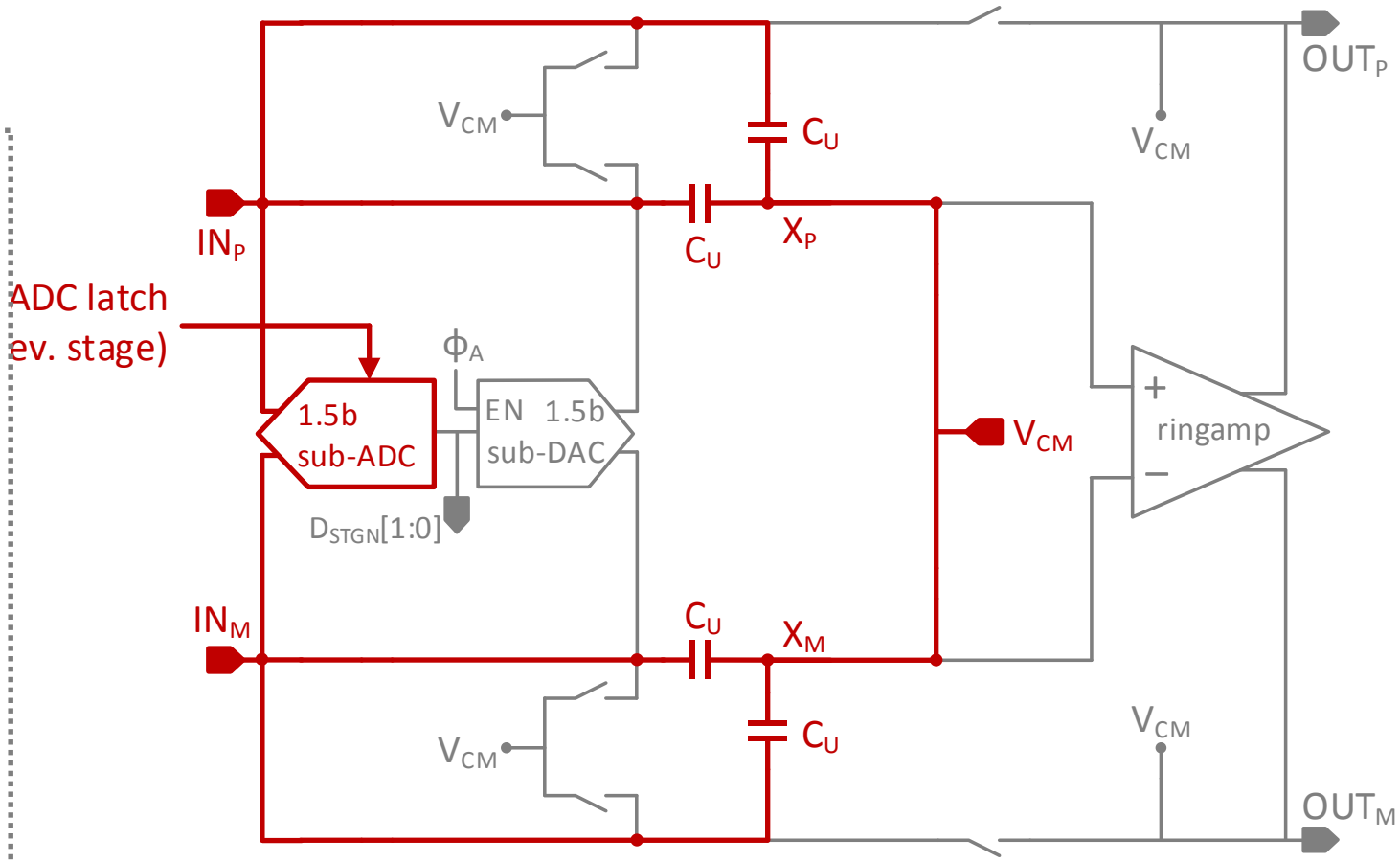


Stages 2-7 MDAC with Early Quantization

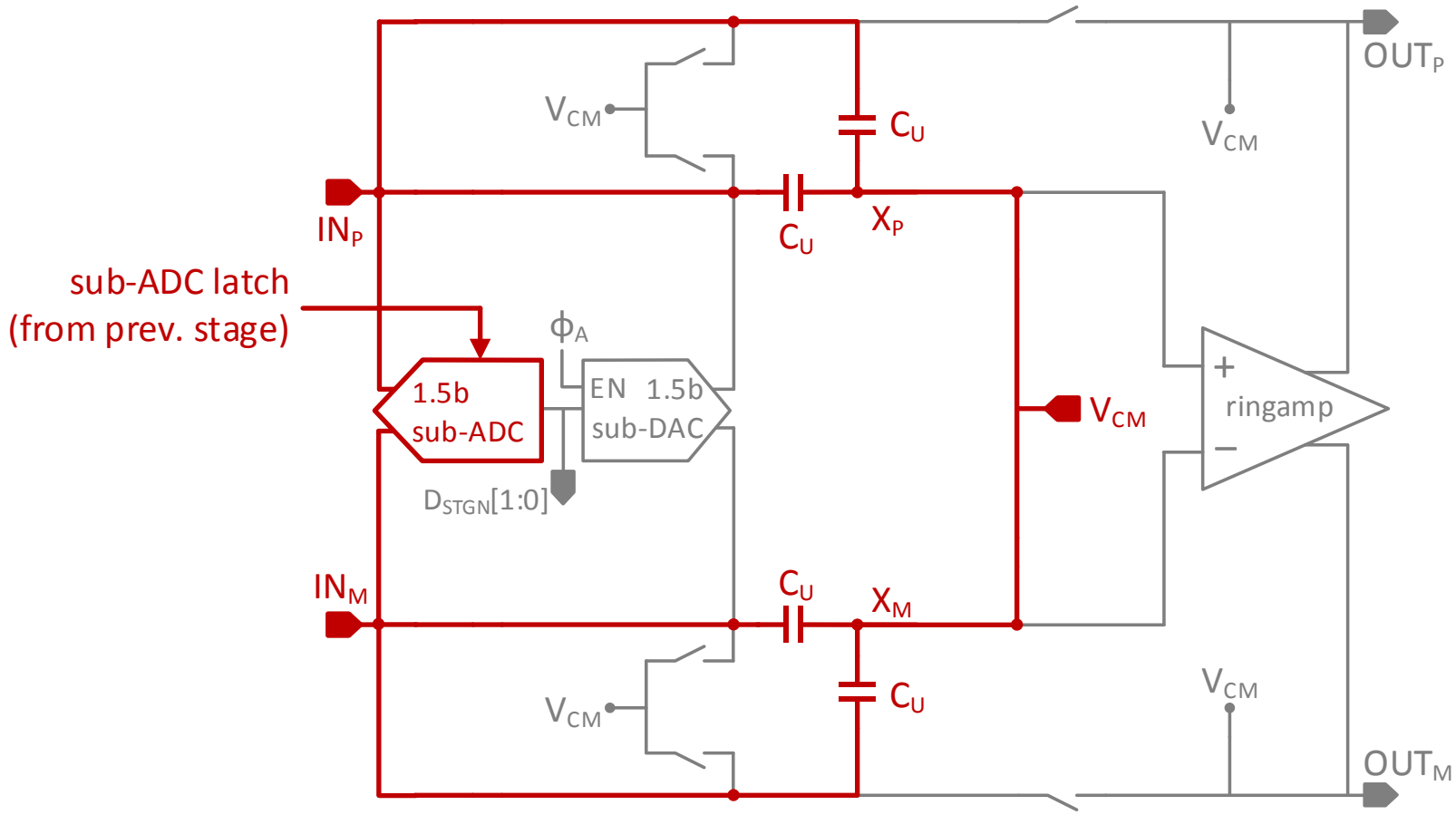


STAGES 2-7

IMPLEMENTATION DETAILS

- Clear (optional)
- Track
  - Early quantize (1.5b)
  - sub-ADC removed from critical timing path. ☺

Stages 2-7 MDAC with Early Quantization

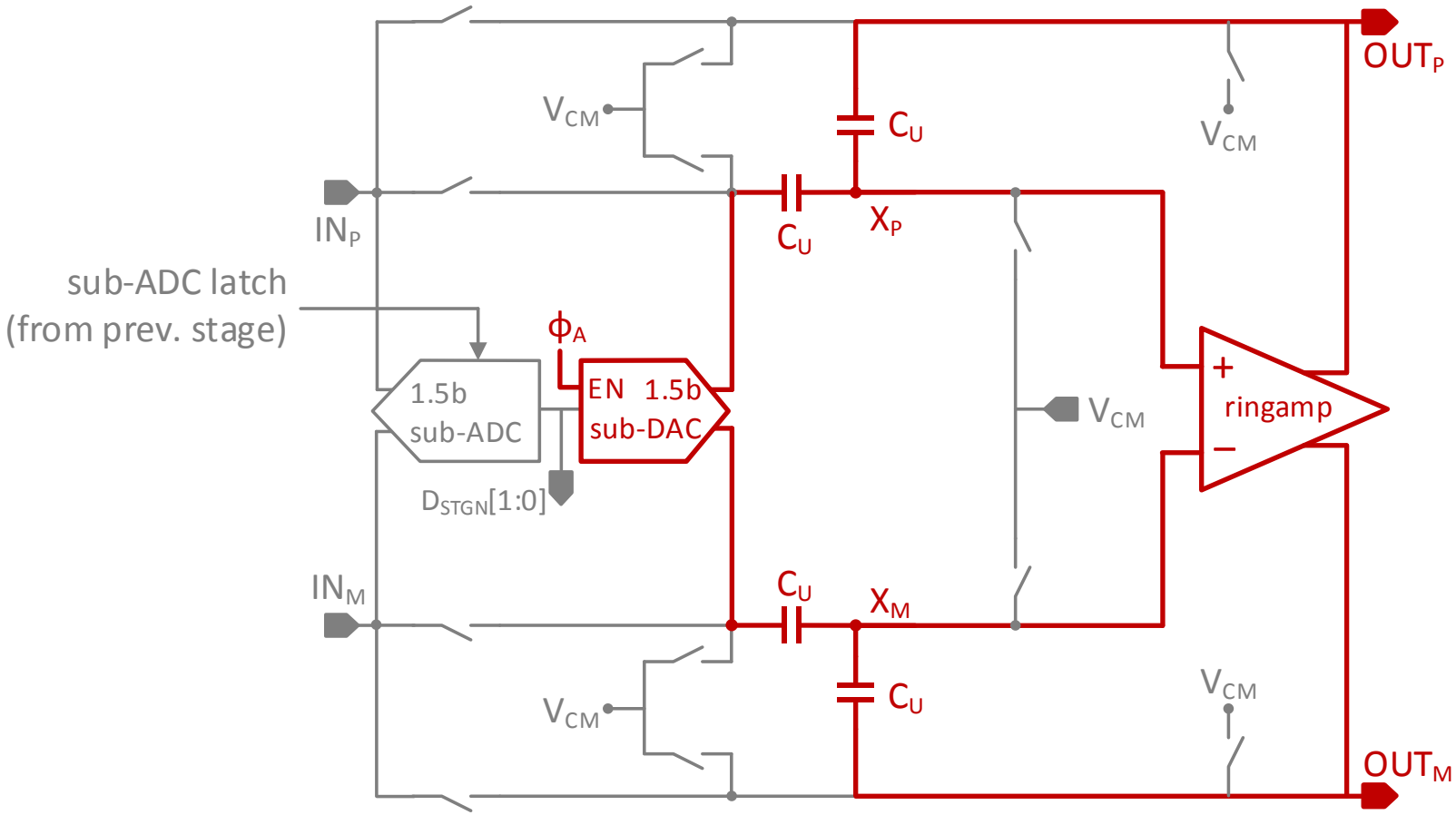


STAGES 2-7

IMPLEMENTATION DETAILS

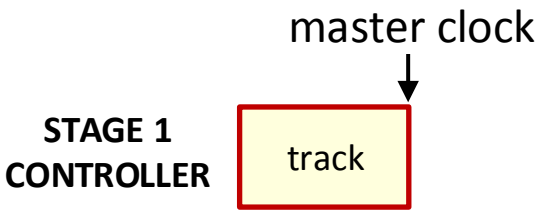
- Clear (optional)
- Track
  - Early quantize (1.5b)
- Amplify

Stages 2-7 MDAC with Early Quantization



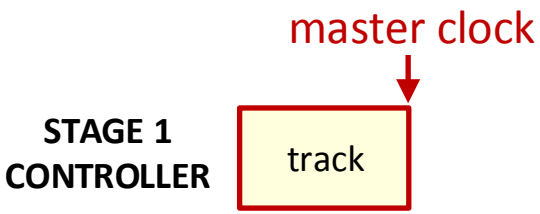
TIMING OPERATION EXAMPLE

EVENT-DRIVEN TIMING CONTROL



- Pipeline in idle state, waiting for a master clock...

EVENT-DRIVEN TIMING CONTROL



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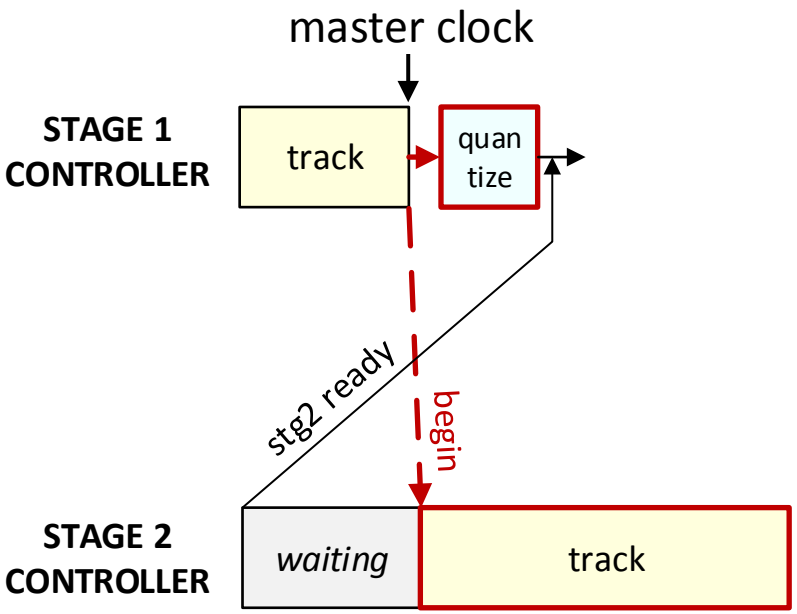

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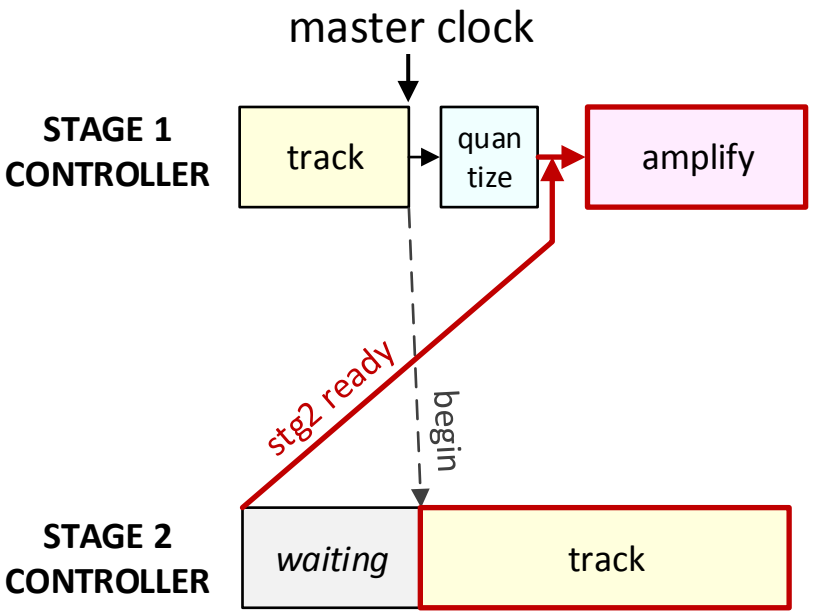

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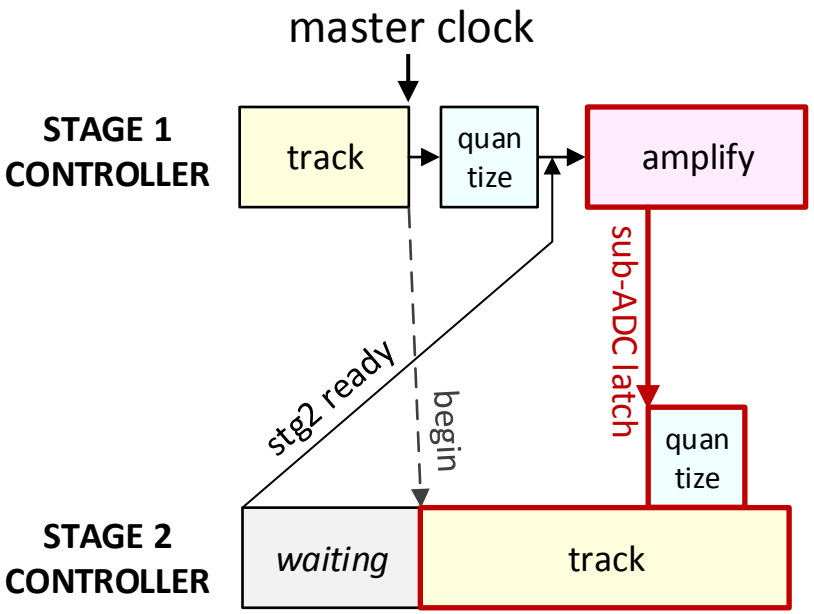

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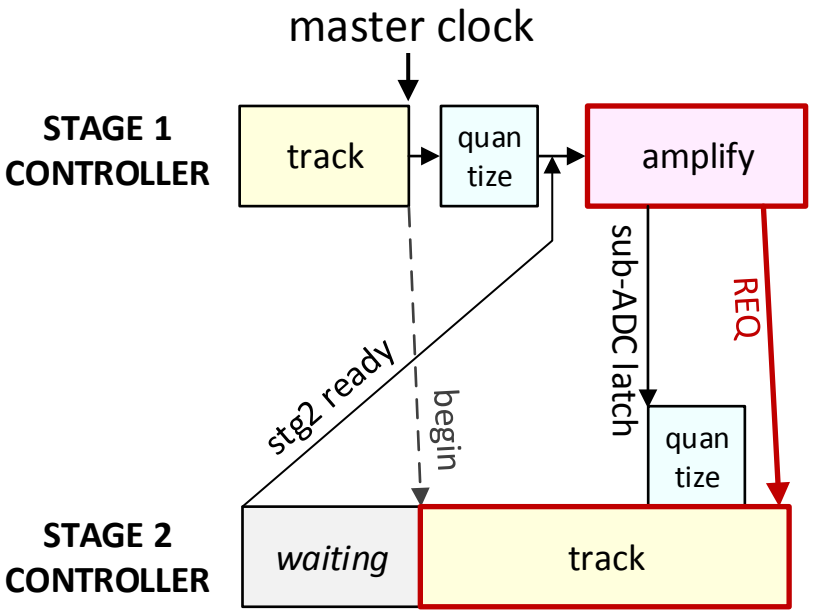

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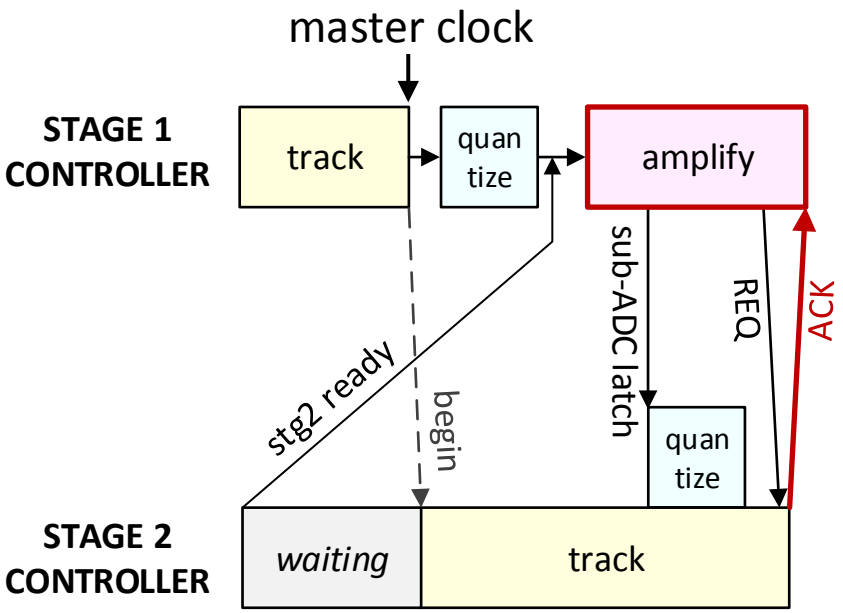

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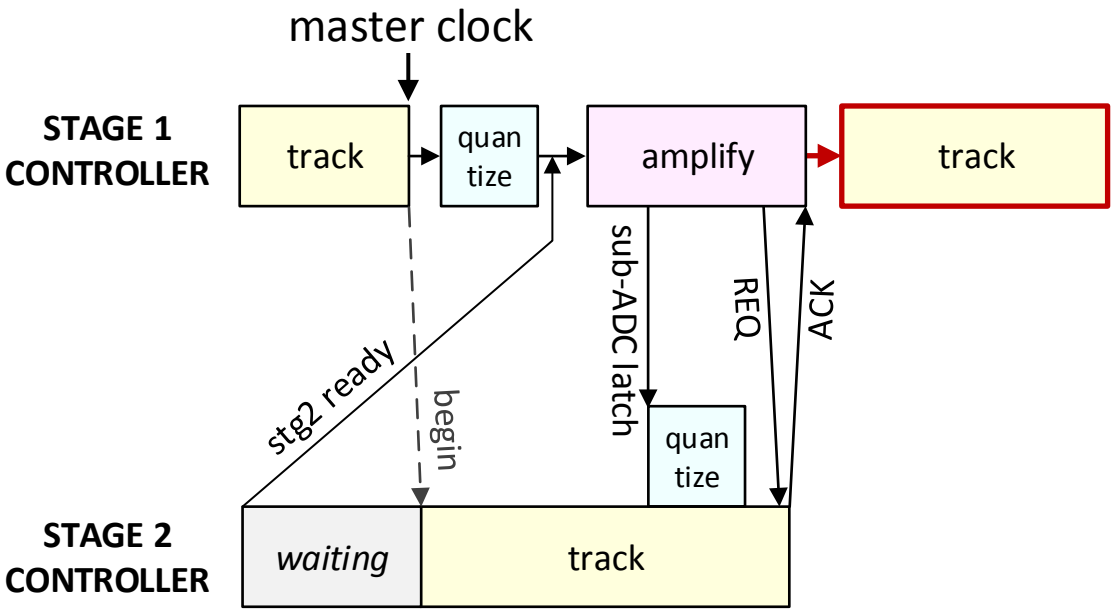

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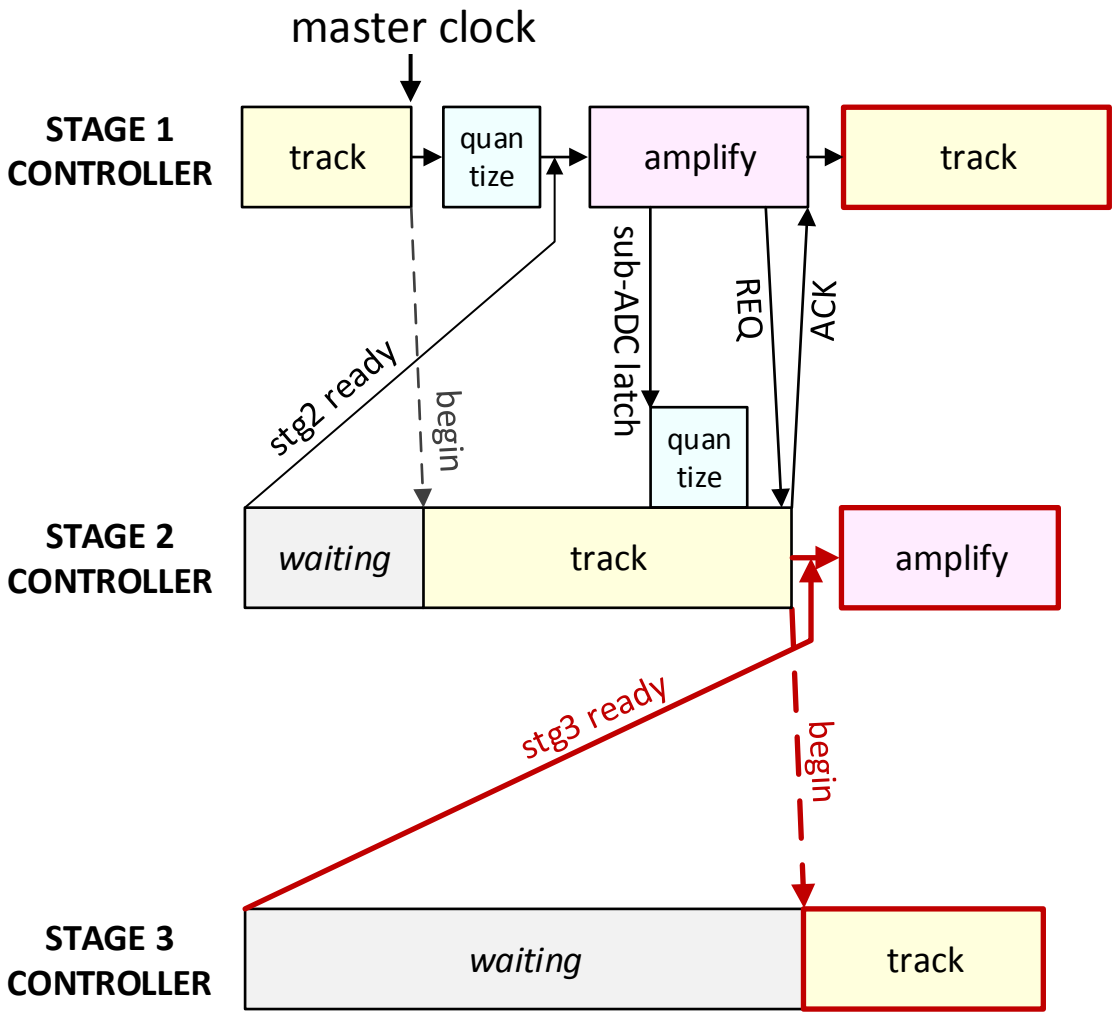

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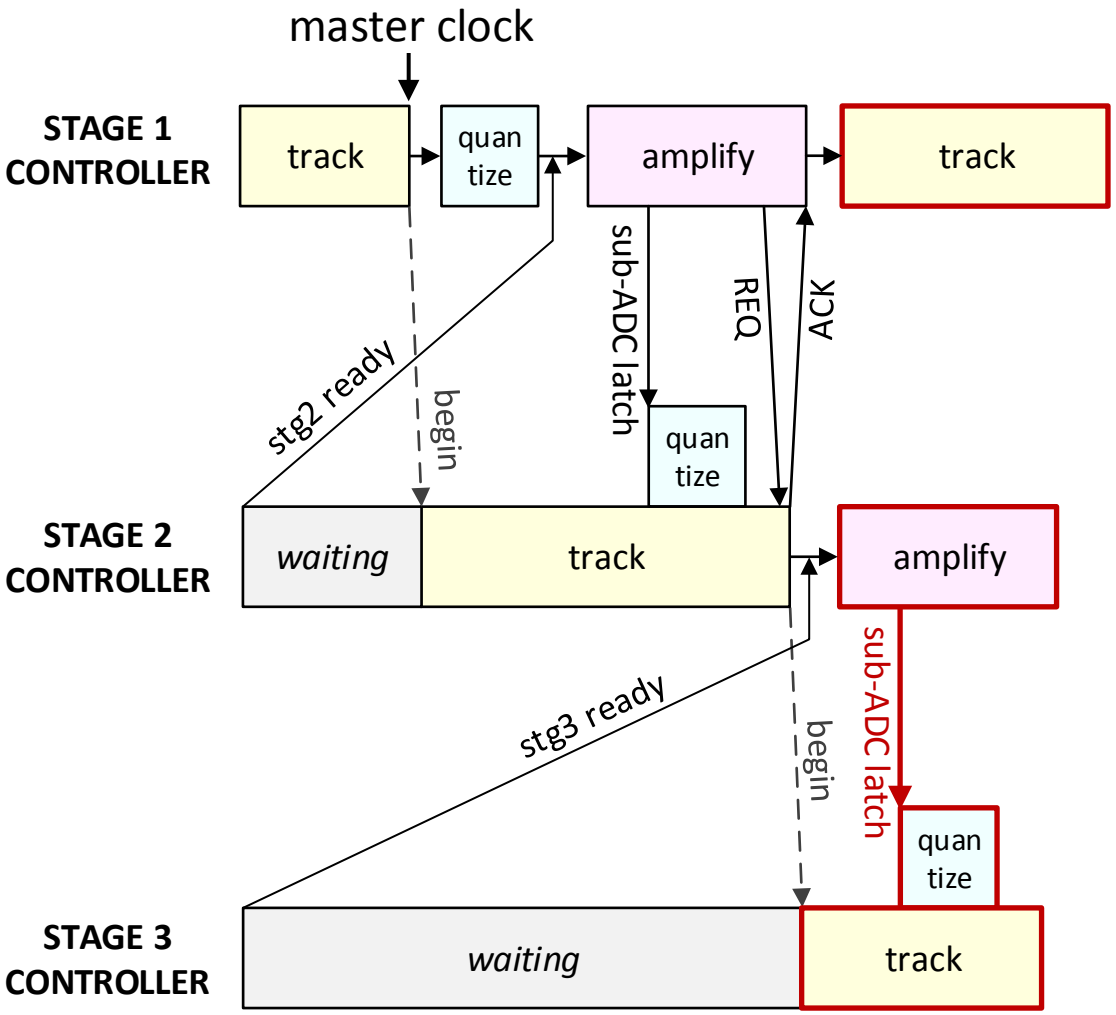

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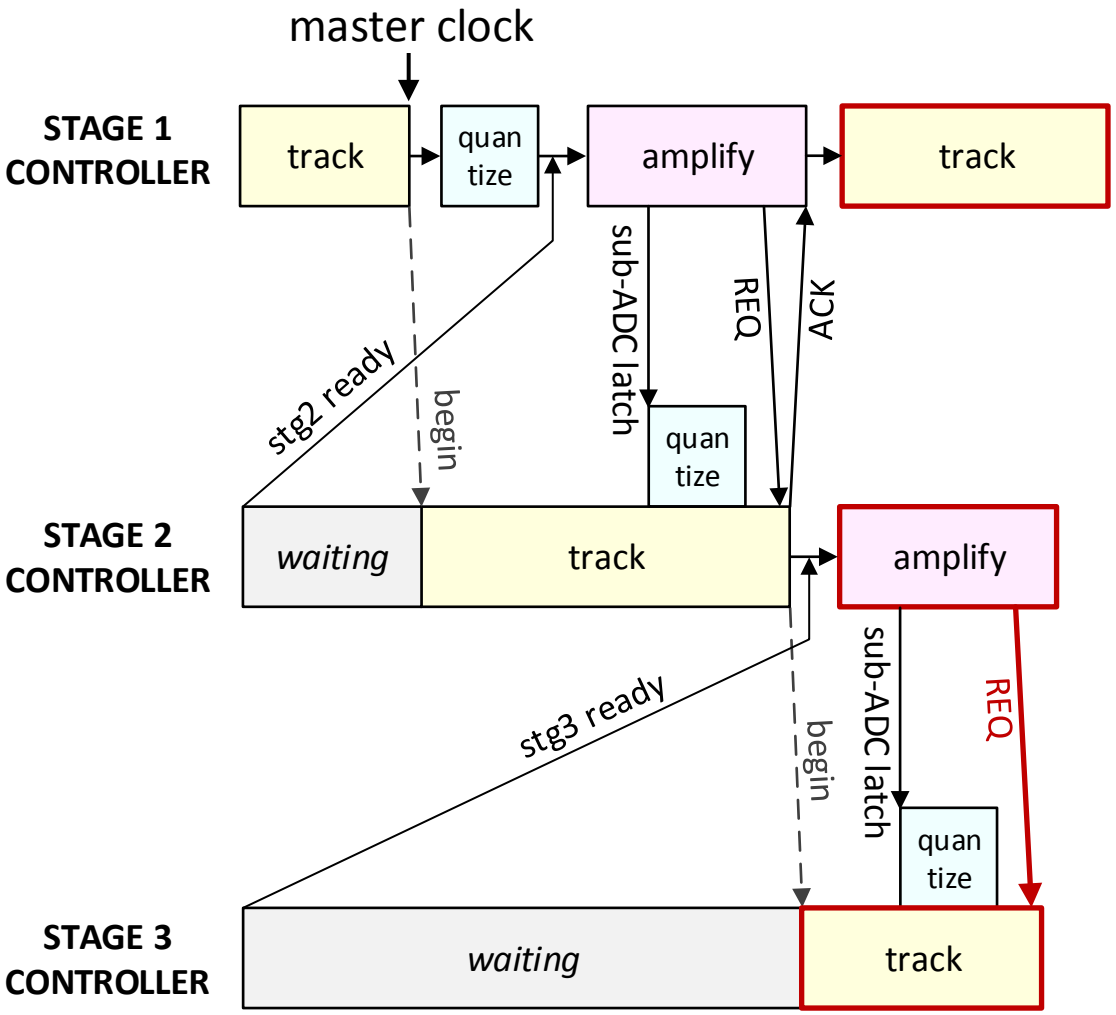

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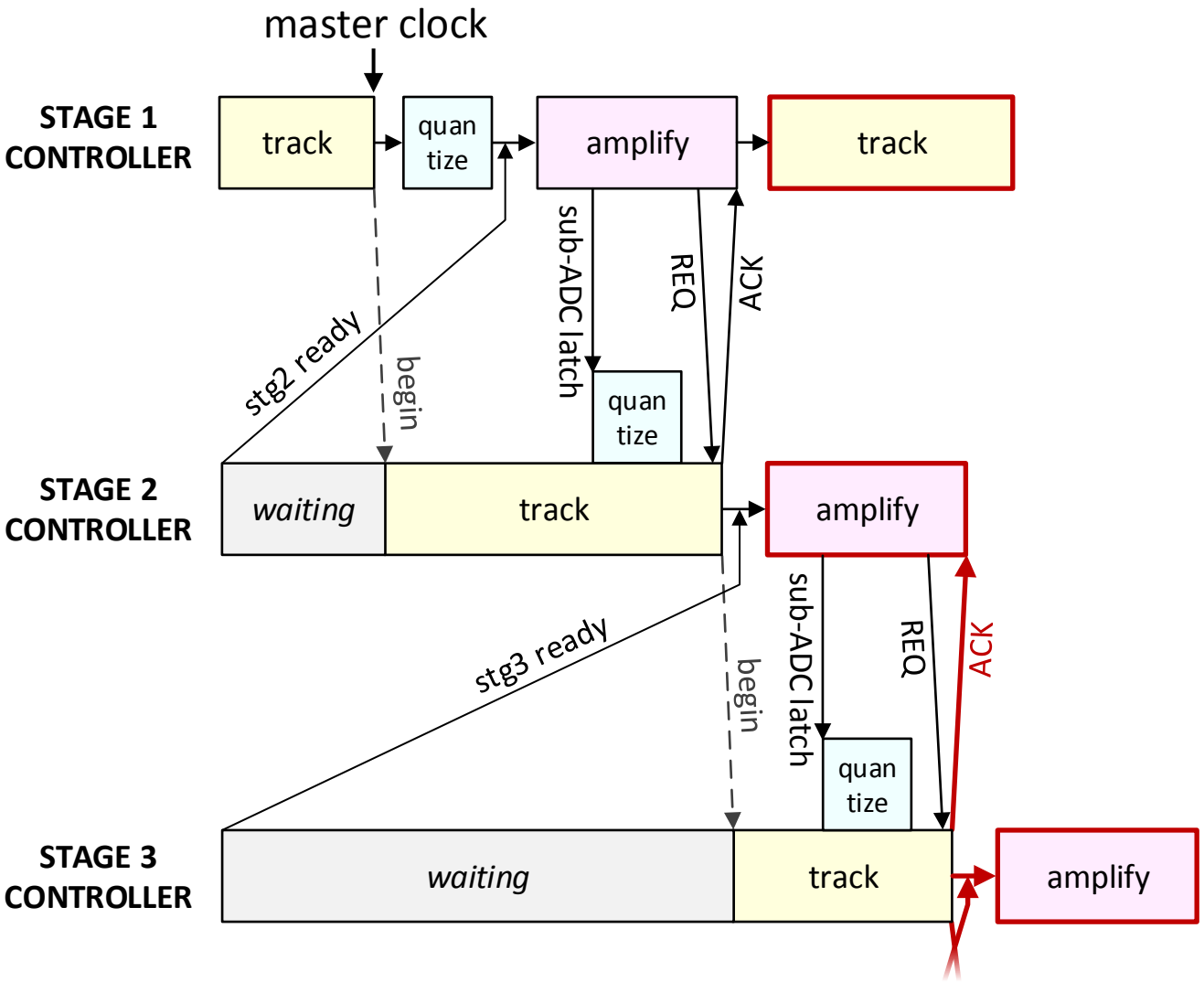

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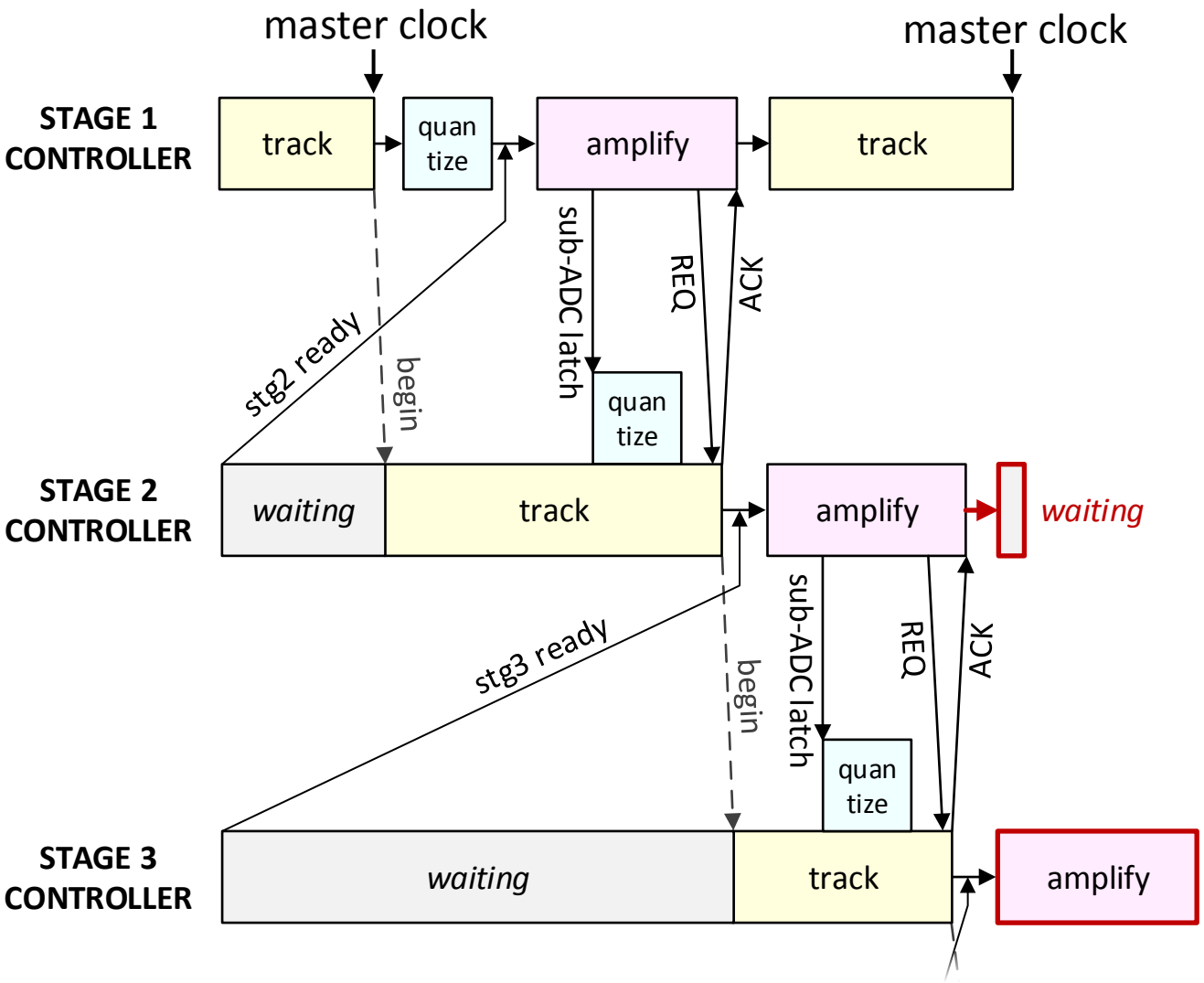

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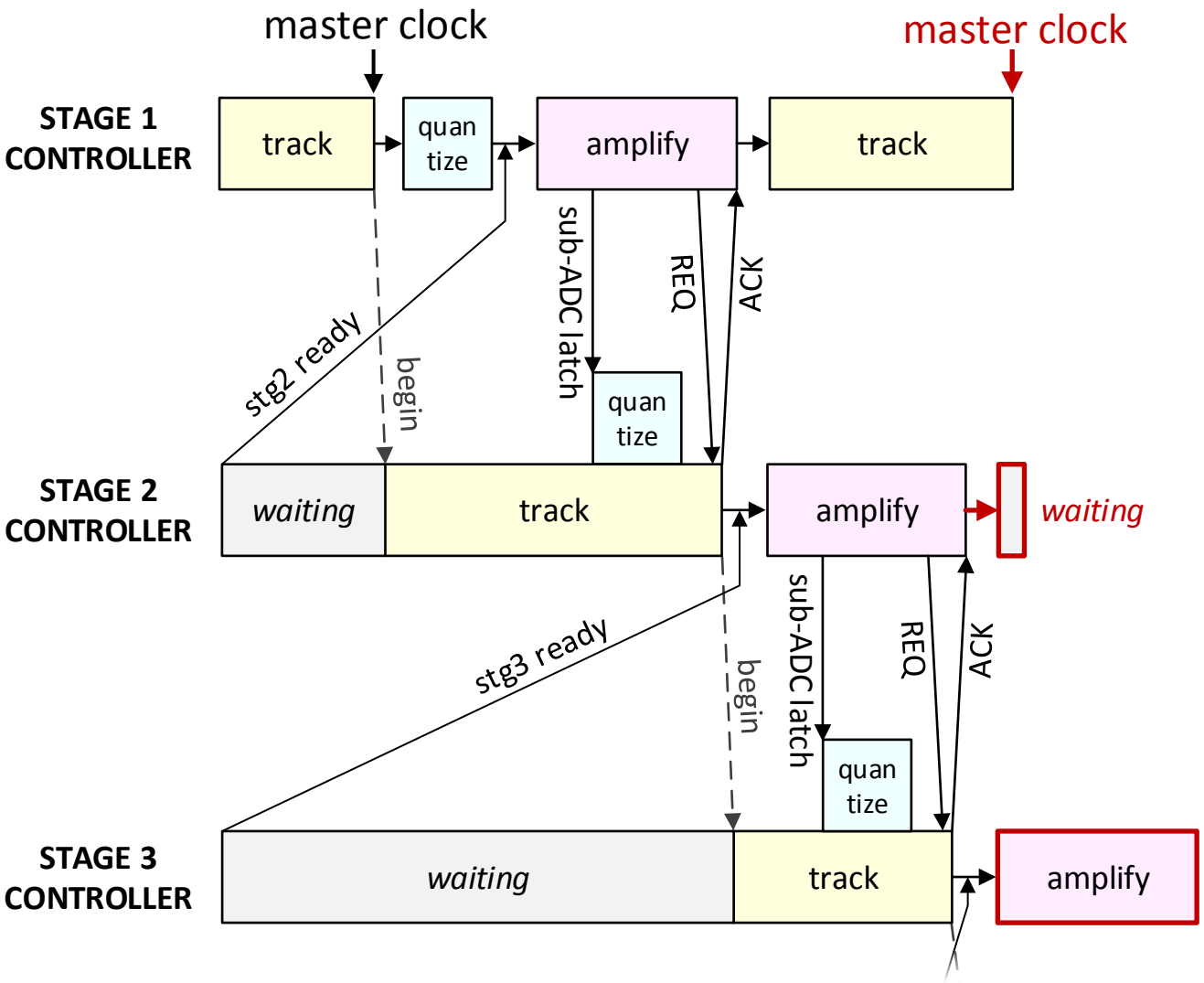

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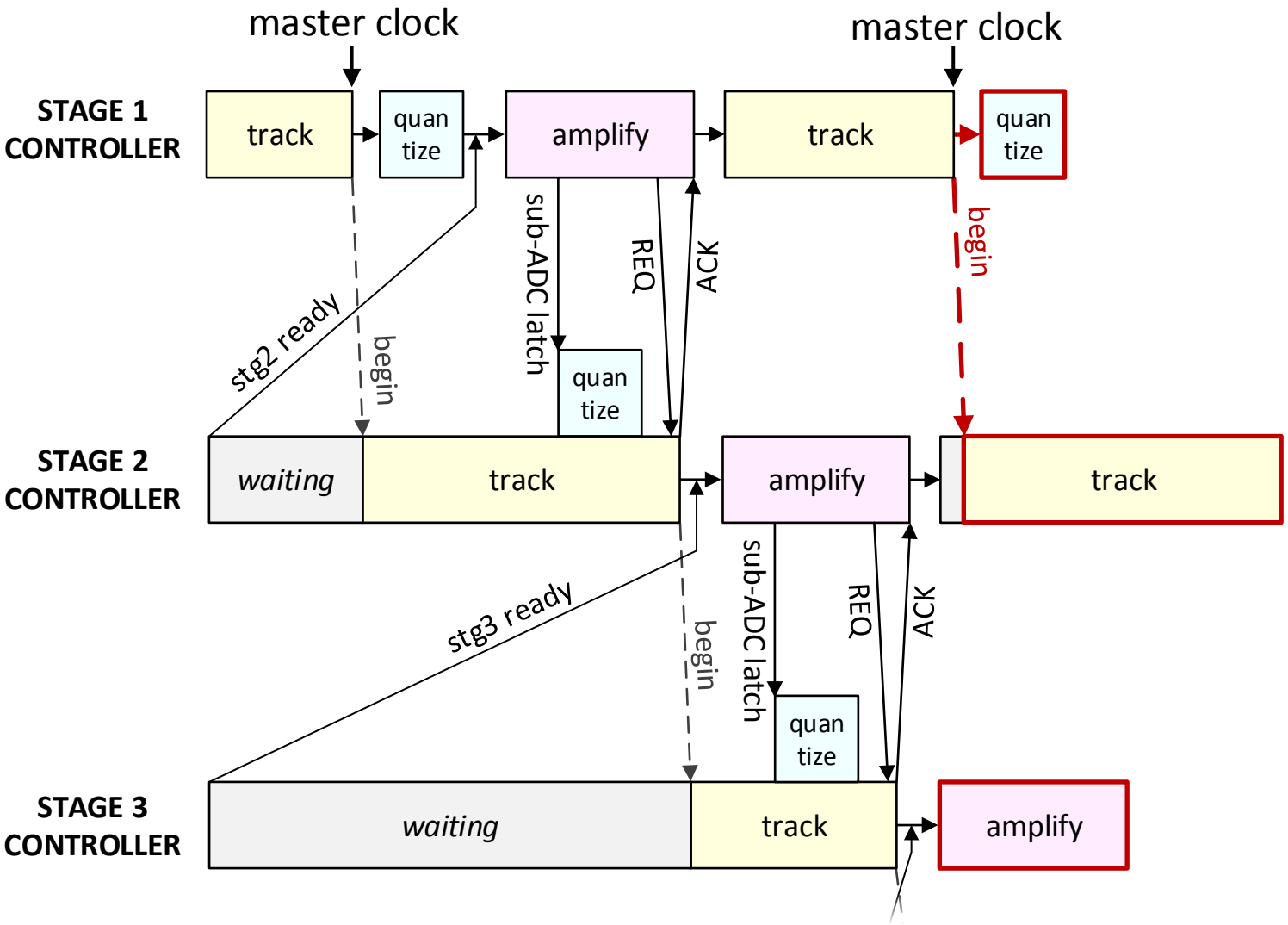

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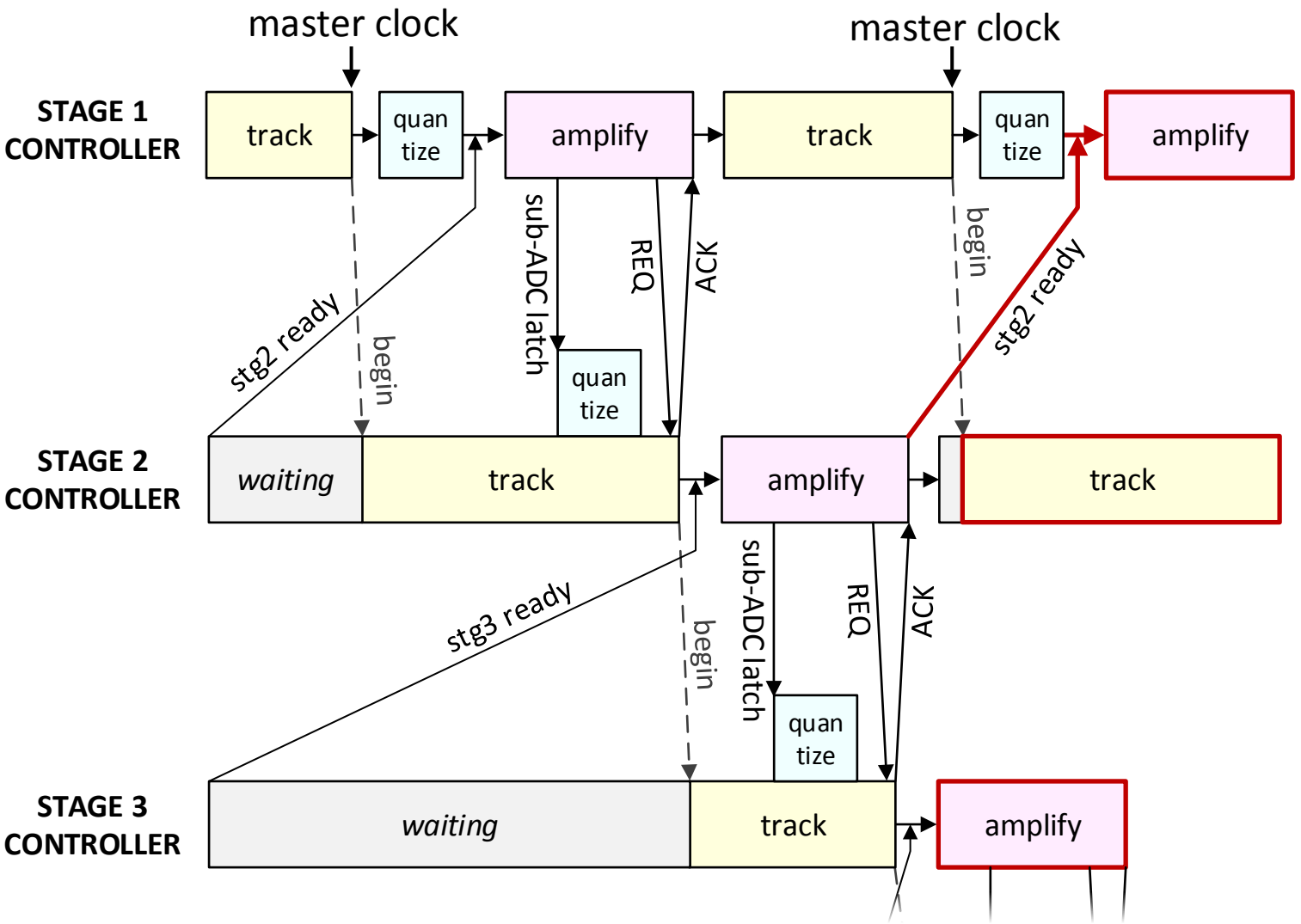

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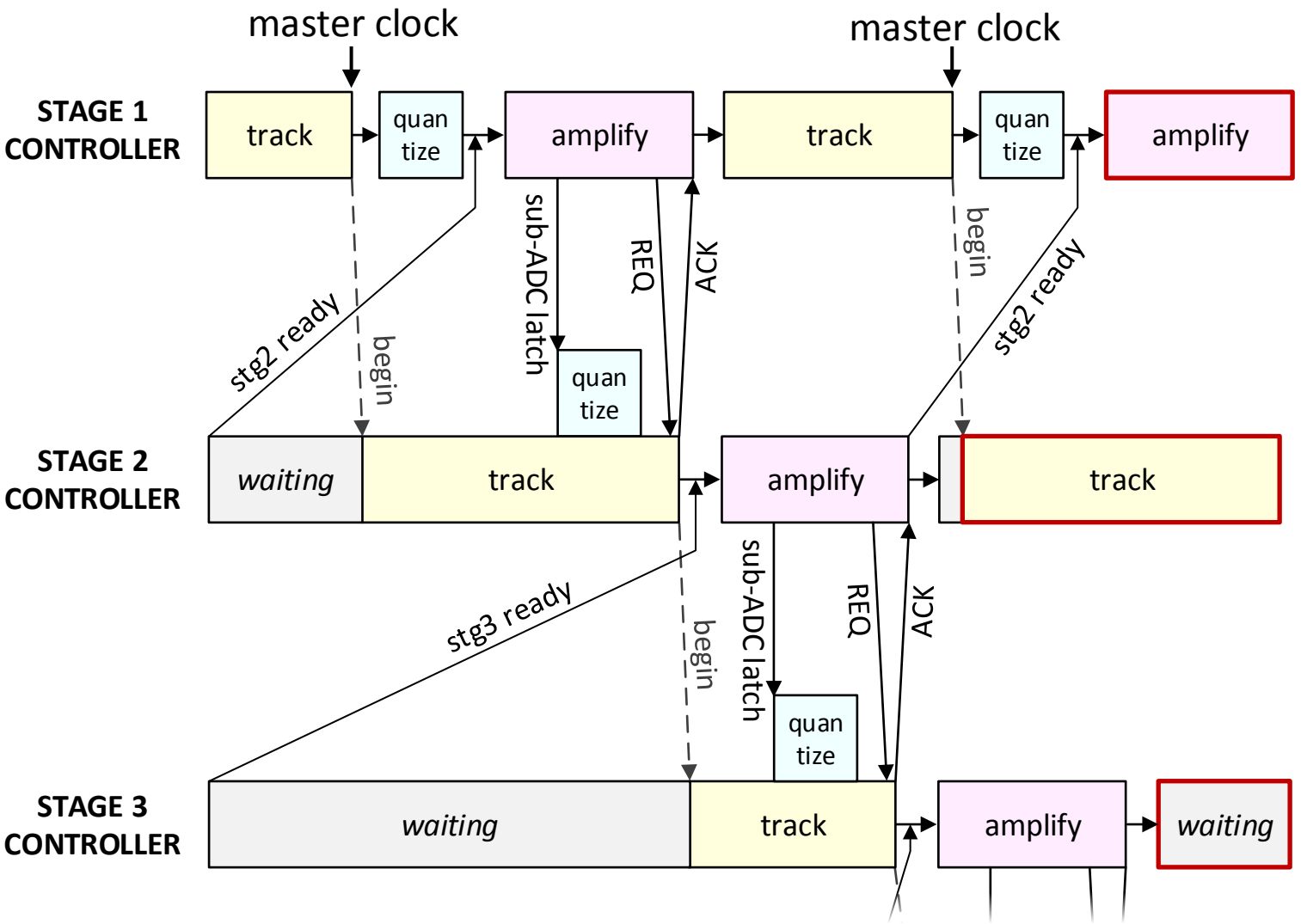
EVENT-DRIVEN TIMING CONTROL



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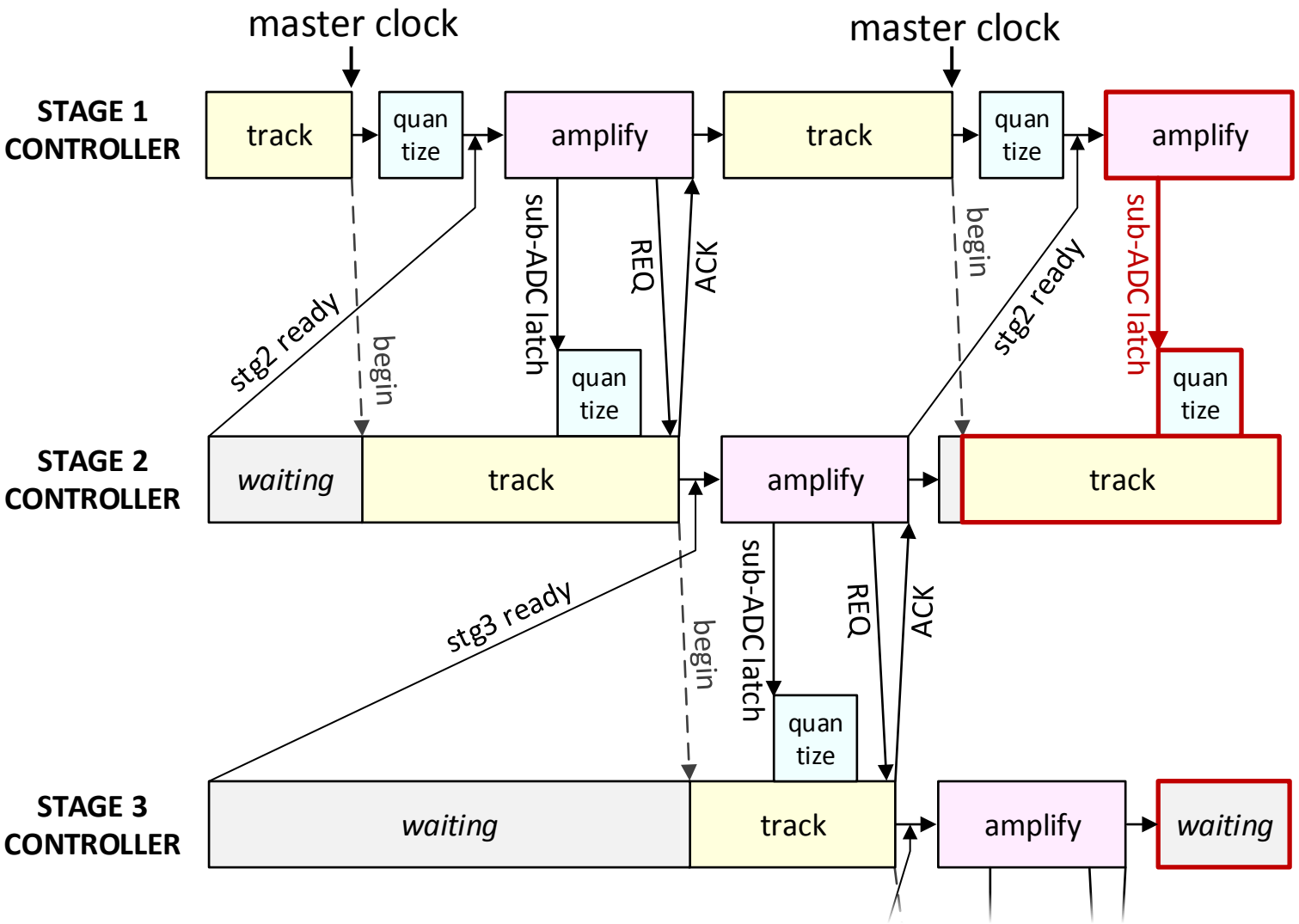
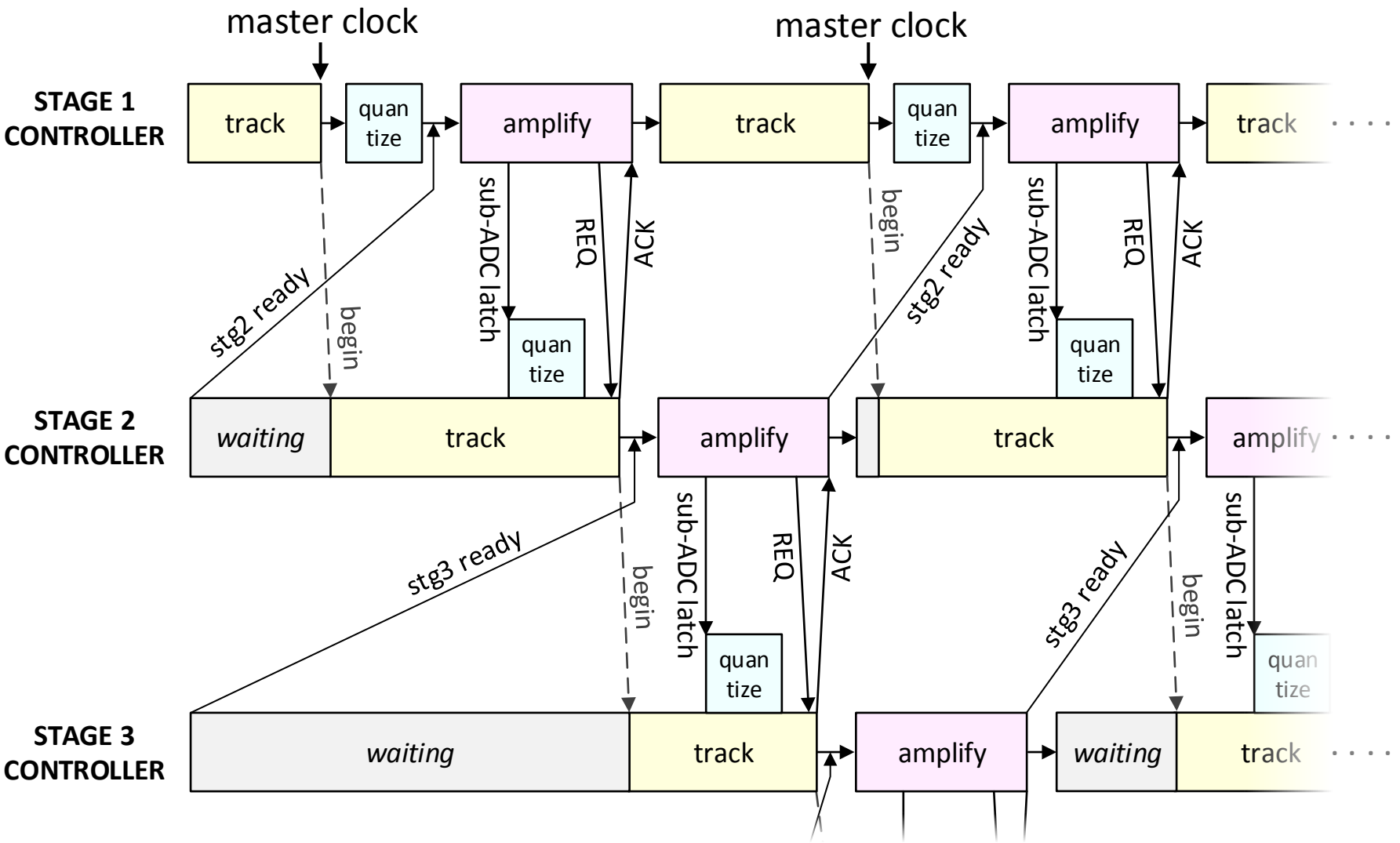


EVENT-DRIVEN TIMING CONTROL



- And so on...

CORRECT-BY-CONSTRUCTION

EVENT-DRIVEN TIMING

- BENEFIT: Event-driven control is correct-by-construction
  - Delay immune
  - Parasitic/loading immune
  - Skew immune

- But, the state machines must be correctly designed!

ANALOG-BASED EVENT TRIGGERS

TYPES OF TRIGGERS

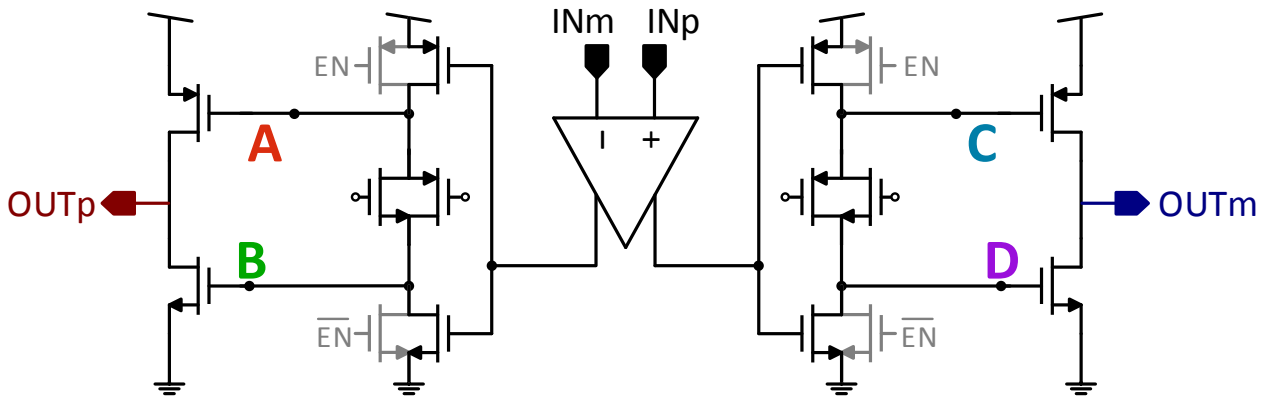
EVENT-DRIVEN TIMING

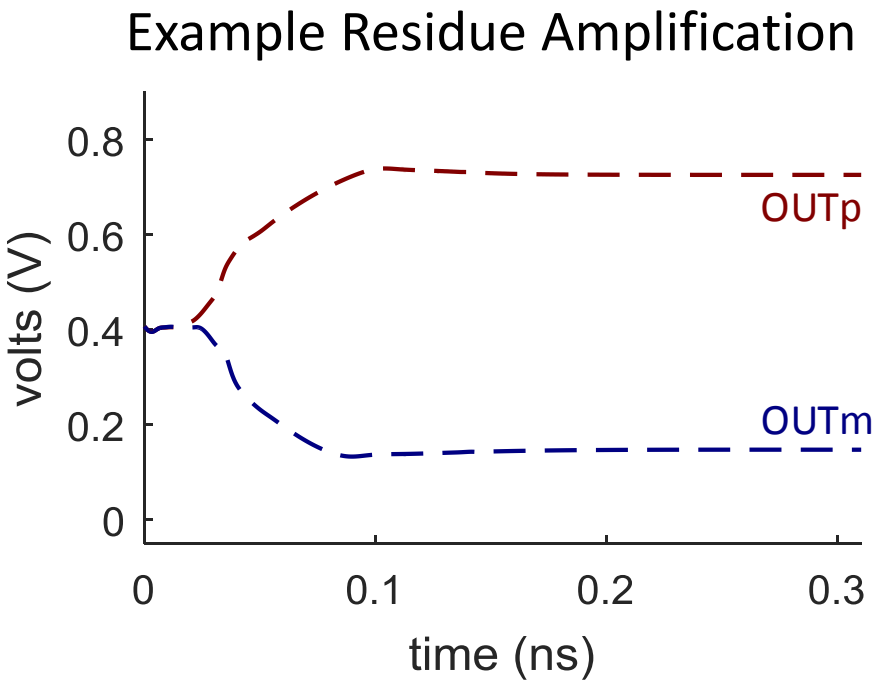
- Event triggers can be generated from:
  - Delay cells
  - Analog events
  - Combination of both

- Example analog trigger: detect when ringamp is done slewing

SLEW-DONE DETECTION

EVENT-DRIVEN CONTROL

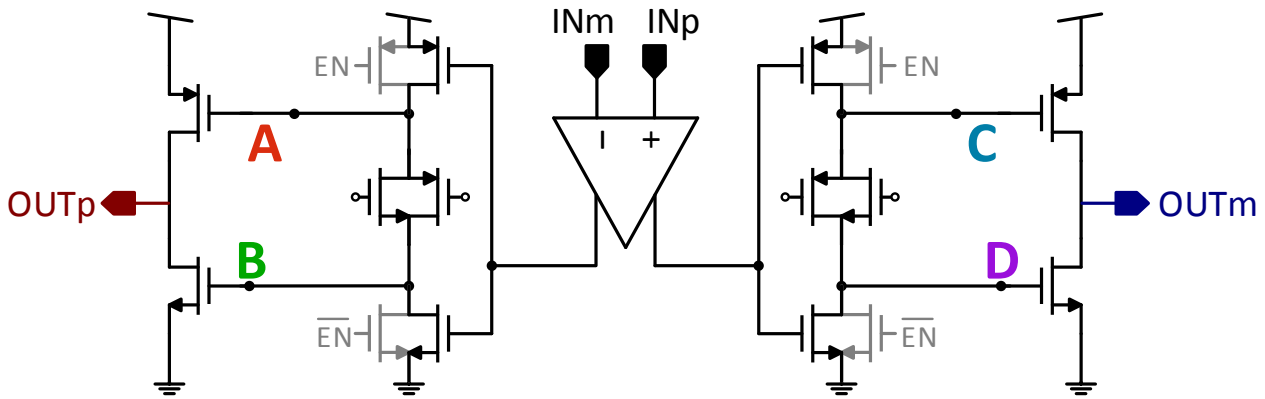


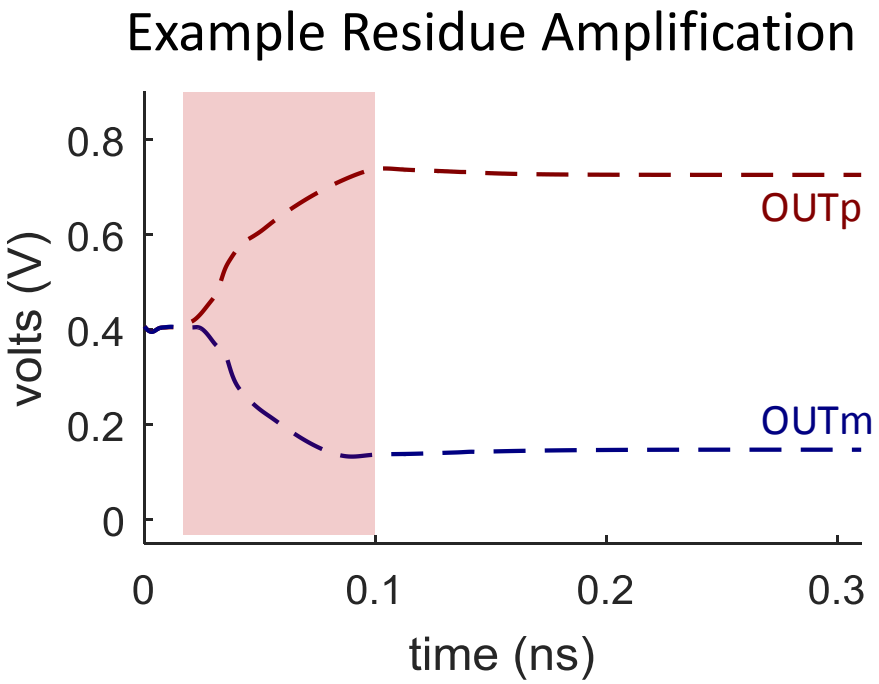


- 3 phases of operation

SLEW-DONE DETECTION

EVENT-DRIVEN CONTROL

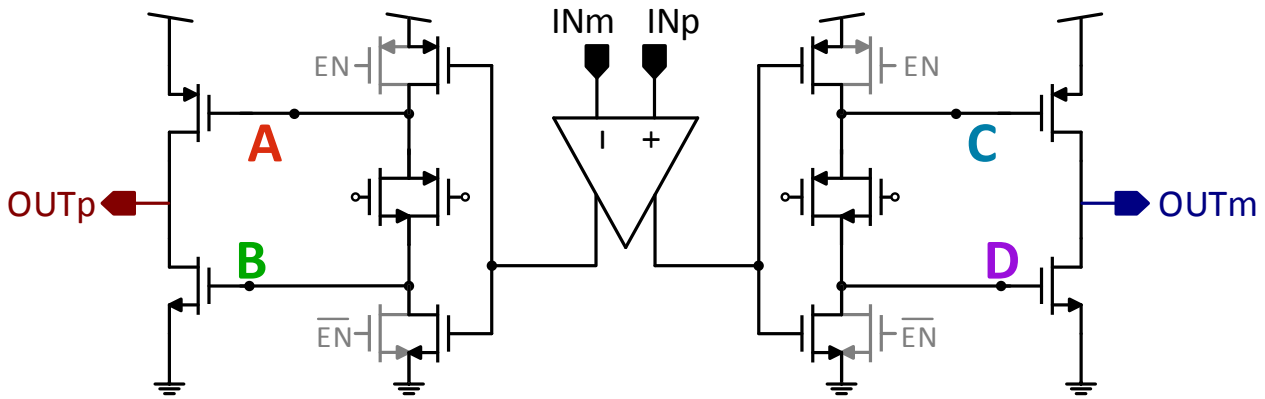


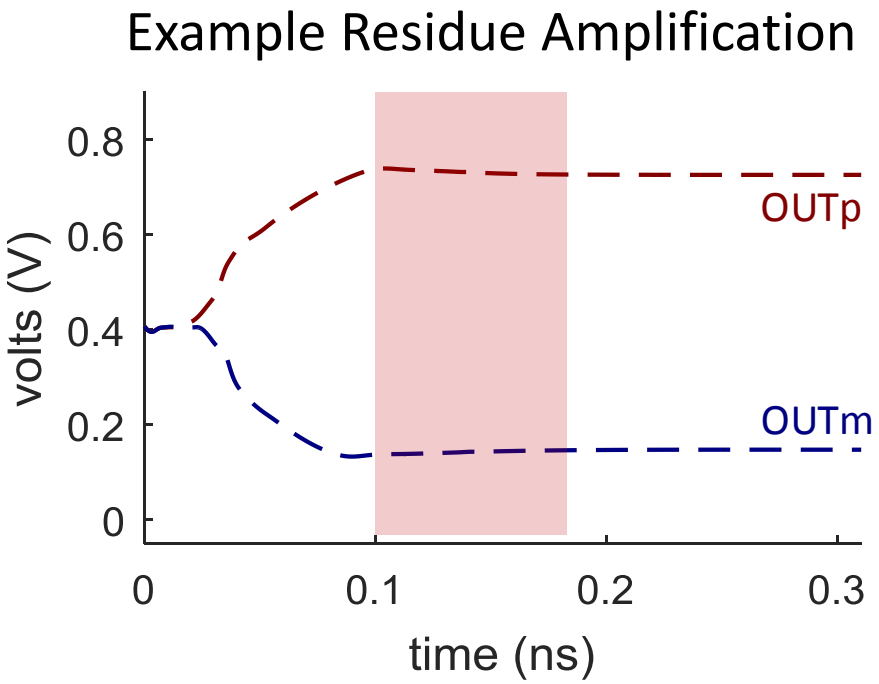


- 3 phases of operation
  1. Slewing

SLEW-DONE DETECTION

EVENT-DRIVEN CONTROL

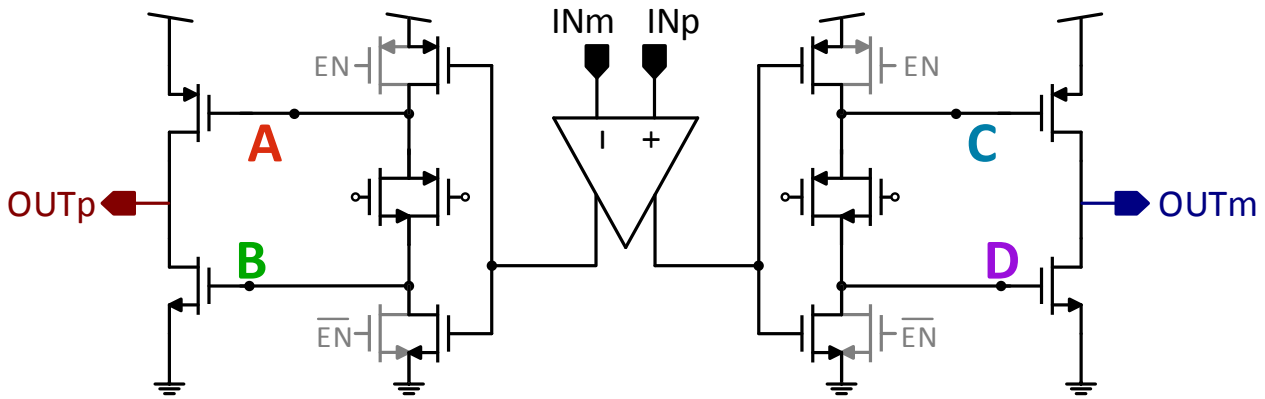


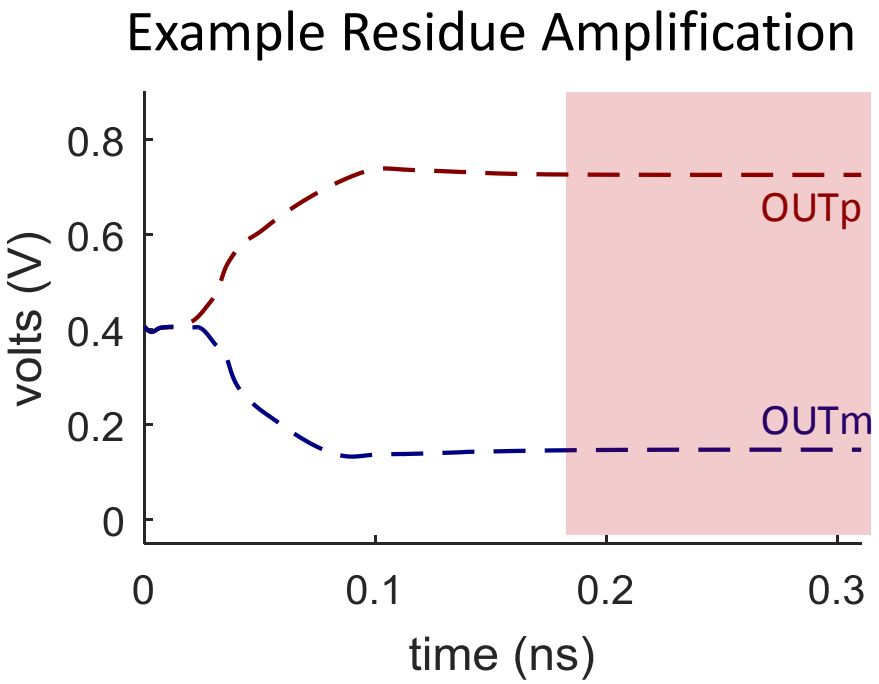


- 3 phases of operation
  1. Slewing
  2. Stabilization

SLEW-DONE DETECTION

EVENT-DRIVEN CONTROL

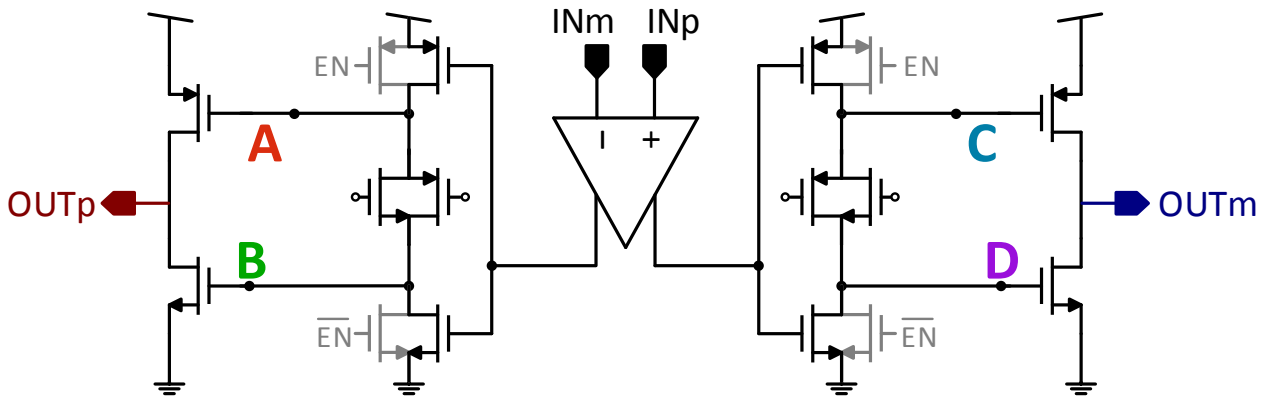




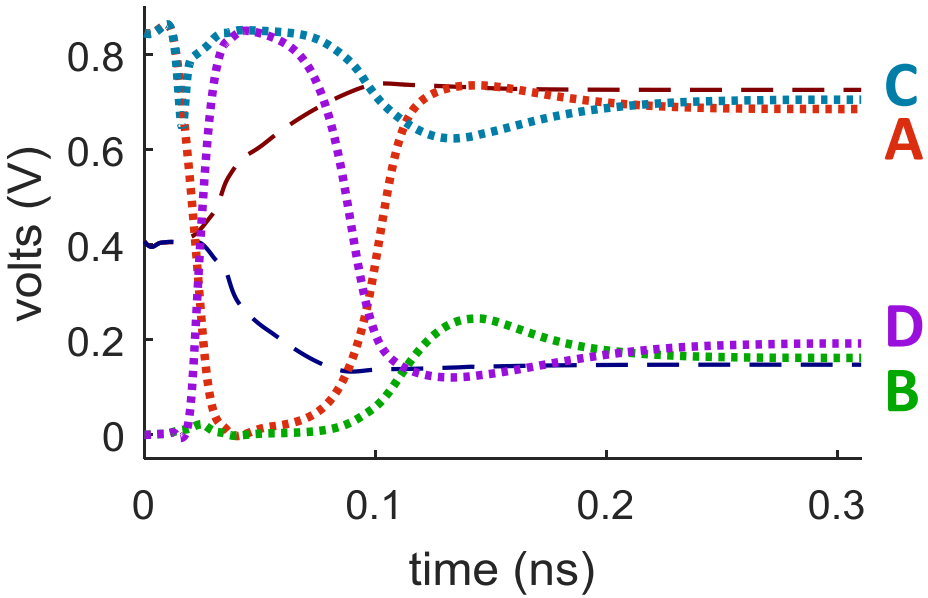
- 3 phases of operation
  1. Slewing
  2. Stabilization
  3. Settling

SLEW-DONE DETECTION

EVENT-DRIVEN CONTROL



Example Residue Amplification

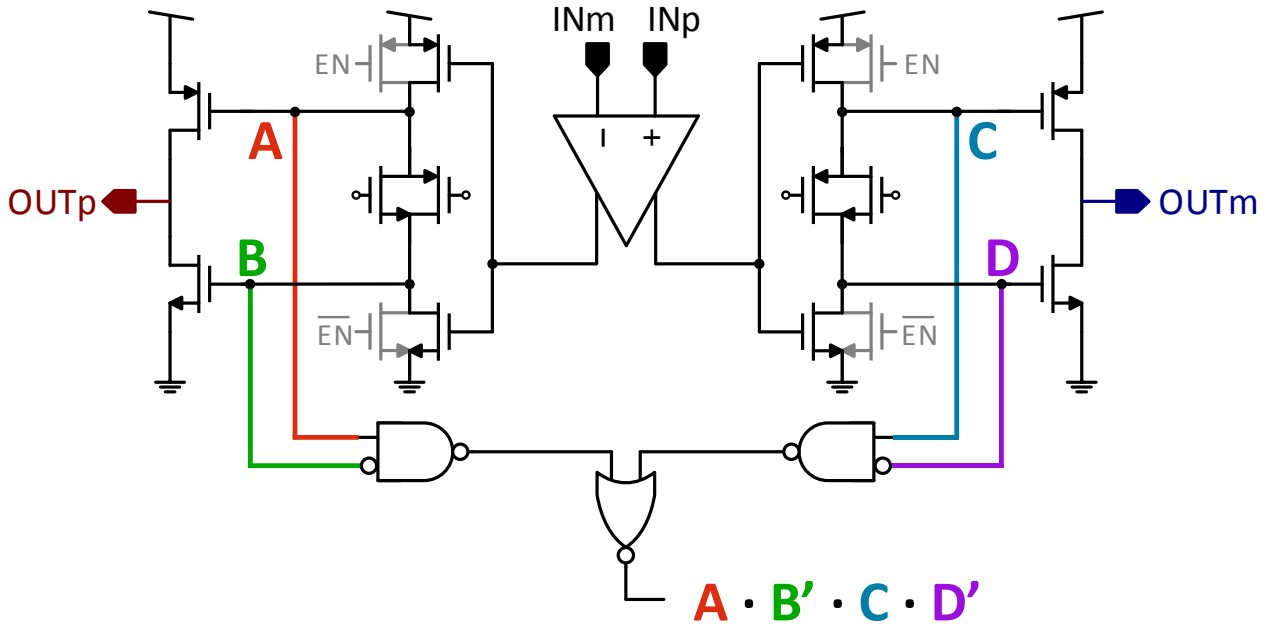


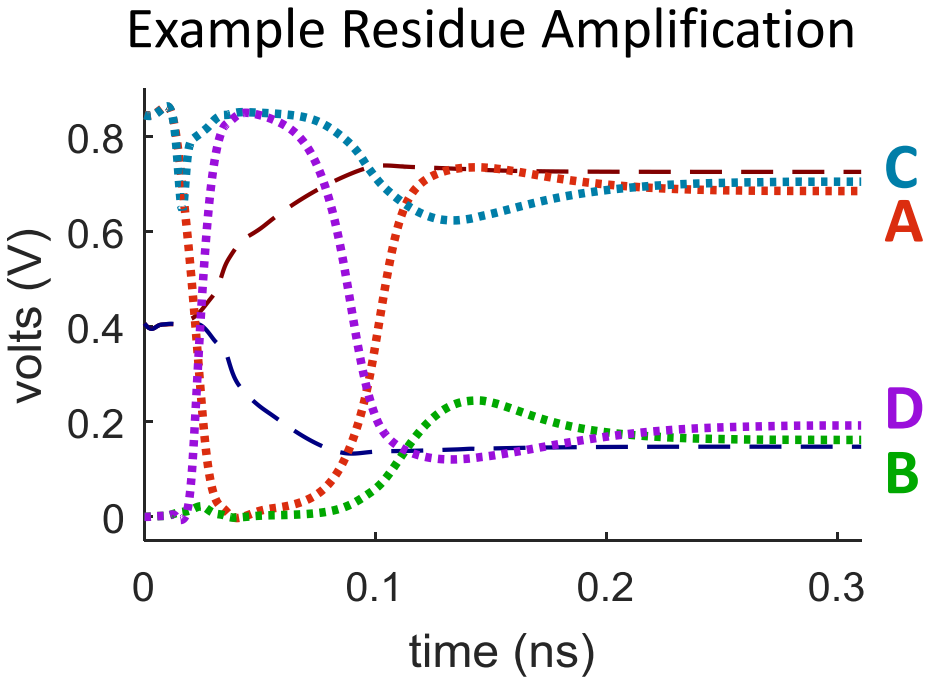
- Stabilization forces A,C high and B,D low

- Thus, fine settling begins when: $A \cdot B' \cdot C \cdot D' = 1$

SLEW-DONE DETECTION

EVENT-DRIVEN CONTROL

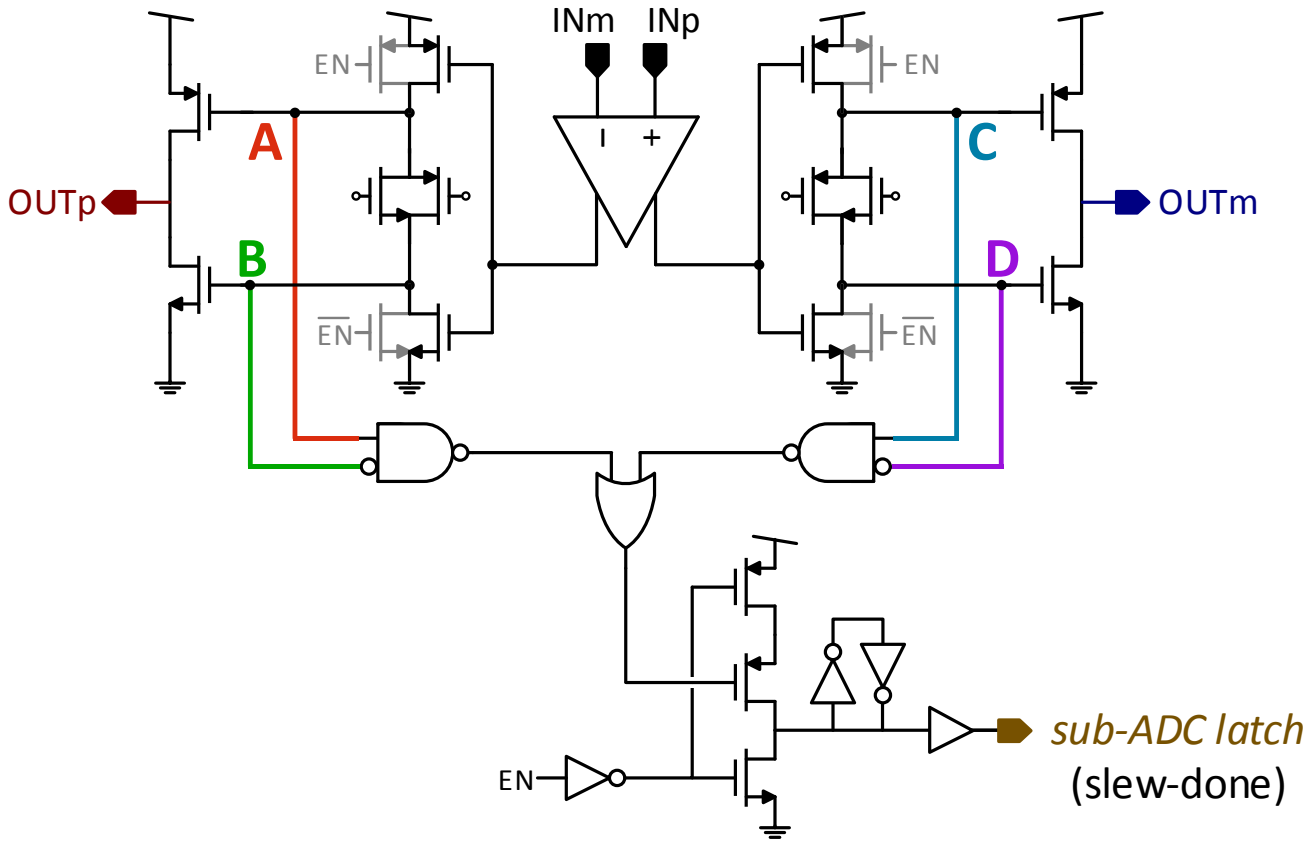




- Simple sensor using logic gates
  - Minimal loading of internal nodes

SLEW-DONE DETECTION

EVENT-DRIVEN CONTROL



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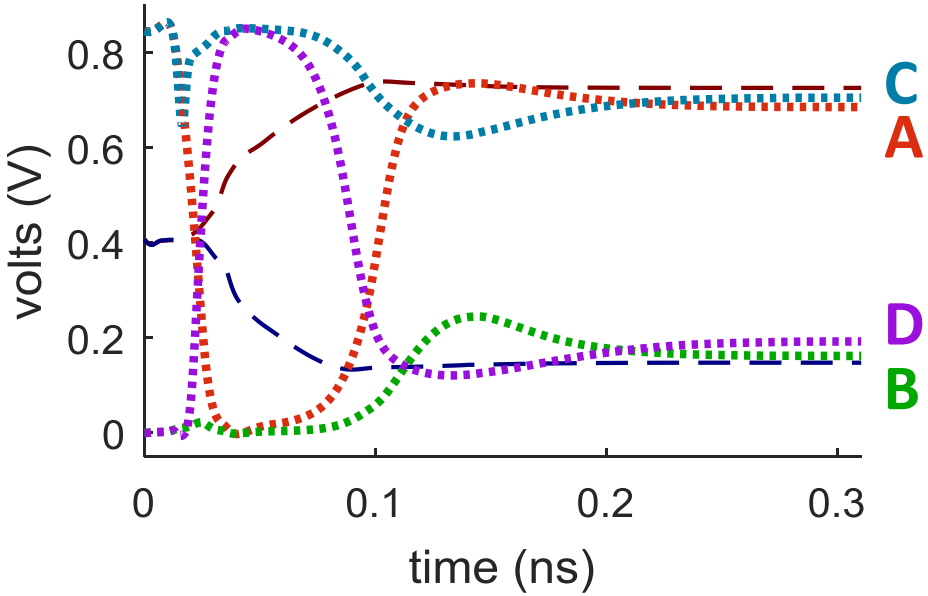
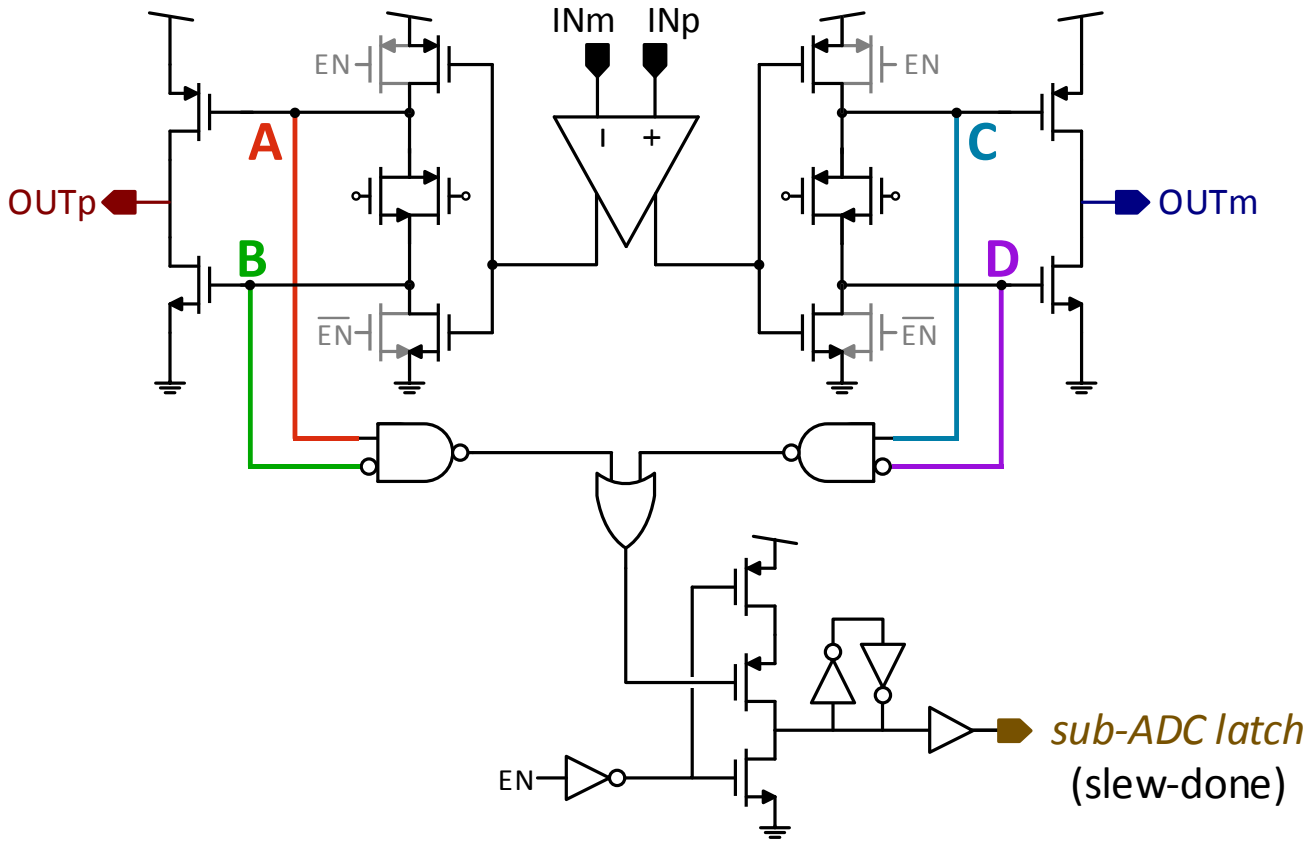


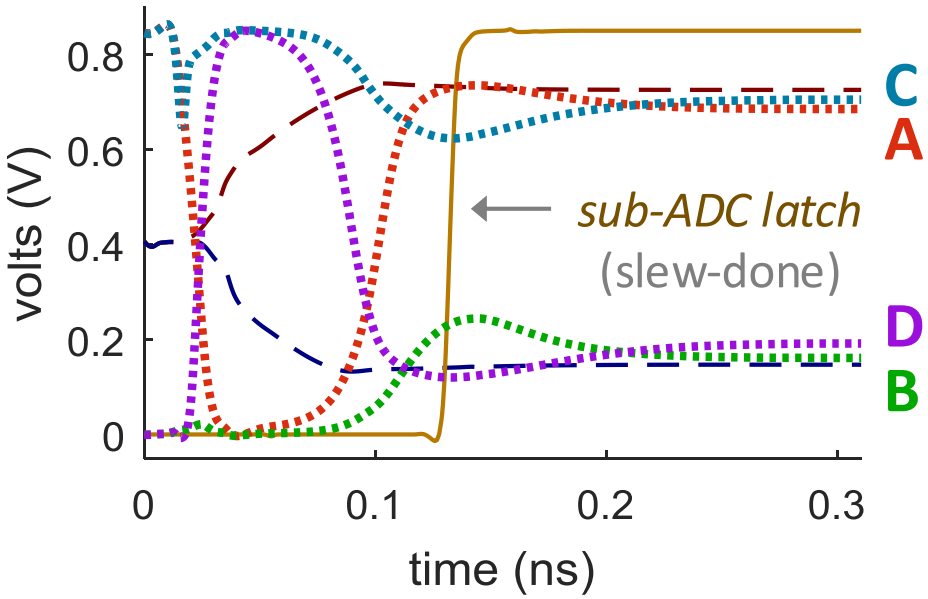
- Dynamic latch grabs *first* detection event

SLEW-DONE DETECTION

EVENT-DRIVEN CONTROL



Example Residue Amplification

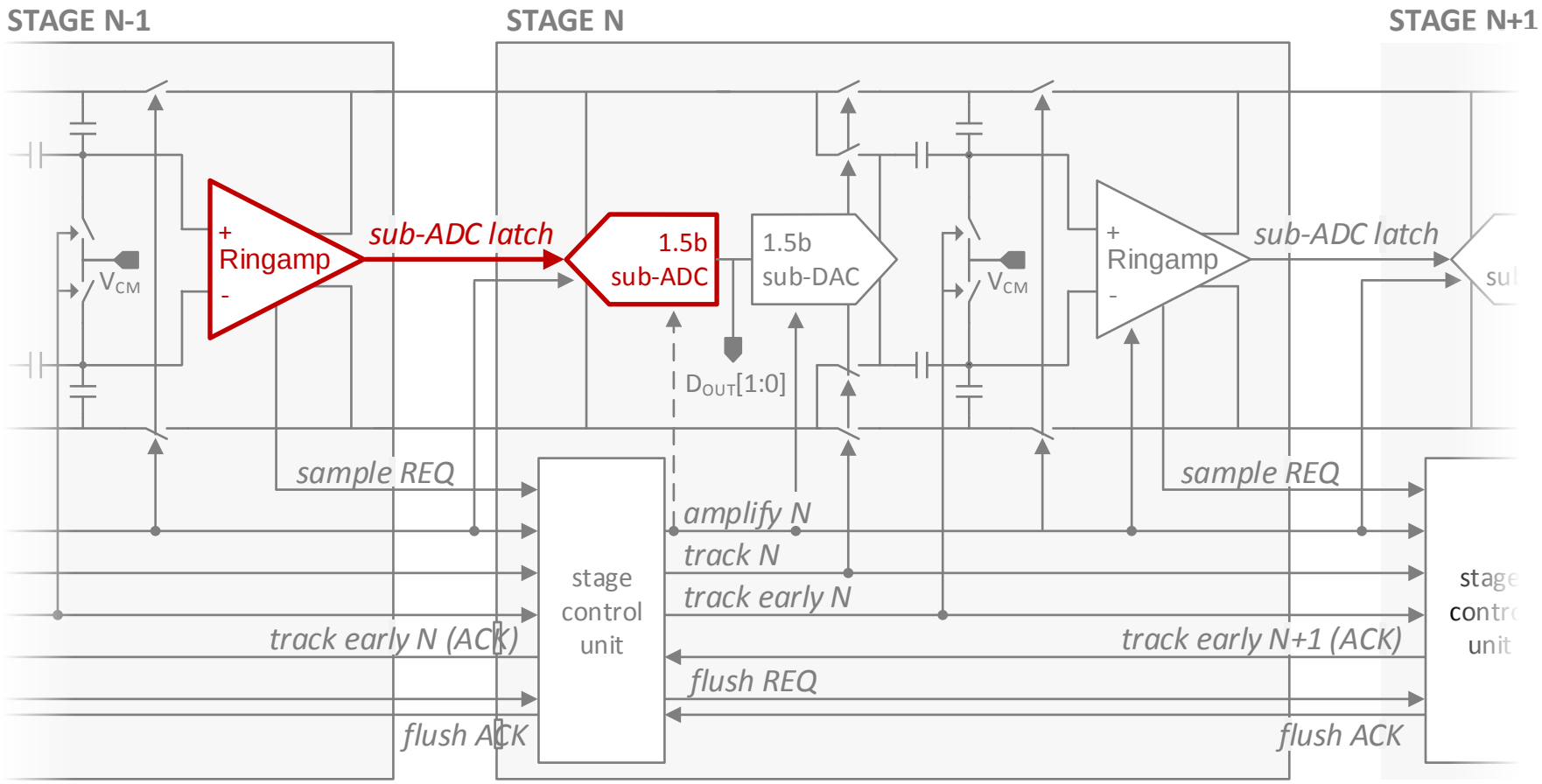


- Dynamic latch grabs *first* detection event

EARLY QUANTIZATION

CONCEPT

- Slew-done is the perfect time for early quantization
  - Accurate enough
  - Doesn't disrupt fine settling



CHALLENGES

DEADLOCK DETECTION & RESOLUTION

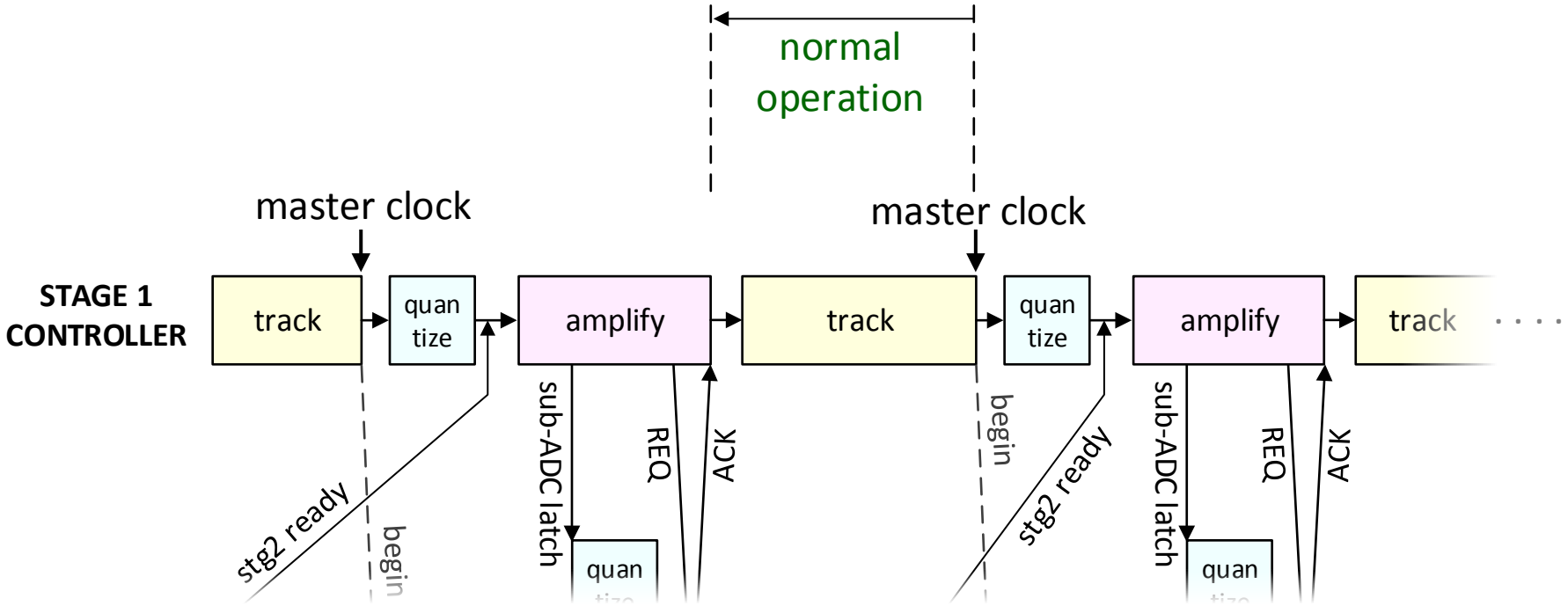
EVENT-DRIVEN TIMING

- Triggering on analog events requires correct analog operation
  - Not always the case
  - E.g. ringamp CMFB startup
    - Output saturates
    - *“slew done”* never detected

- Key Observation: any deadlock will eventually propagate to the front
  - Detect & force reset

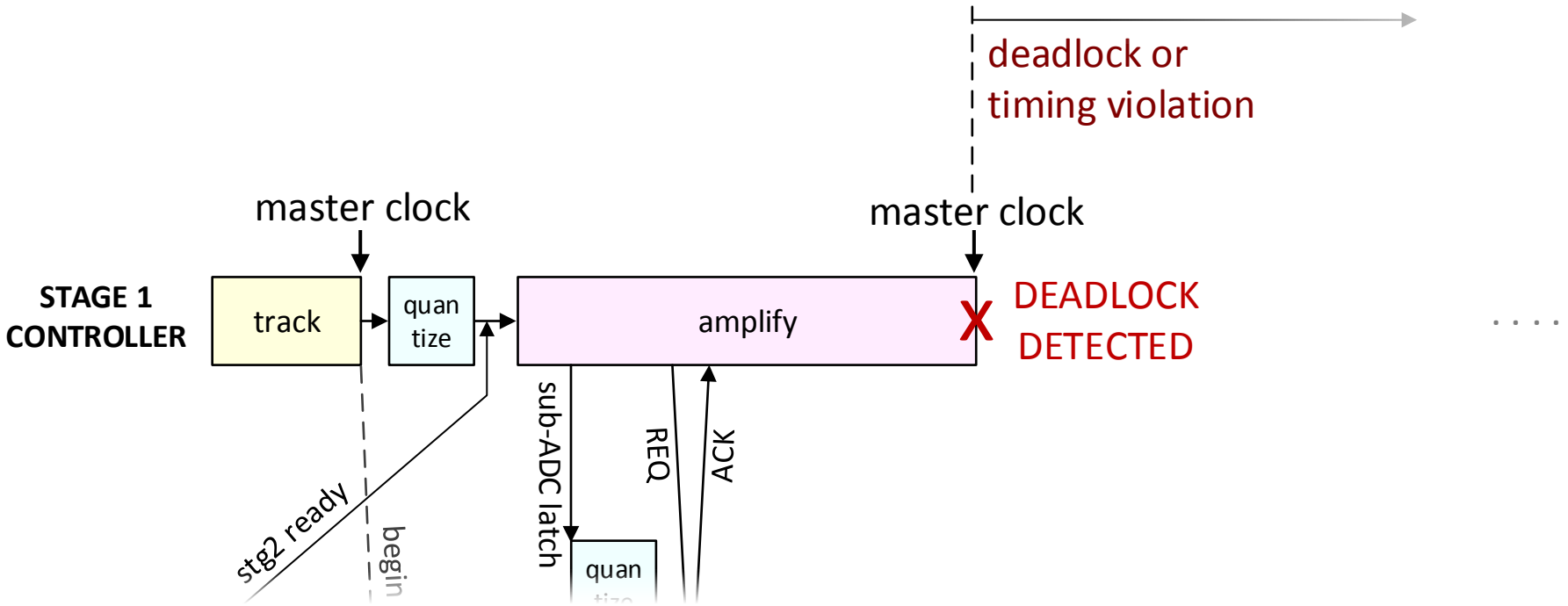
DEADLOCK DETECTION & RESOLUTION

EVENT-DRIVEN TIMING



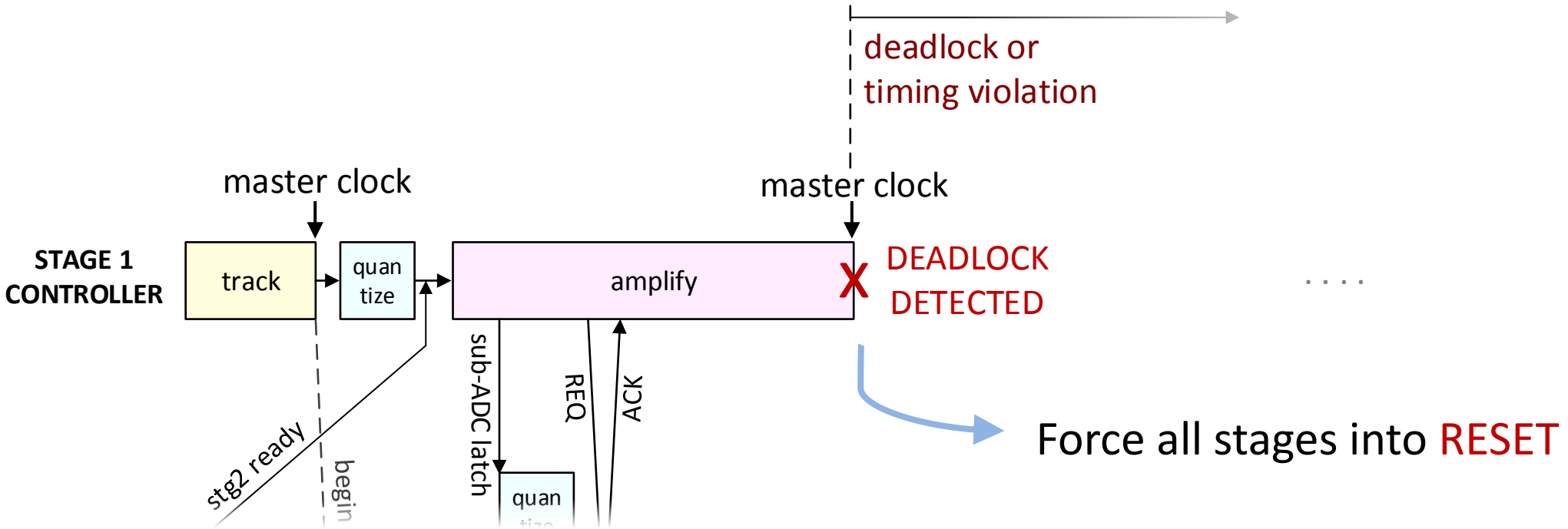
DEADLOCK DETECTION & RESOLUTION

EVENT-DRIVEN TIMING



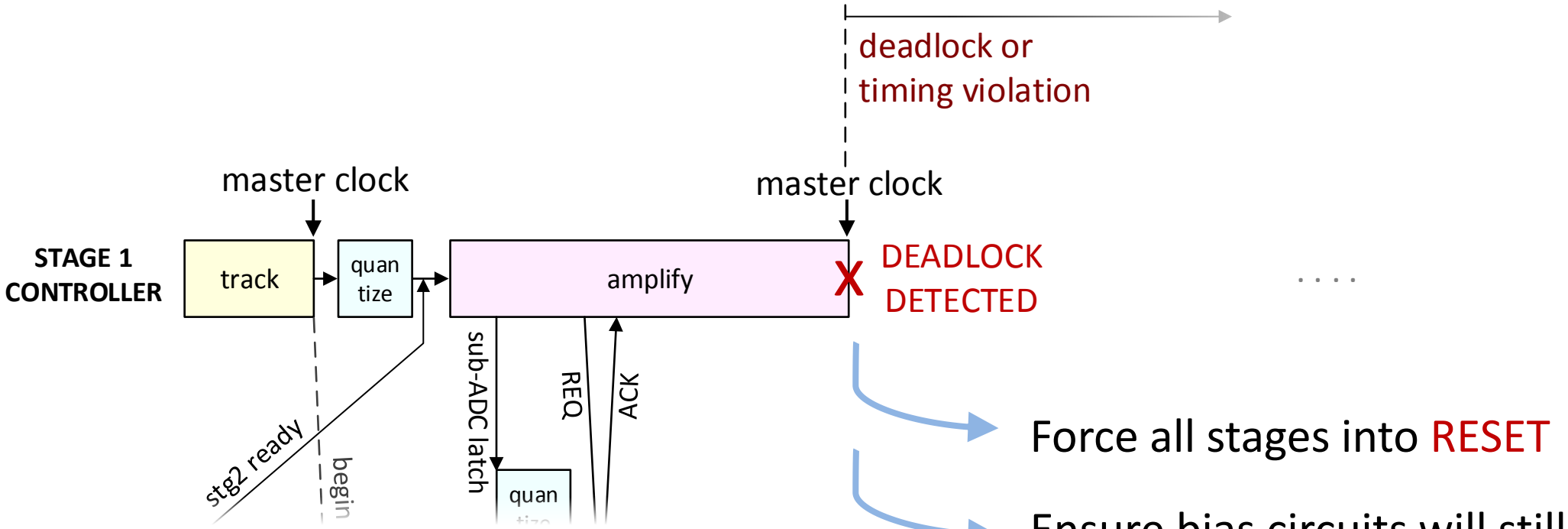
DEADLOCK DETECTION & RESOLUTION

EVENT-DRIVEN TIMING



DEADLOCK DETECTION & RESOLUTION

EVENT-DRIVEN TIMING



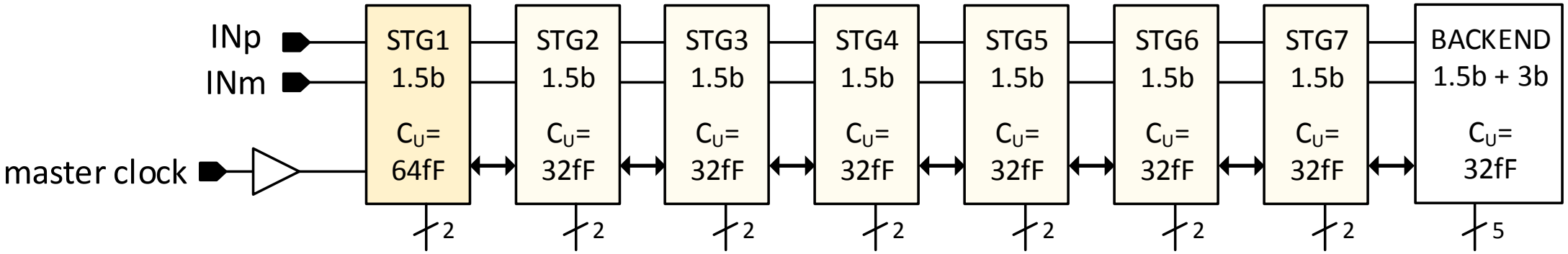
Force all stages into RESET

Ensure bias circuits will still converge after repeated resets (e.g. CMFB)

RE-SYNCHRONIZATION OF DIGITAL OUTPUT

EVENT-DRIVEN TIMING

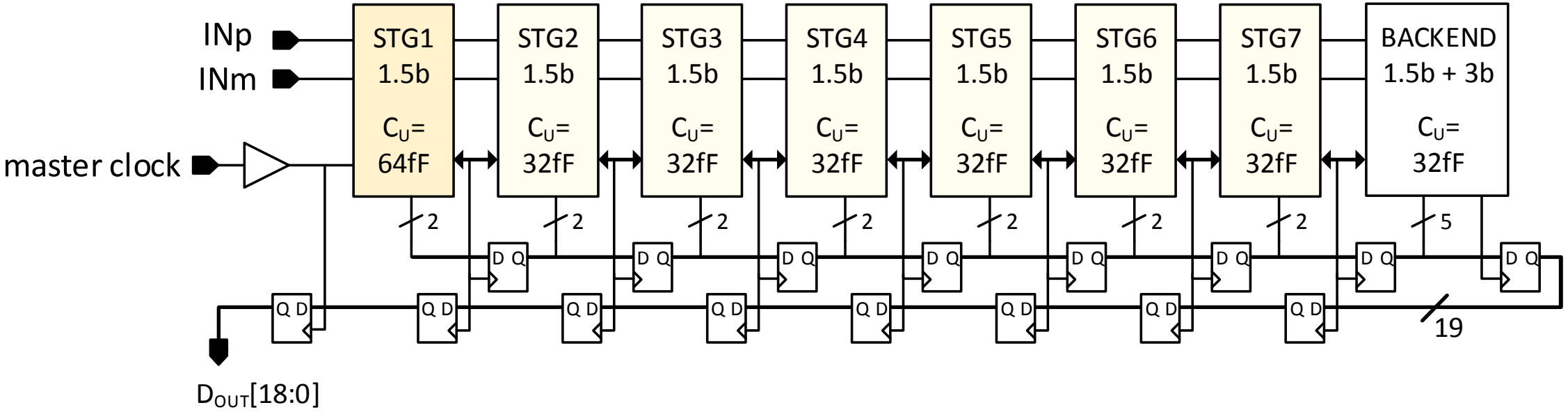
- Digital outputs exit pipeline asynchronously



RE-SYNCHRONIZATION OF DIGITAL OUTPUT

EVENT-DRIVEN TIMING

- Causal relation between signals used to shift data:
  1. Down to the end for alignment
  2. Back to the front for synchronization



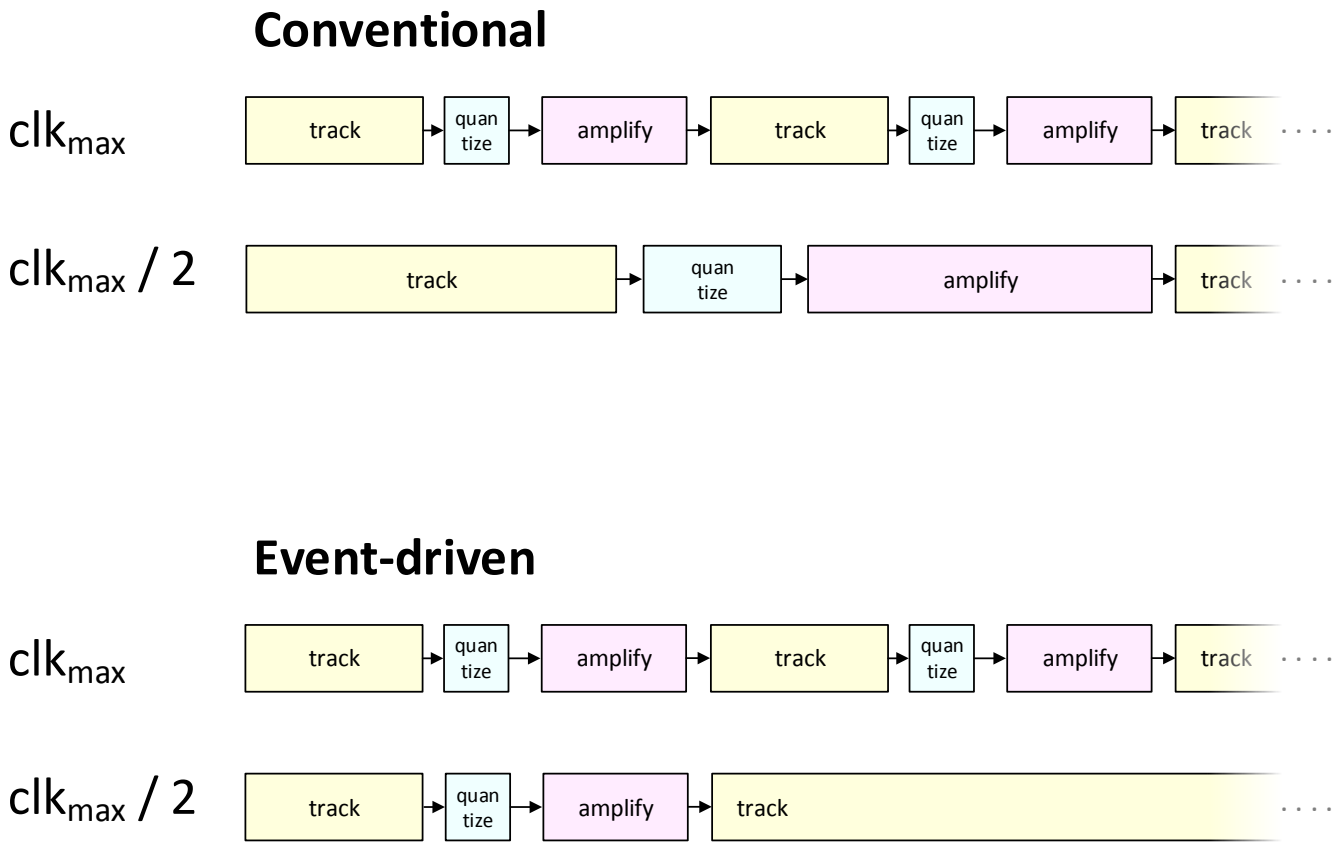
BENEFITS OF CONSTANT INTERNAL SPEED

CONSTANT INTERNAL SPEED

OBSERVATION

- Internal processing behavior is independent of clock rate
  - 6 MS/s same as 600 MS/s

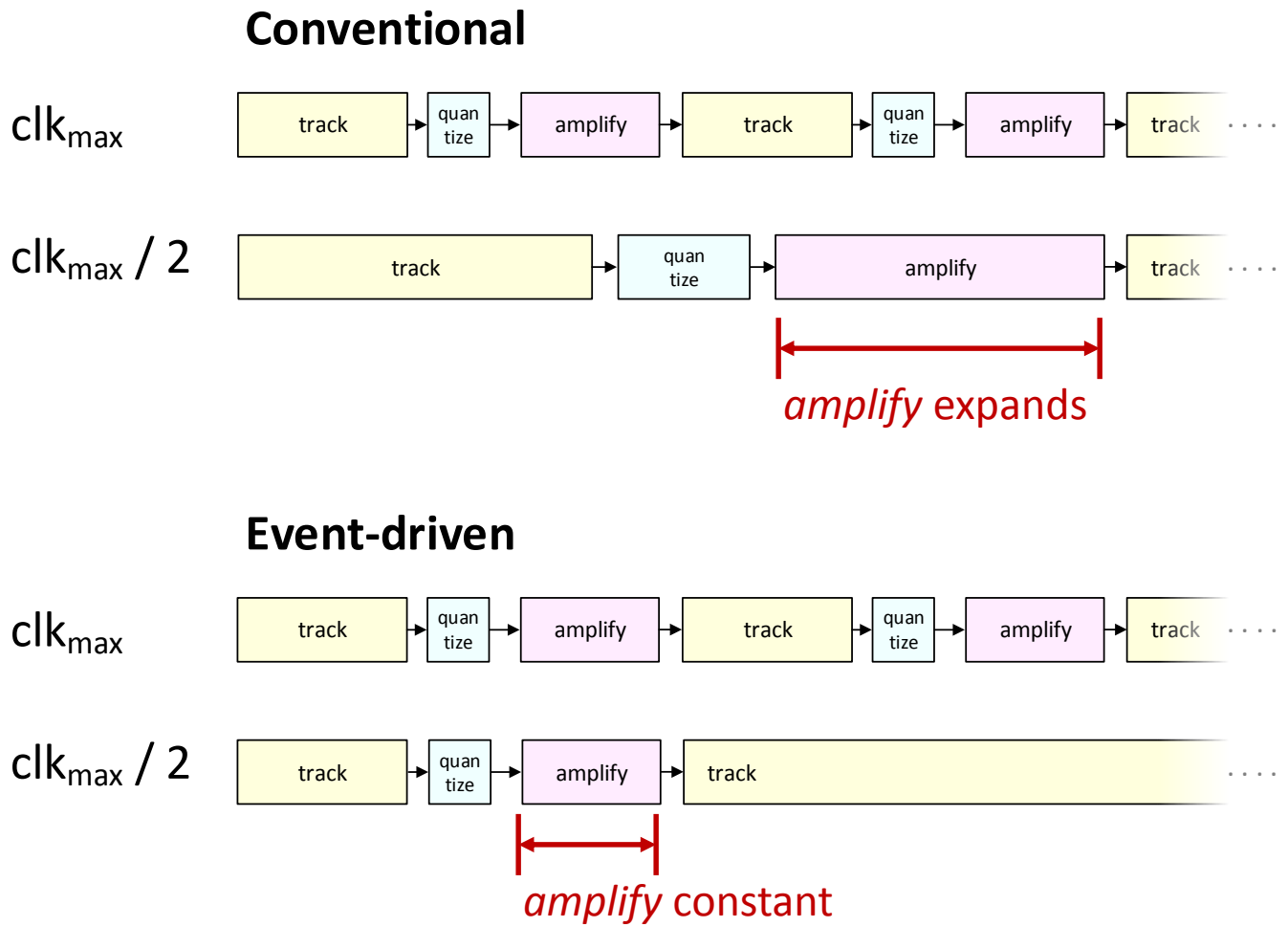
- Several related advantages



CONSTANT INTERNAL SPEED

ADVANTAGES

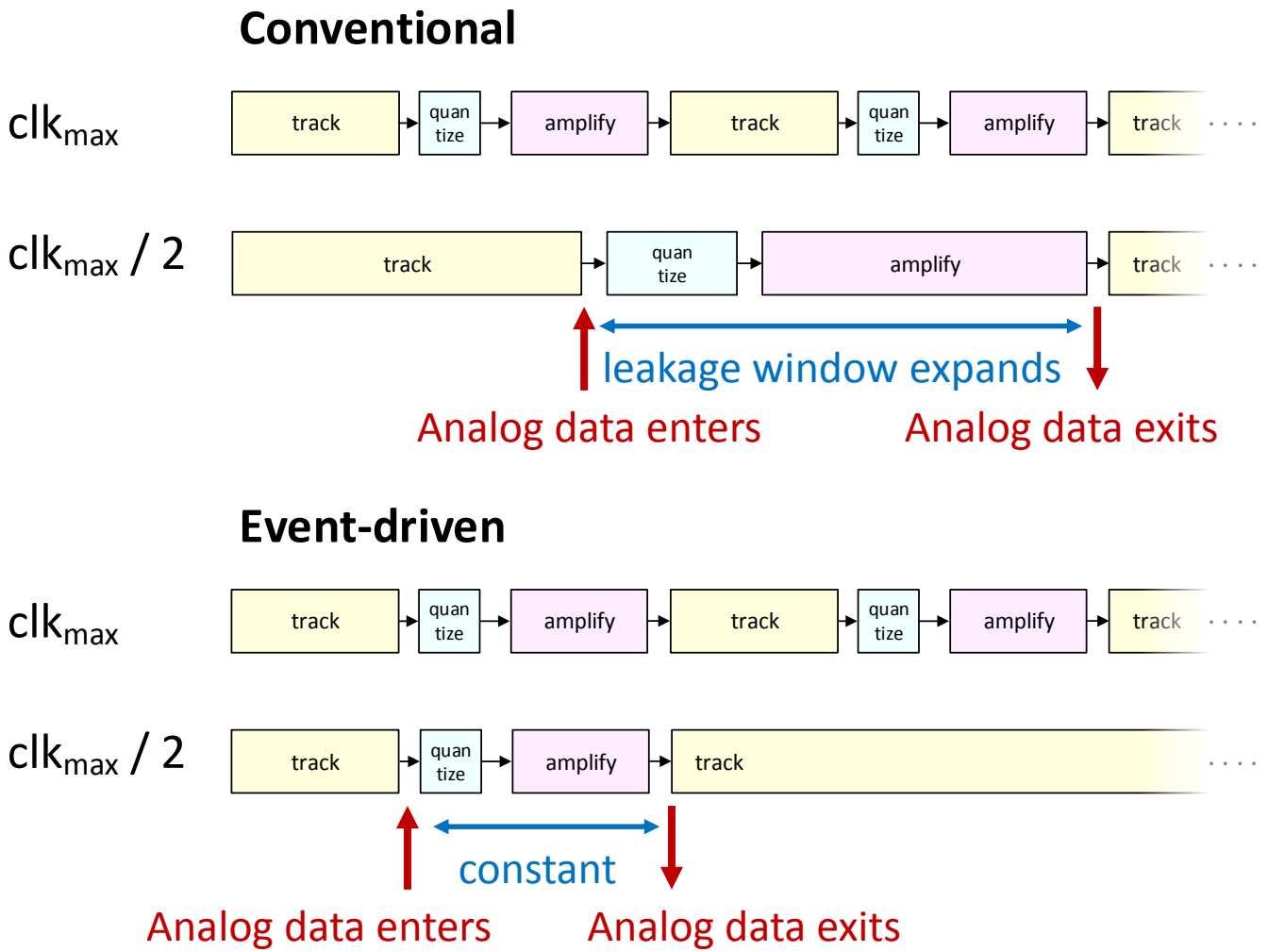
- BENEFIT: Linear scaling of power w.r.t. clock
  - When combined with ringamp power-down



CONSTANT INTERNAL SPEED

ADVANTAGES

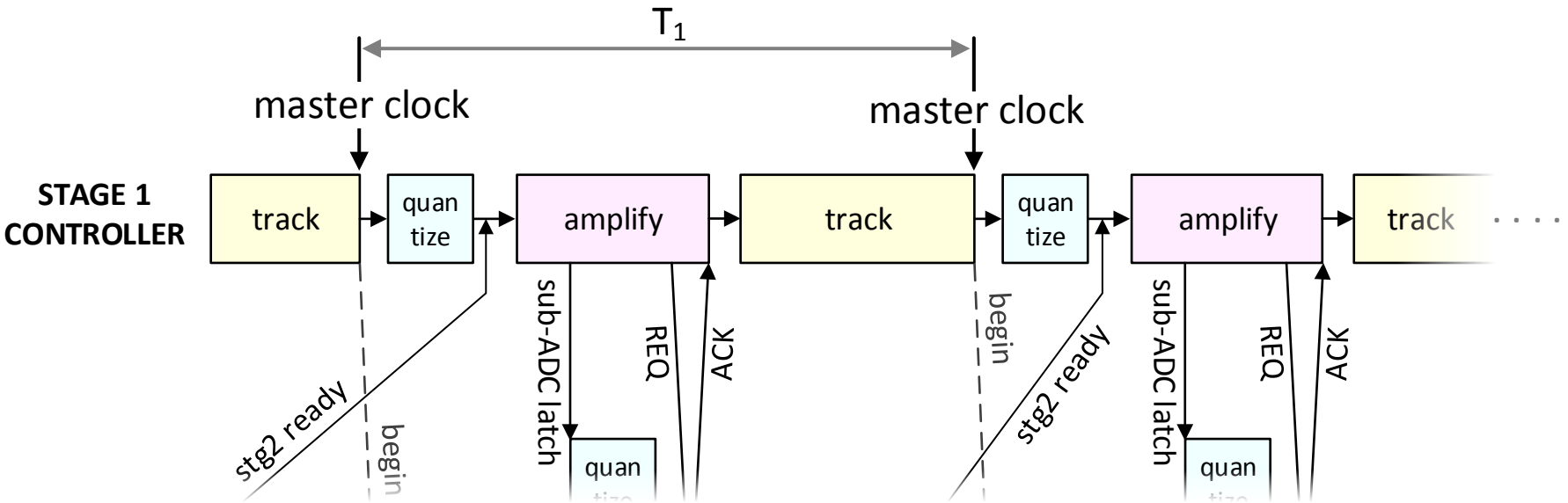
- BENEFIT: Eliminates critical leakage-window constraints
  - E.g. MDAC switches
  - Optimize for *highest* speed of operation



CONSTANT INTERNAL SPEED

ADVANTAGES

- BENEFIT: Automatically maximizes input signal track time



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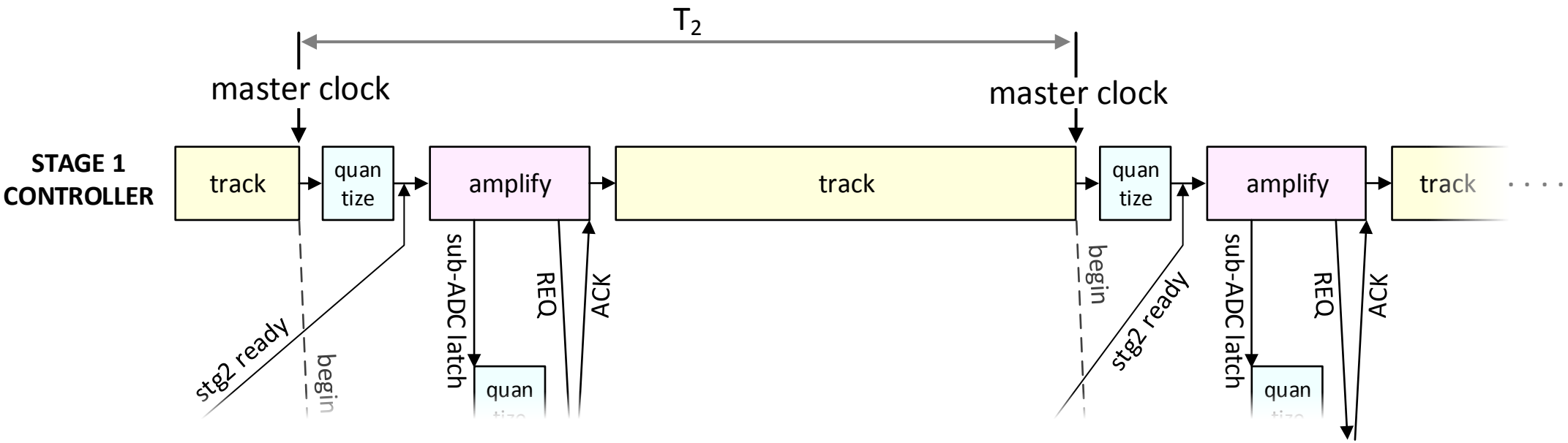
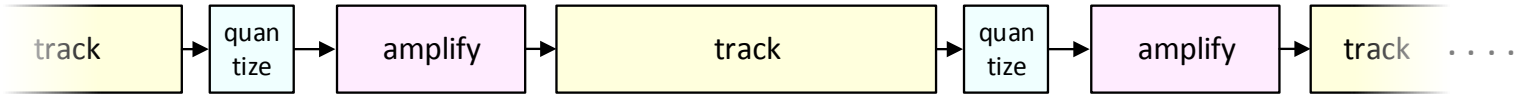


CONSTANT INTERNAL SPEED

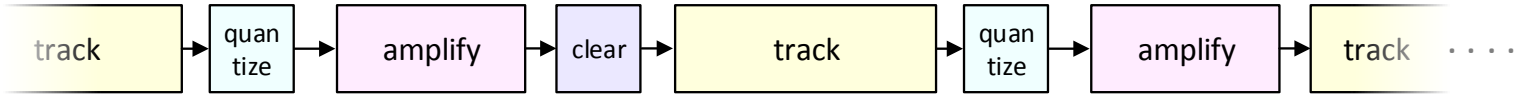
ADVANTAGES

- BENEFIT: Flexible state machine behavior
  - Easily reconfigured
  - Entire phases added/subtracted
  - Special calibration modes

Pre-clearing off:



Pre-clearing on:



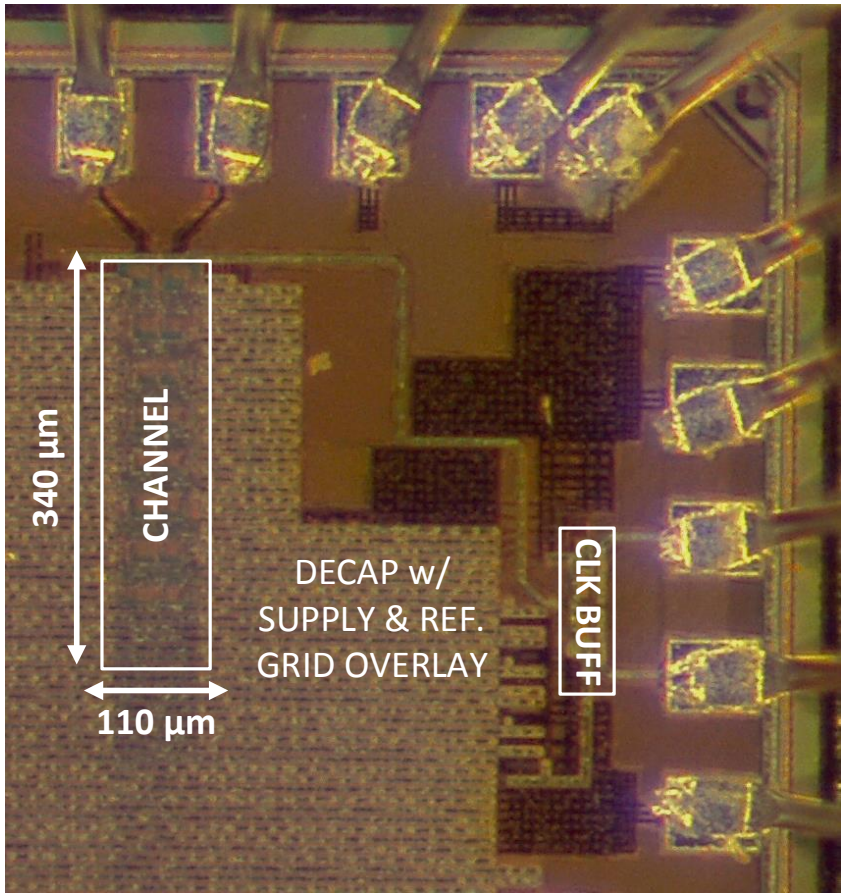
MEASURED PERFORMANCE

IMPLEMENTATION IN 16NM CMOS

MEASURED PERFORMANCE

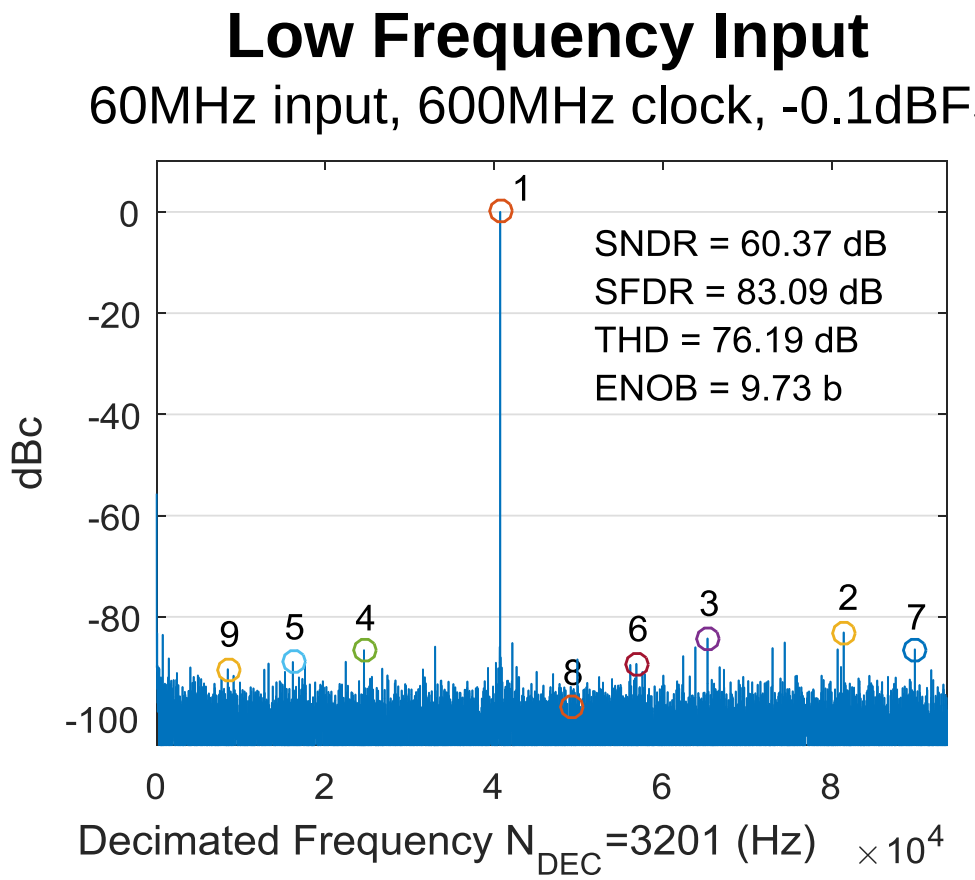
- 0.037mm^2 active area

- Single chip configuration for all measurements reported
  - Digital controls
  - Analog levels



FFT

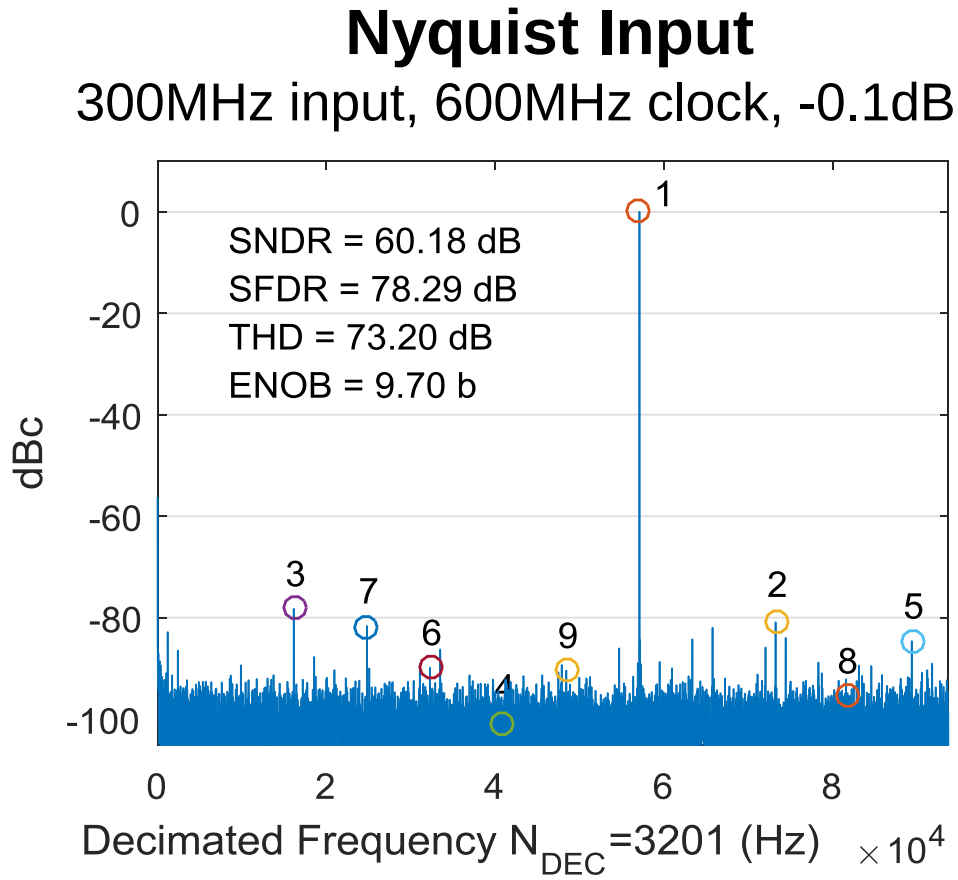
MEASURED PERFORMANCE



- 60.4dB SNDR
- 83.1dB SFDR
- Decimated by 3201

FFT

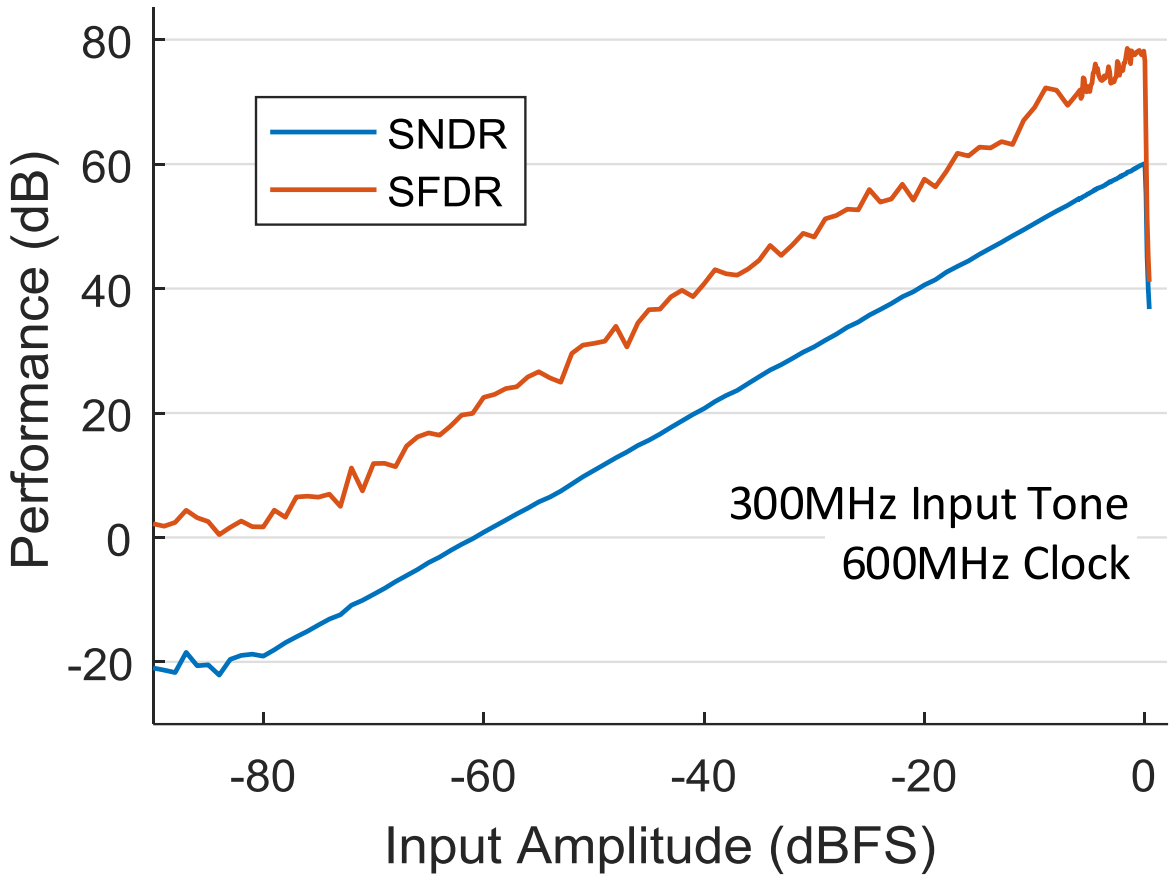
MEASURED PERFORMANCE



- 60.2dB SNDR
- 78.3dB SFDR
- 6.0mW total power

SWEEP: INPUT AMPLITUDE

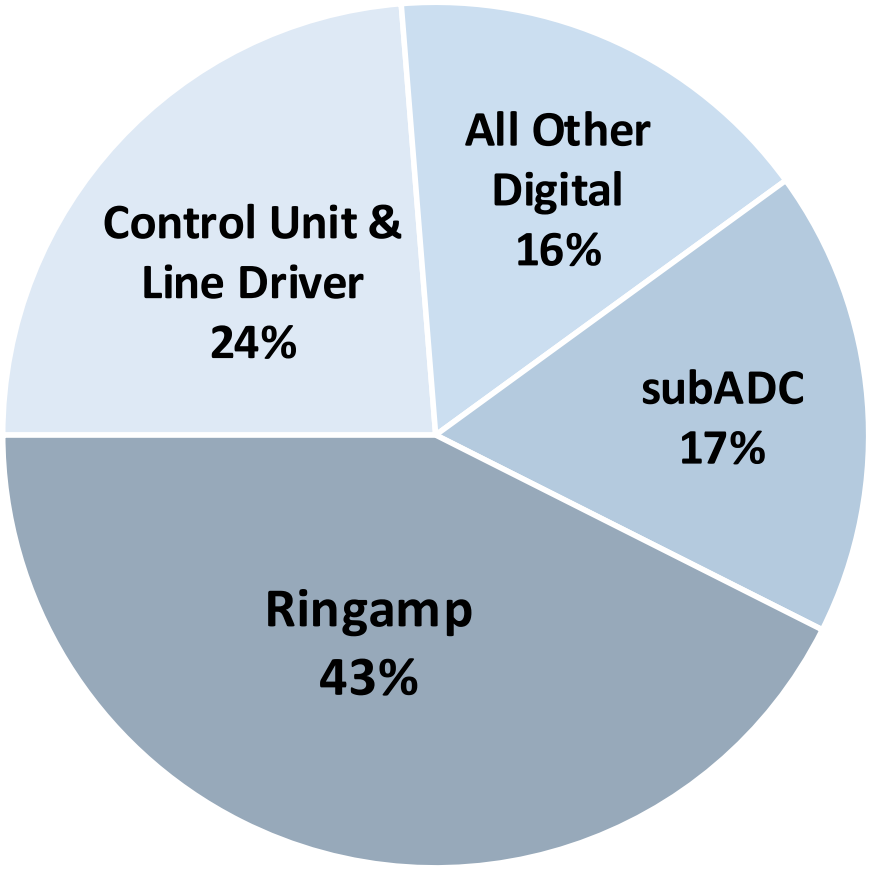
MEASURED PERFORMANCE



- No compression at full-scale
  - Ringamps maintain high linearity even with large output swing
  - Utilize 88% of supply range
    - V_{DD} = 850mV
    - V_{REFP} = 800mV
    - V_{REFM} = 50mV

POWER CONSUMPTION

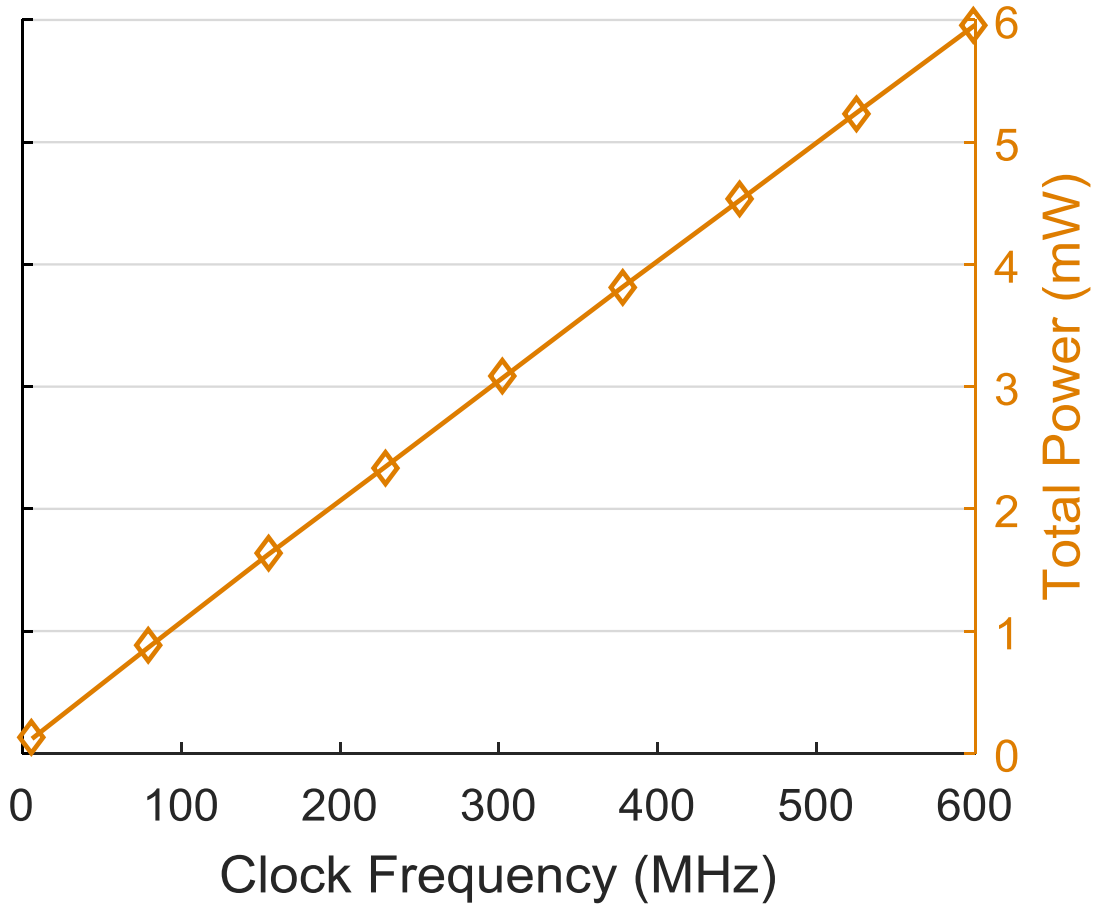
MEASURED PERFORMANCE



- Clock power minimized

SWEEP: CLOCK FREQUENCY

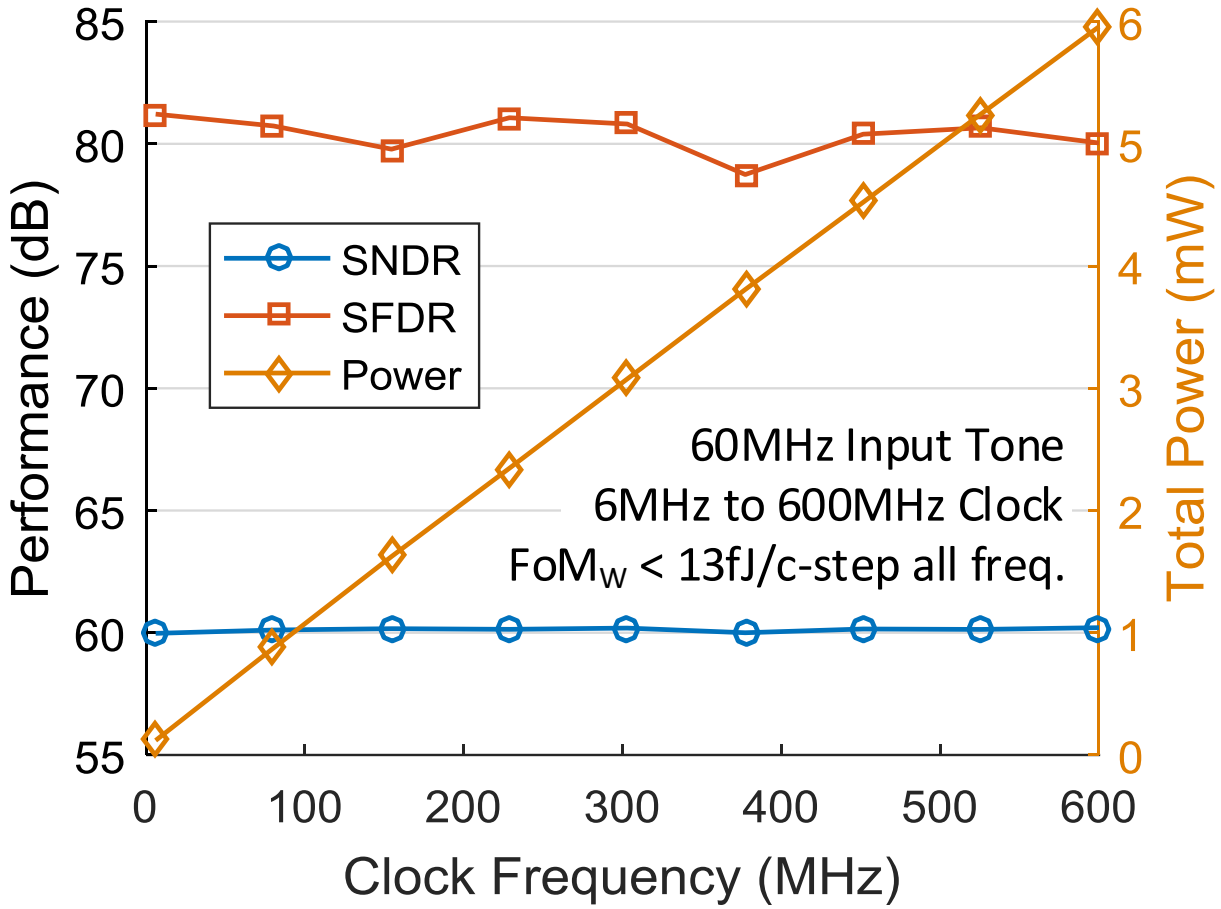
MEASURED PERFORMANCE



- Fully dynamic power consumption
  - Linear scaling w.r.t. clock
- Attractive feature for multi-standard mobile wireless applications

SWEEP: CLOCK FREQUENCY

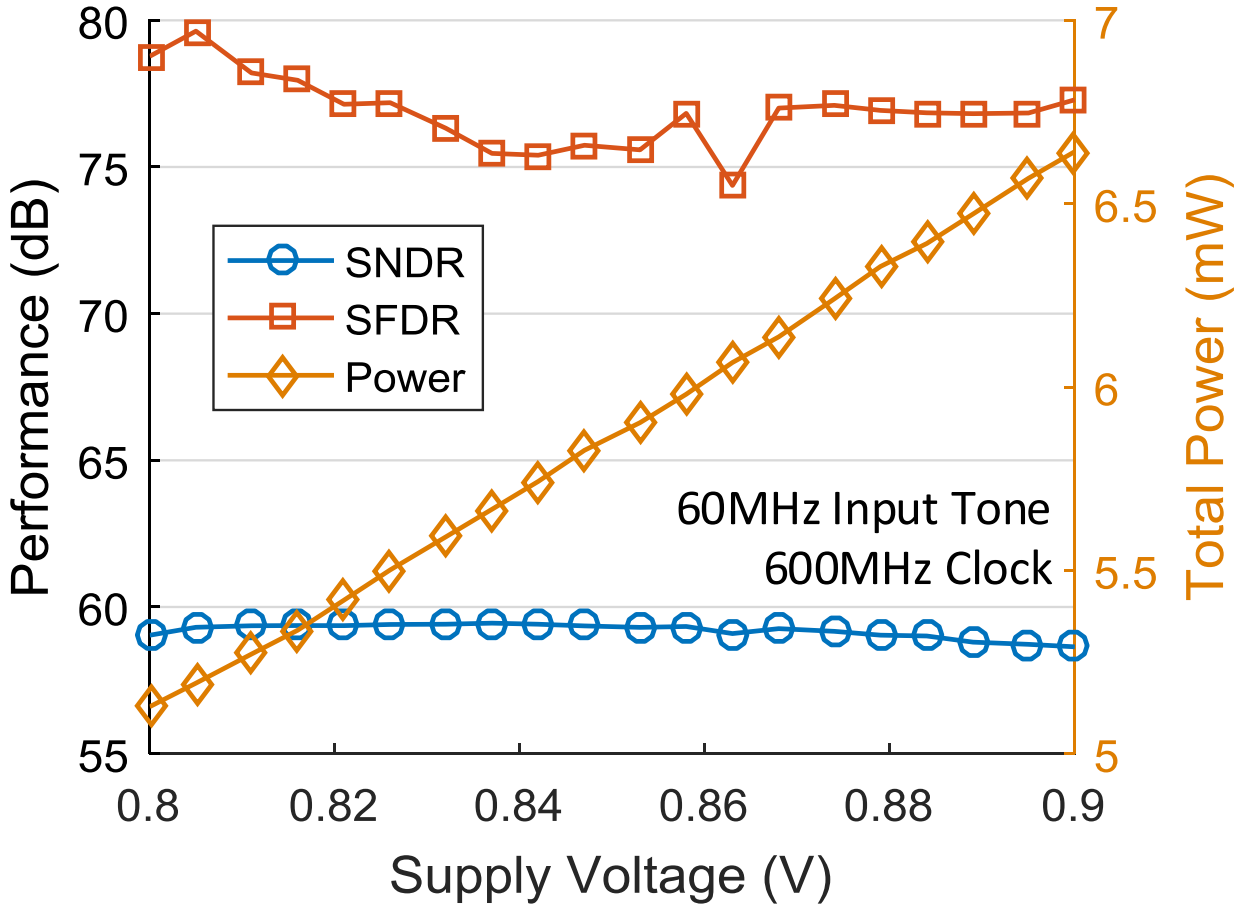
MEASURED PERFORMANCE



- Fully dynamic power consumption
  - Linear scaling w.r.t. clock
- Attractive feature for multi-standard mobile wireless applications

SWEEP: POWER SUPPLY

MEASURED PERFORMANCE

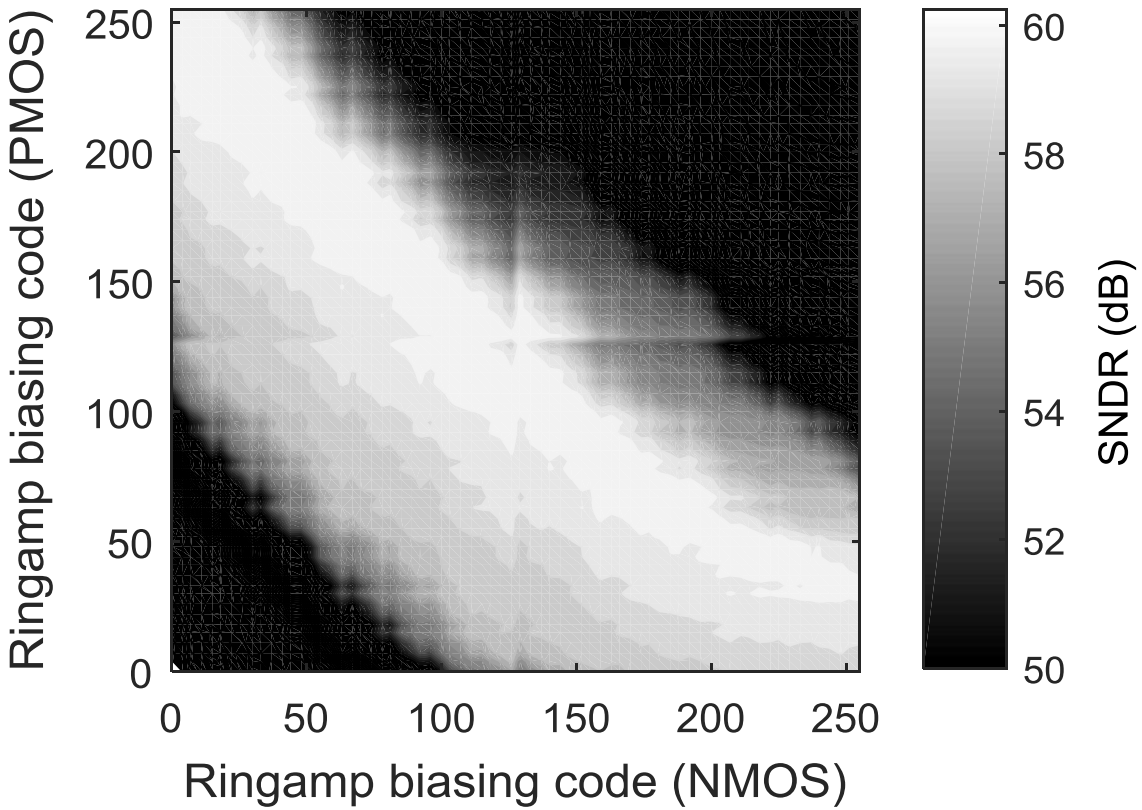


- Robust to supply variation
  - Ringamp
  - Timing delays
- V_{REFP} reduced to 750mV for this test

SWEEP: RINGAMP DIGITAL BIASING CONTROLS

MEASURED PERFORMANCE

Stage 1 Ringamp Digital Biasing Controls



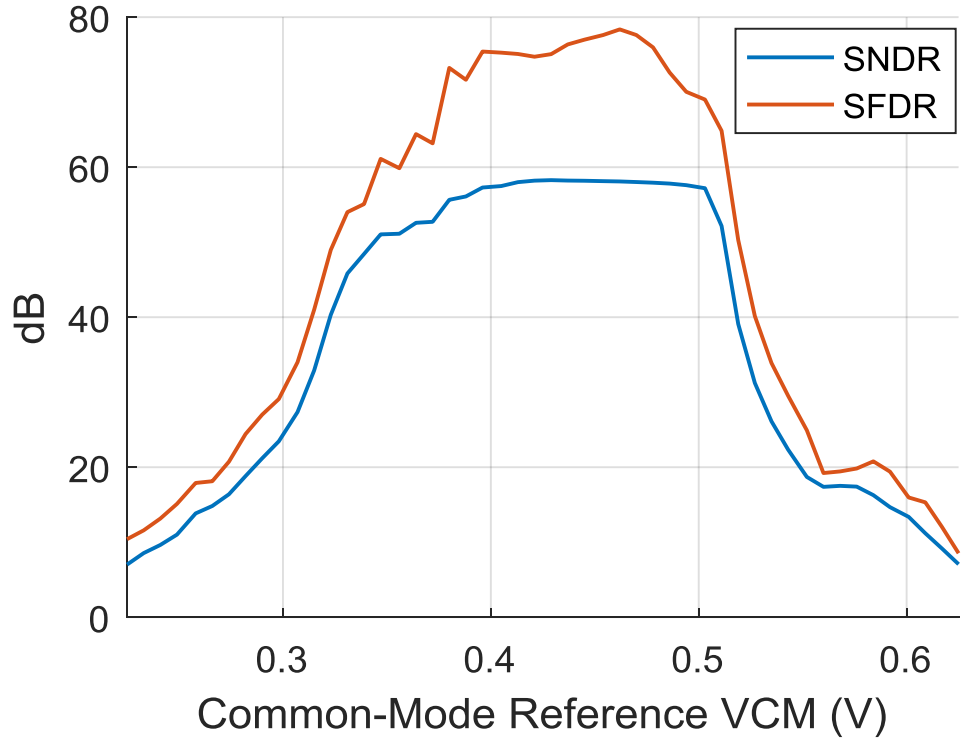
- Ringamp robust to biasing variation

SWEEP: COMMON-MODE REFERENCE

MEASURED PERFORMANCE

Internal Common-Mode Reference Voltage

-2dBFS input tone



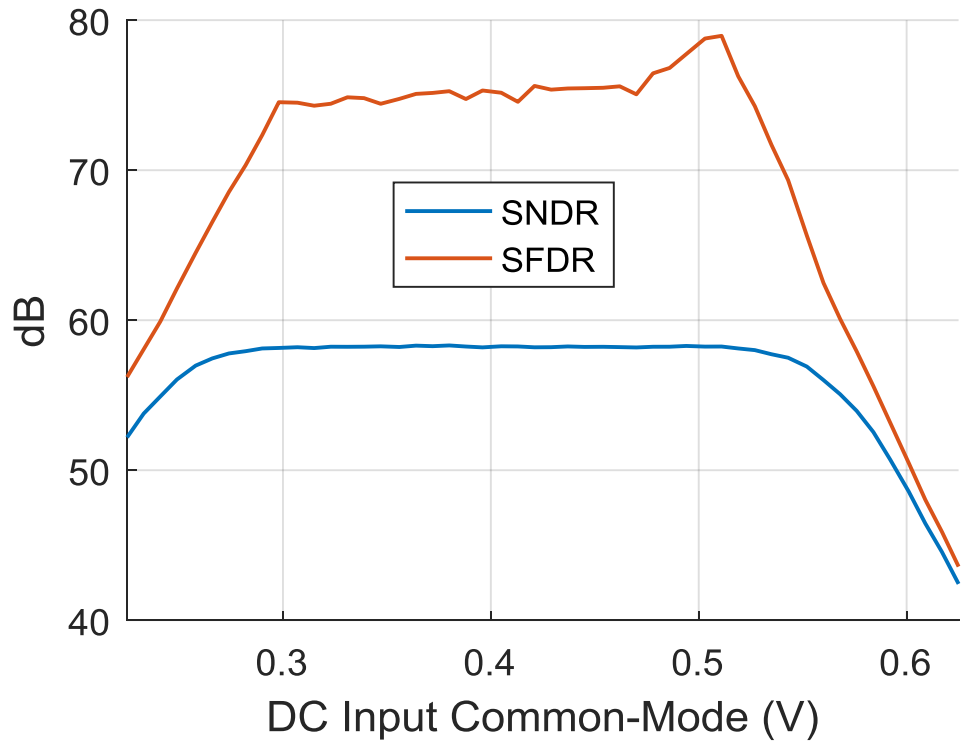
- *Internal* common mode reference V_{CM}
- Demonstrates robustness of Ringamp CMFB circuit
  - Shown in talk 3.1

SWEEP: INPUT COMMON MODE VOLTAGE

MEASURED PERFORMANCE

External Input Common-Mode Voltage

-2dBFS input tone



- *External* common-mode input V_{CMI} on PCB
- Demonstrates robustness of Ringamp CMFB circuit
  - Shown in talk 3.1

COMPARISON WITH SOTA

MEASURED PERFORMANCE

- SoTA comparison

	High Speed Ringamp SoTA			SoTA in [1] for SNDR > 56dB, Fs > 410MHz			
	This work	Lagos CICC 2018	Lagos VLSI 2017	Venca ISSCC 2016	Nam VLSI 2016	Lien VLSI 2016	Sung ISSCC 2015
Architecture	**Pipeline**	Pipeline	Pipeline	TI SAR ΔΣ	TI SAR ΔΣ	TI Pipe-SAR	TI FATI-SAR
Sampling rate (max) [MS/s]	**600**	1000	600	600	1600	800	1600
Number of channels	**1**	1	1	4	8	4	12
Per-channel rate [MS/s]	**600**	1000	600	150	200	200	133
Technology [nm]	**16**	28	28	28	65	28	65
ENOB Nyquist [bit]	**9.7**	9.1	9.1	9.3	10.6	9.8	9.0
SFDR Nyquist [dB]	**78.3**	73.1	69.2	66.0	65.3	75.0	61.2
Power [mW]	**6.0**	24.8	14.2	26.5	37.7	14.6	17.3
FoM_{Walden} [fJ/c.step]	**12.0**	45.0	44.3	68.0	17.8	20.0	21.0
$FoM_{Schreier}$ [dB]	**167.2**	159.6	159.5	158.5	168.6	165.2	162.8
Core area [mm^2]	**0.037**	0.540	0.620	0.042	0.900	0.093	0.360
Calibration	**gain**	gain	gain	offset, gain, mismatch	offset, gain, timing skew	offset, gain	offset

COMPARISON WITH SOTA

MEASURED PERFORMANCE

- High speed ringamp-based ADCs

	High Speed Ringamp SoTA			SoTA in [1] for SNDR > 56dB, Fs > 410MHz			
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Calibration	**gain**	gain	gain	offset, gain, mismatch	offset, gain, timing skew	offset, gain	offset

COMPARISON WITH SOTA

MEASURED PERFORMANCE

- High speed ringamp-based ADCs
- *All* ADCs with SNDR > 56dB, Fs > 410MHz

	High Speed Ringamp SoTA			SoTA in [1] for SNDR > 56dB, Fs > 410MHz			
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Calibration	**gain**	gain	gain	offset, gain, mismatch	offset, gain, timing skew	offset, gain	offset

COMPARISON WITH SOTA

MEASURED PERFORMANCE

- Competitive performance across all metrics
- Record FoM_W of 12fJ/c-step

	High Speed Ringamp SoTA			SoTA in [1] for SNDR > 56dB, Fs > 410MHz			
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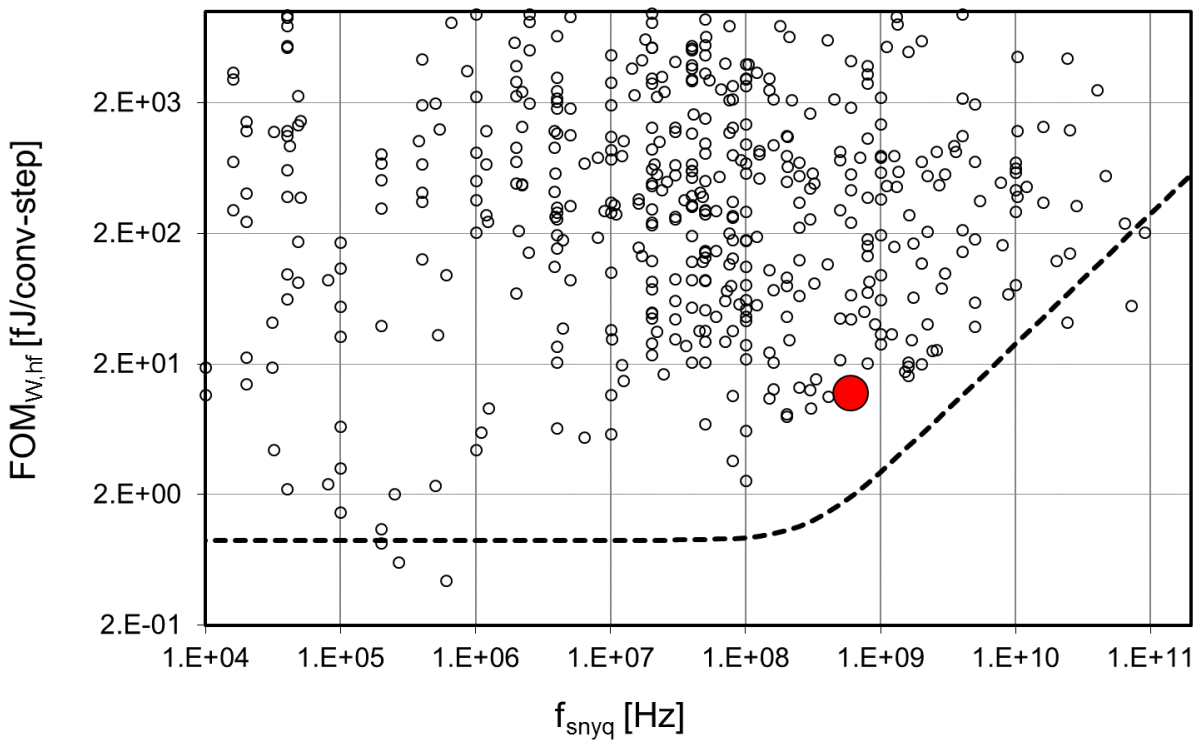
Per-channel rate [MS/s]	**600**	1000	600	150	200	200	133
Technology [nm]	**16**	28	28	28	65	28	65
ENOB Nyquist [bit]	**9.7**	9.1	9.1	9.3	10.6	9.8	9.0
SFDR Nyquist [dB]	**78.3**	73.1	69.2	66.0	65.3	75.0	61.2
Power [mW]	**6.0**	24.8	14.2	26.5	37.7	14.6	17.3
FoM_{Walden} [fJ/c.step]	**12.0**	45.0	44.3	68.0	17.8	20.0	21.0
$FoM_{Schreier}$ [dB]	**167.2**	159.6	159.5	158.5	168.6	165.2	162.8
Core area [mm²]	**0.037**	0.540	0.620	0.042	0.900	0.093	0.360
Calibration	**gain**	gain	gain	offset, gain, mismatch	offset, gain, timing skew	offset, gain	offset

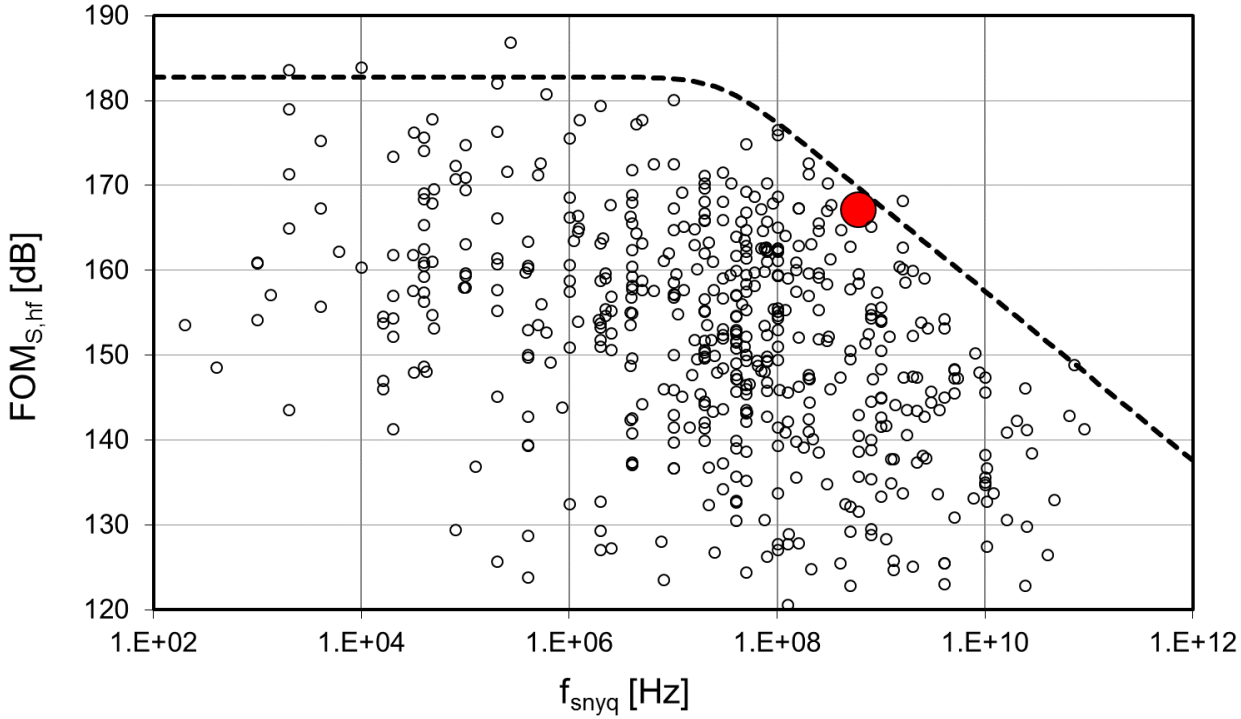
COMPARISON WITH SOTA

MEASURED PERFORMANCE

Walden FoM



Schreier FoM



B. Murmann, "ADC Performance Survey 1997-2018," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

THE BIG PICTURE

CONCLUSION

- Asynchronous, event-driven control in “deep” pipelines offers many compelling benefits
  - Efficient
  - Reconfigurable
  - Robust

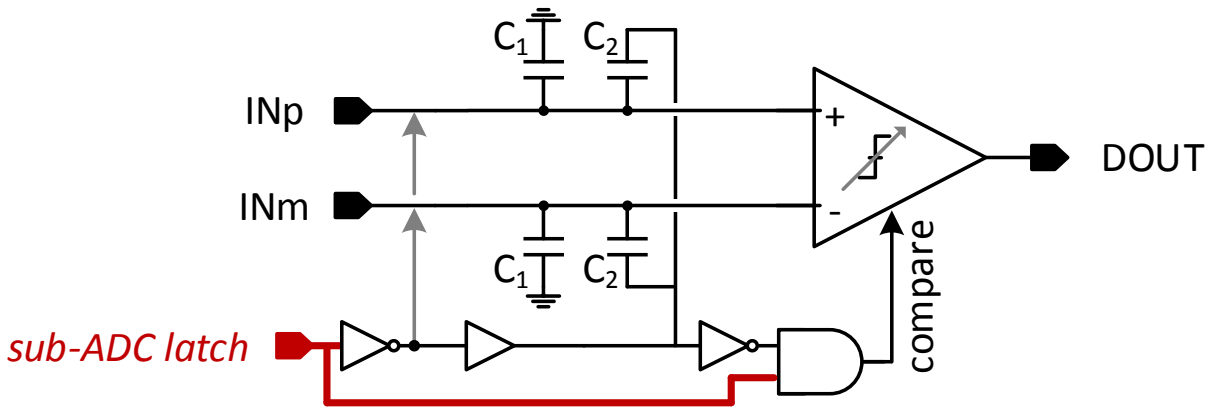
- High speed ringamp-based pipelines offer a viable alternative to multi-channel SAR architectures

THANK YOU FOR YOUR ATTENTION!

ADDITIONAL MATERIALS...

EARLY QUANTIZATION

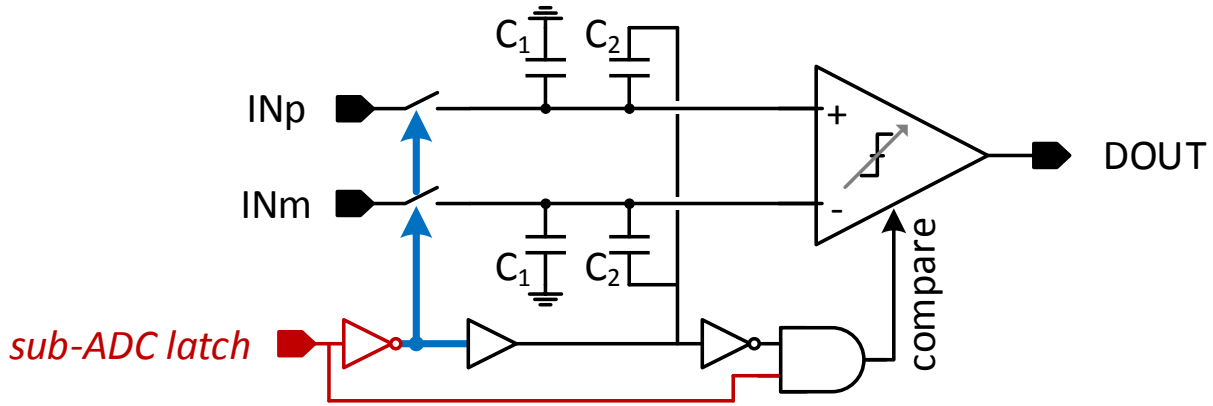
SUB-ADC IMPLEMENTATION DETAILS



1. Receives previous stage ringamp's slew-done signal

EARLY QUANTIZATION

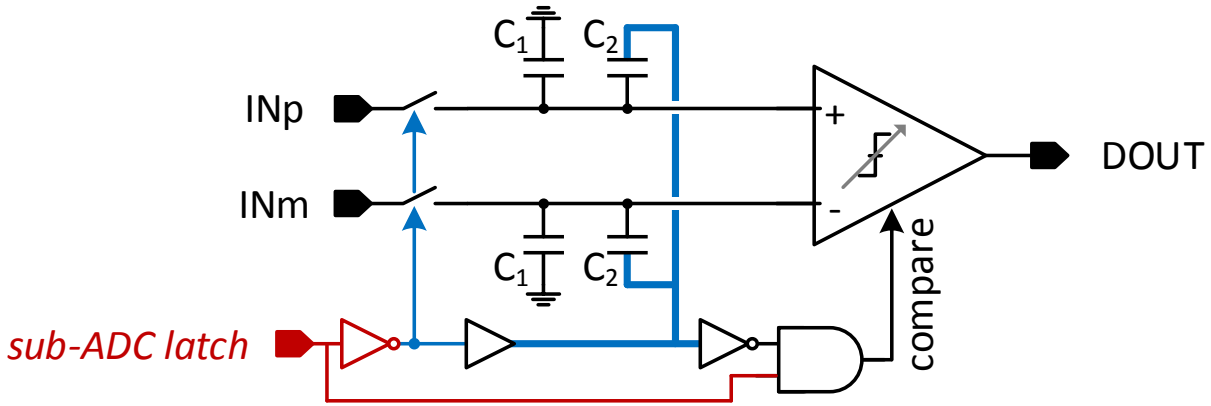
SUB-ADC IMPLEMENTATION DETAILS



1. Receives previous stage ringamp's slew-done signal
2. Samples previous stage

EARLY QUANTIZATION

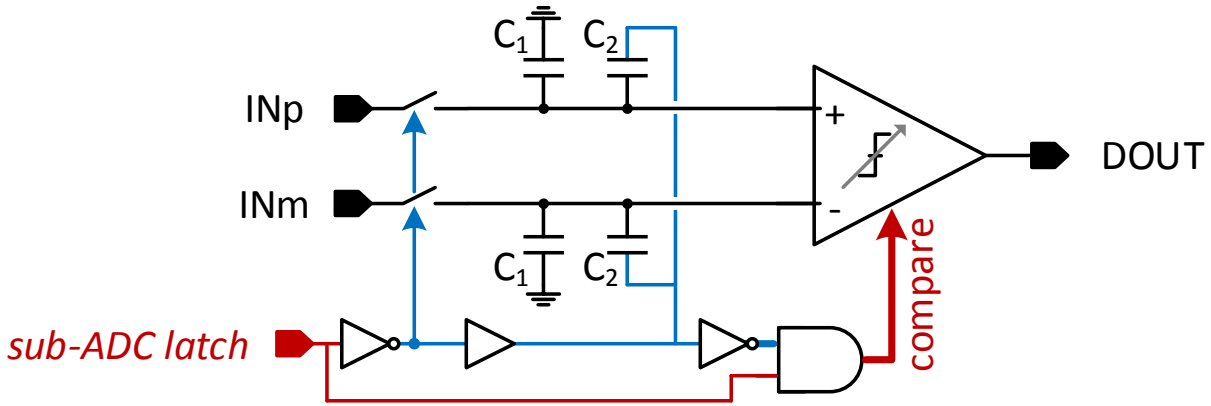
SUB-ADC IMPLEMENTATION DETAILS



1. Receives previous stage ringamp's slew-done signal
2. Samples previous stage
3. Down-shifts internal common-mode voltage

EARLY QUANTIZATION

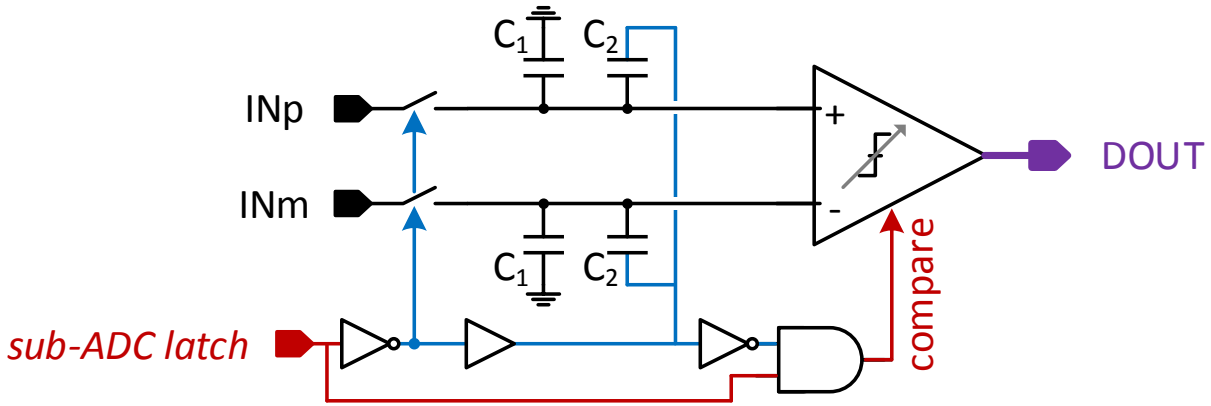
SUB-ADC IMPLEMENTATION DETAILS



1. Receives previous stage ringamp's slew-done signal
2. Samples previous stage
3. Down-shifts internal common-mode voltage
4. Initiates comparison

EARLY QUANTIZATION

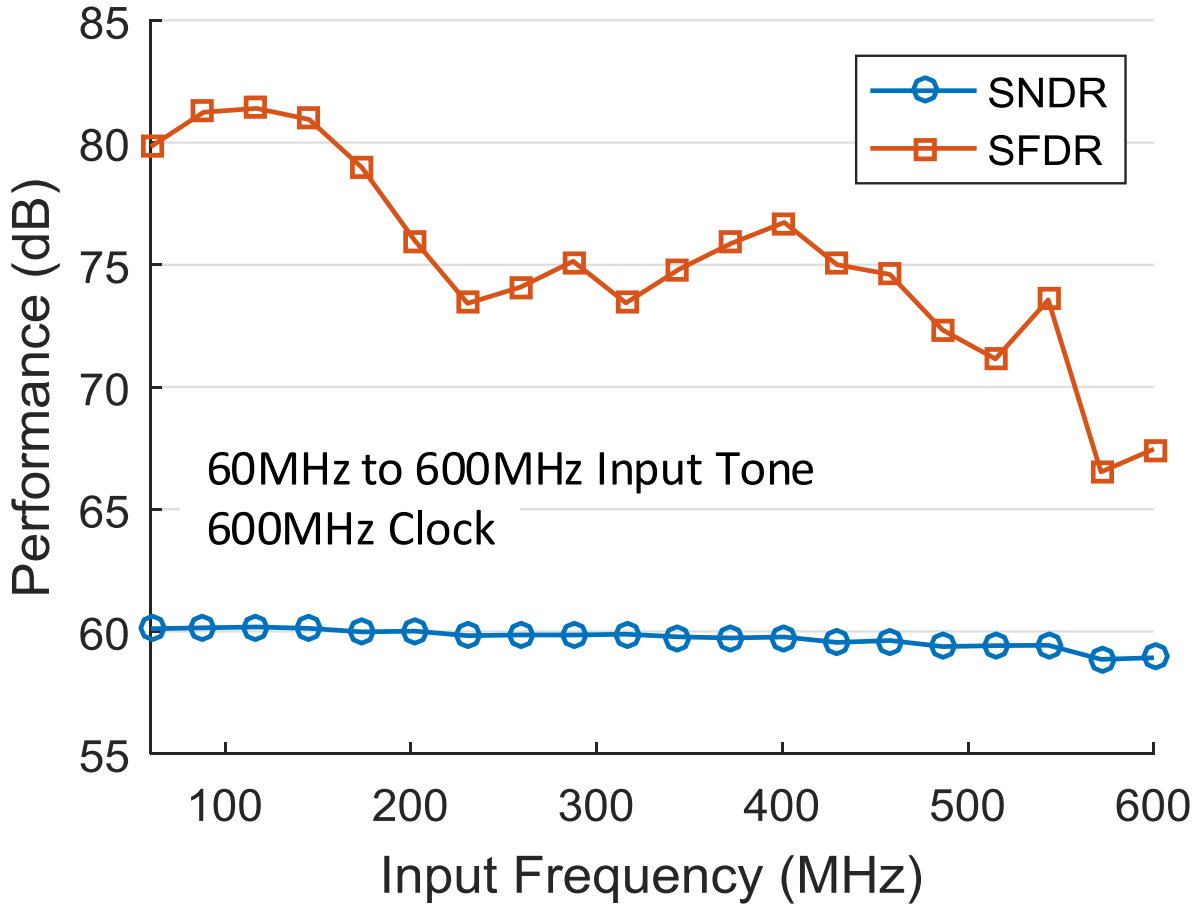
SUB-ADC IMPLEMENTATION DETAILS



1. Receives previous stage ringamp's slew-done signal
2. Samples previous stage
3. Down-shifts internal common-mode voltage
4. Initiates comparison
5. Sends result to subDAC

SWEEP: INPUT FREQUENCY

MEASURED PERFORMANCE



- Linearity limited by pass-gate input switches
  - Benefits of 16nm allow for pass-gates instead of bootstrapping