Ringamp: The Scalable Amplifier We've All Been Waiting For?

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Imec

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IEEE SOLID-STATE CIRCUITS SOCIETY™ | IEEE

NANOSCALE CMOS

ADAPTATION AND SURVIVAL

Some ADC architectures have thrived and expanded.

SAR

VCO-based

CT ΔΣ

NANOSCALE CMOS

ADAPTATION AND SURVIVAL

Others have lost ground,
forced into niche applications.

Pipeline

Folding Flash

Algorithmic

DT ΔΣ

Sub-Ranging

NANOSCALE CMOS

ADAPTATION AND SURVIVAL

The reason?

... a hidden bottleneck:

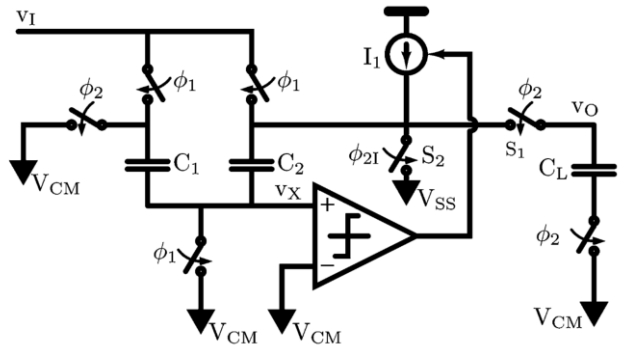
Residue Amplification

What did we lose in diversity?

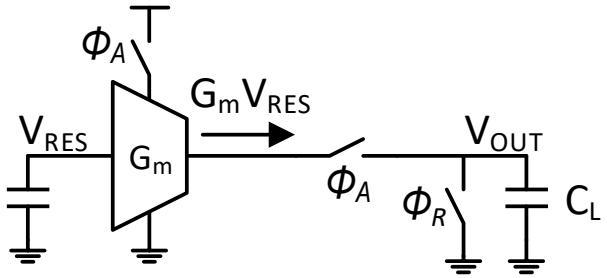
How has this constrained our solutions?

REPLACING THE OPAMP

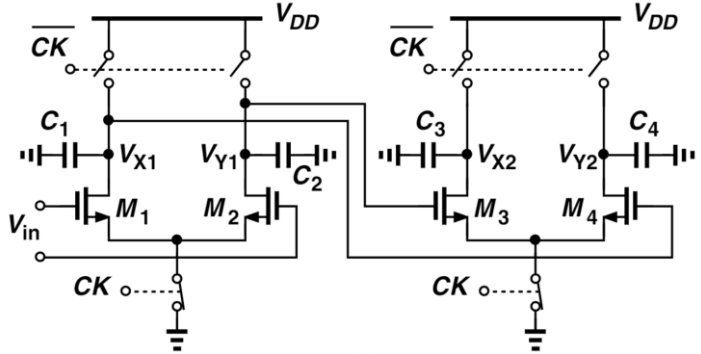
PROPOSED SOLUTIONS



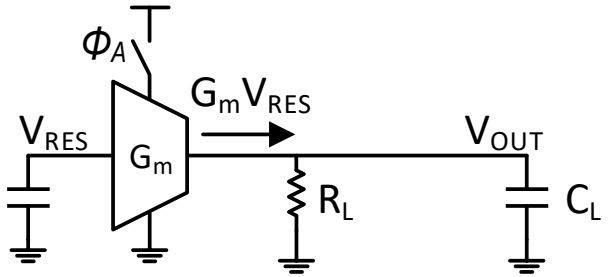
Zero-crossing based



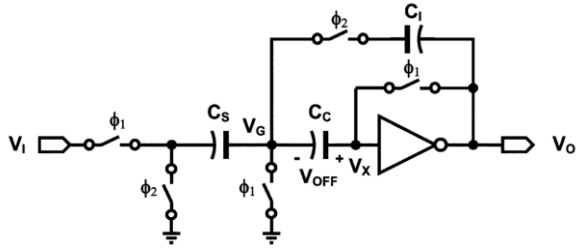
Gm-C style Dynamic Amplifier



Charge-steering

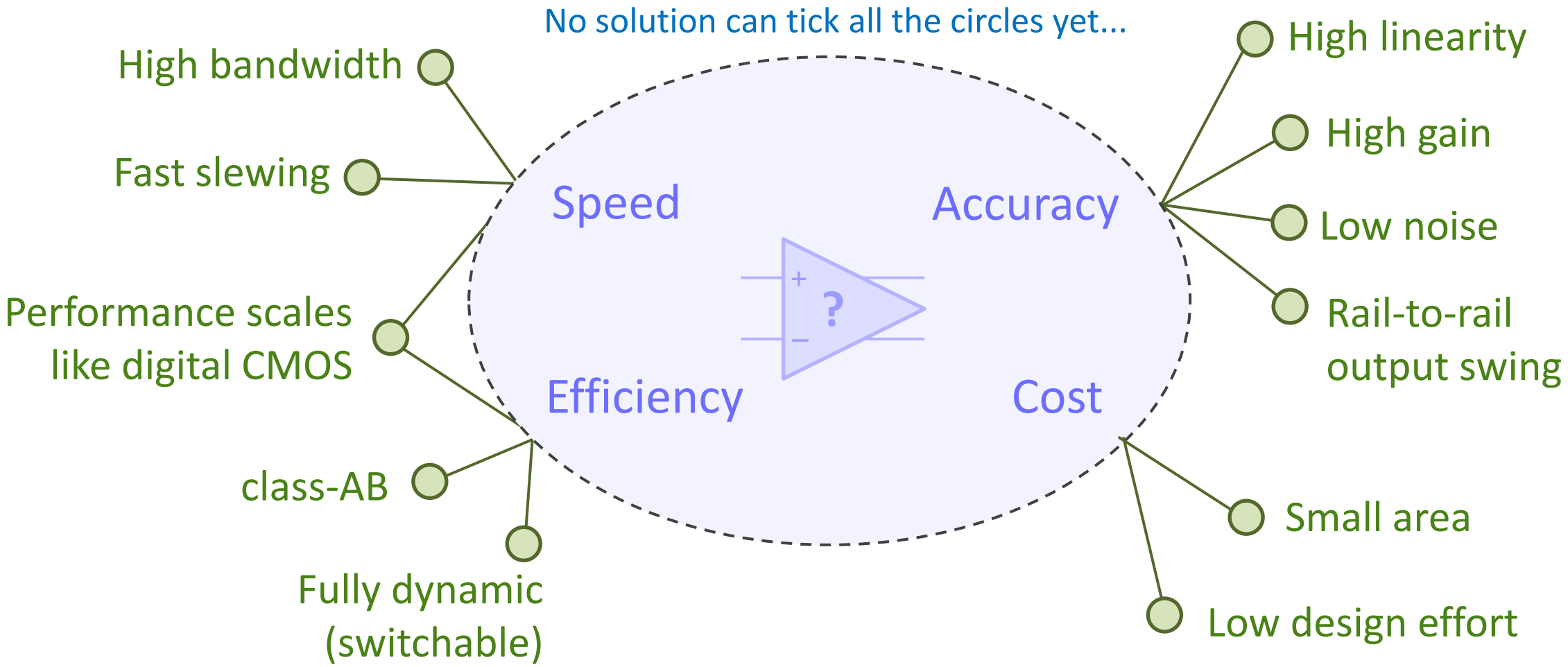


Gm-R style Dynamic Amplifier



Inverter based

THE “IDEAL AMPLIFIER” WISHLIST



THE “IDEAL AMPLIFIER” WISHLIST

what else can we try?

High bandwidth

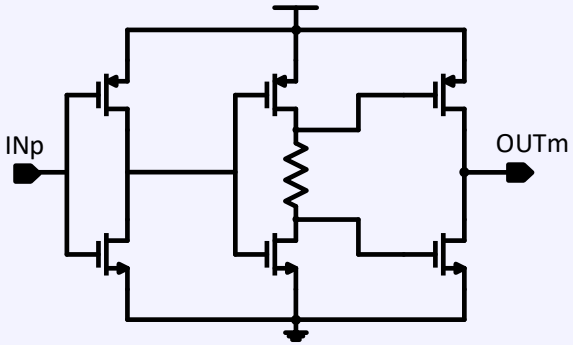
Fast slewing

Performance scales like digital CMOS

class-AB

Fully dynamic (switchable)

Ring Amplifier (ringamp)



High linearity

High gain

Low noise

Rail-to-rail output swing

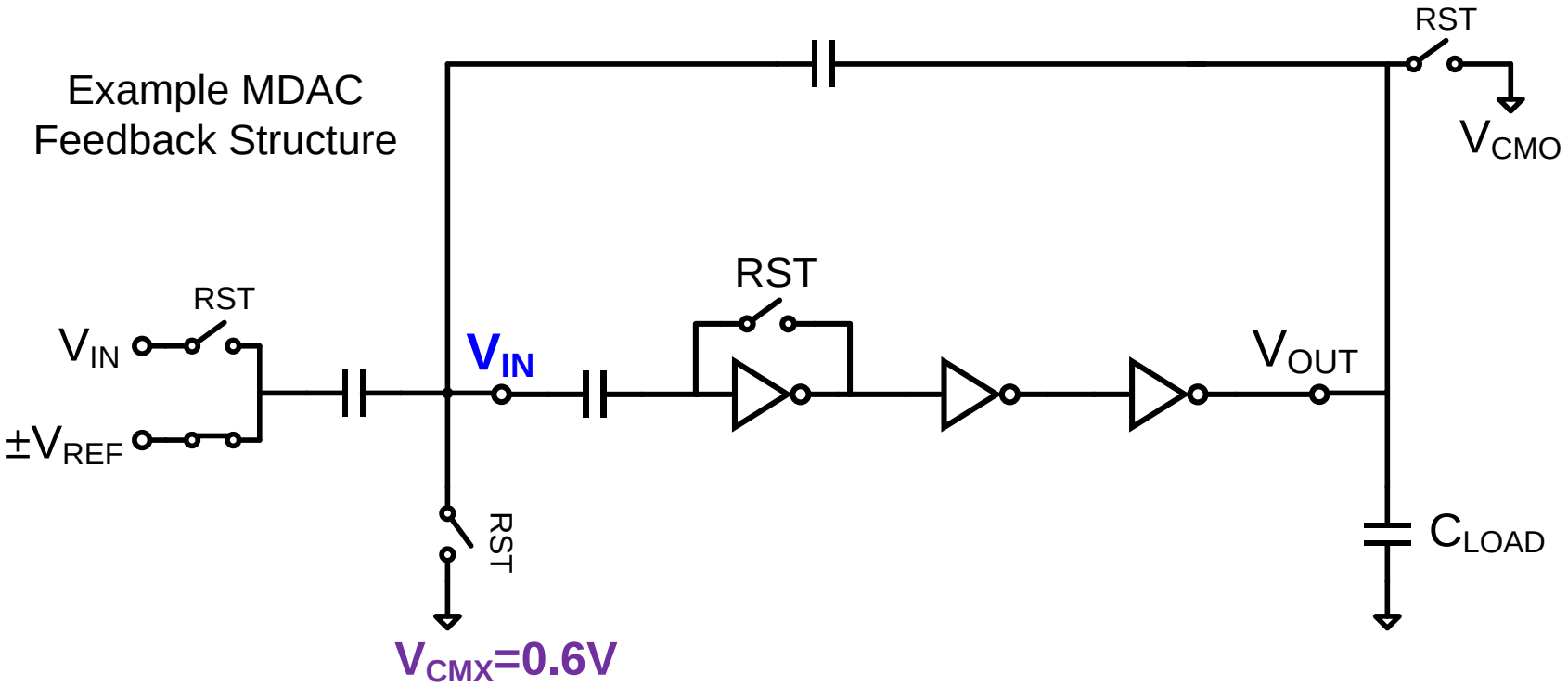
Small area

Low design effort

FUNDAMENTALS

RING OSCILLATOR

IN SWITCHED CAPACITOR FEEDBACK



RING OSCILLATOR

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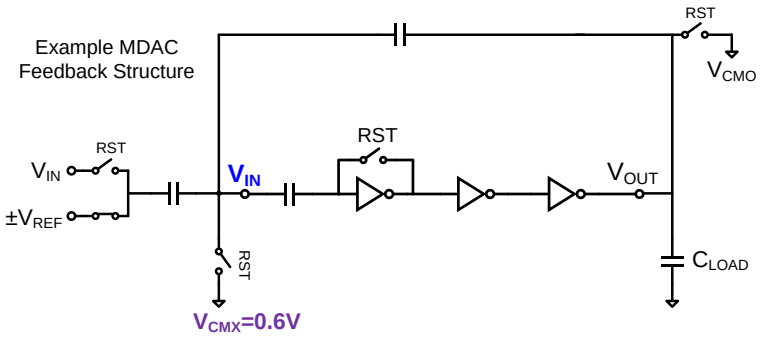
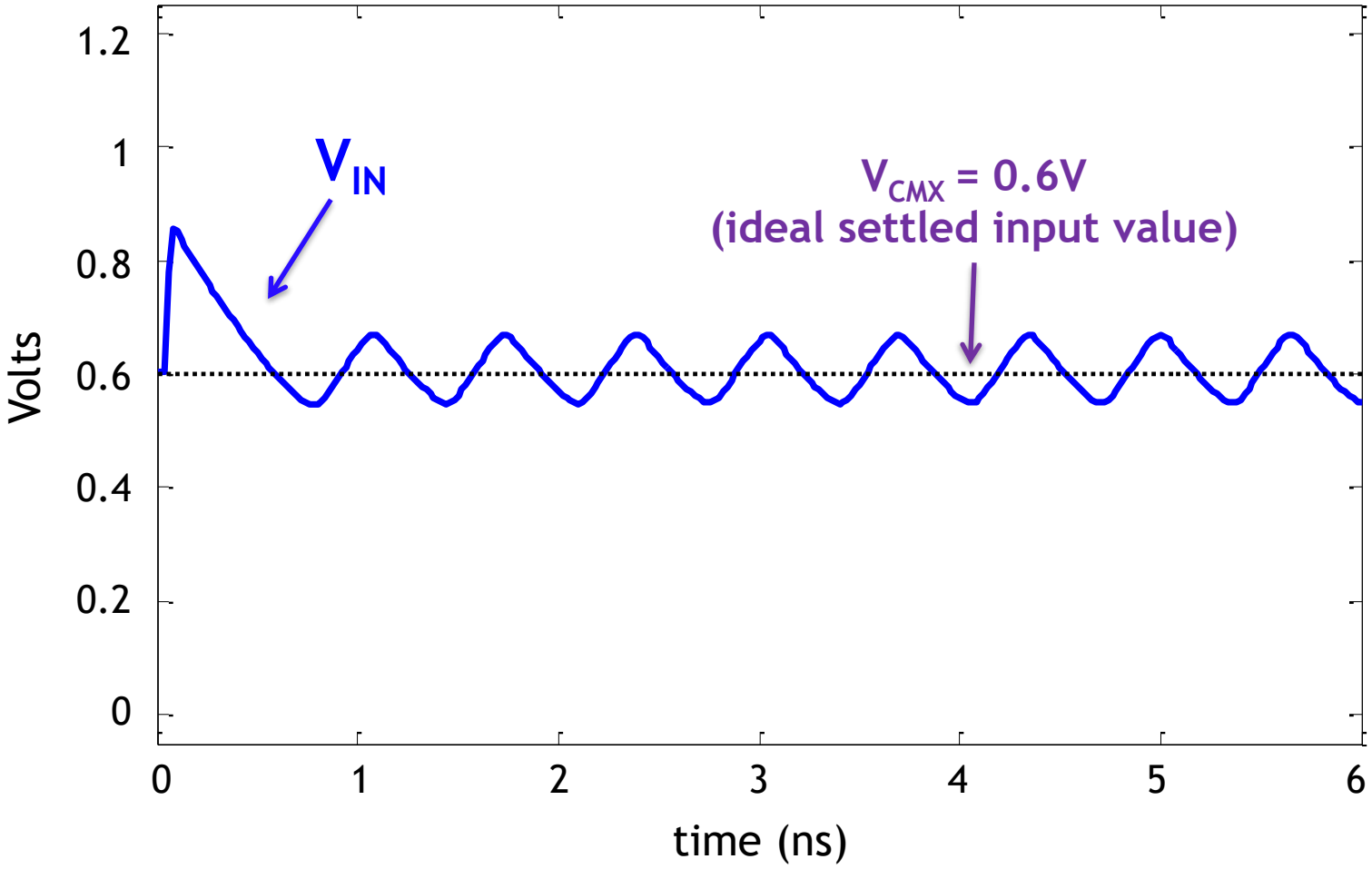
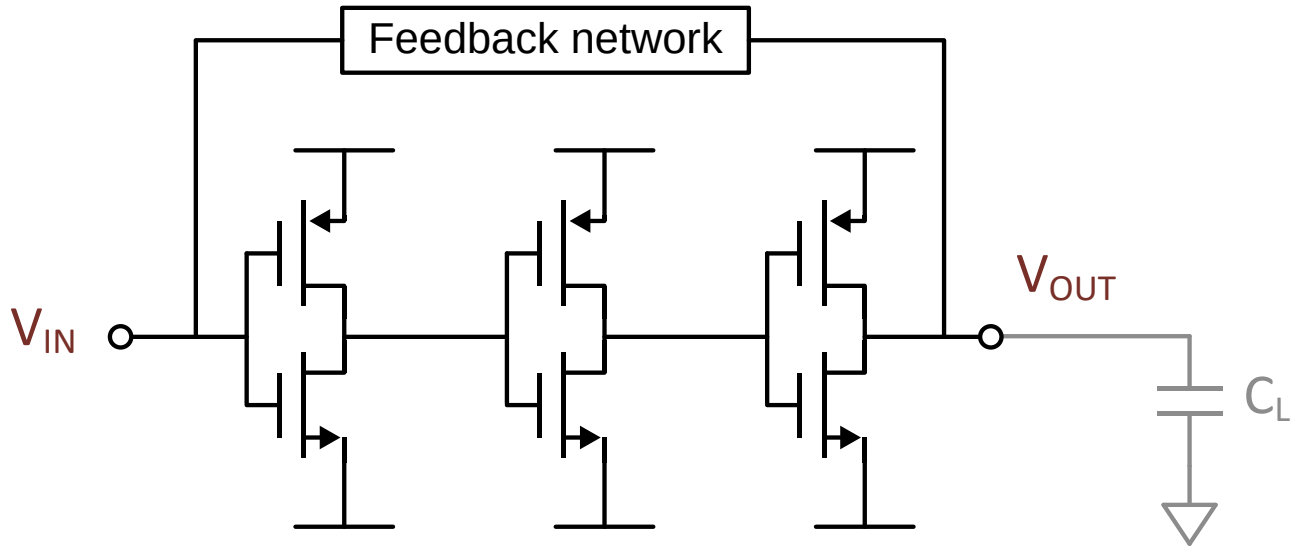




RING OSCILLATOR

IN SWITCHED CAPACITOR FEEDBACK

- ☺ Large gain
- ☺ Rail to rail swing
- ☺ Maximal slewing efficiency
- ☺ Small, simple layout
- ☺ Inherent class-AB behavior
- ☺ Fully compatible with digital CMOS



Sounds great! Only one problem…

IT'S AN OSCILLATOR!

DUALITY

OSCILLATOR → AMPLIFIER

Any ring oscillator can be stabilized

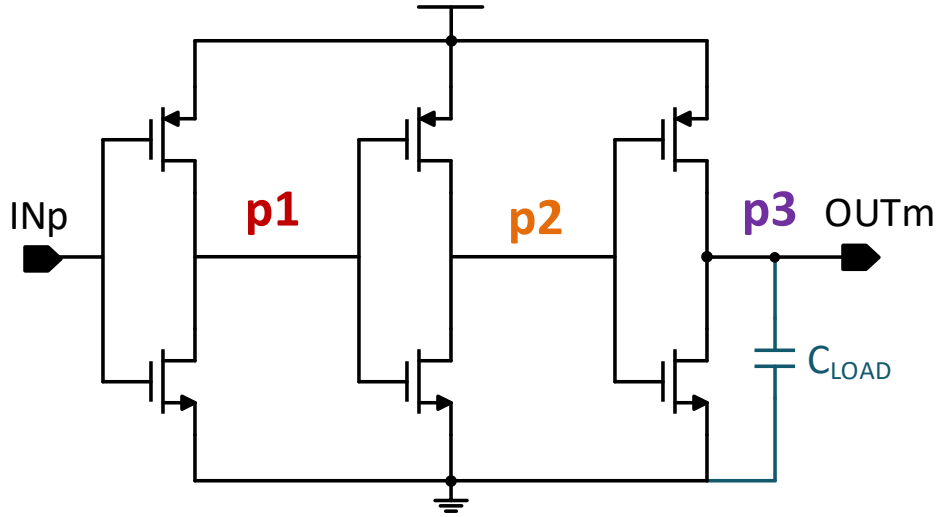
It’s just a matter of putting the poles in the right place

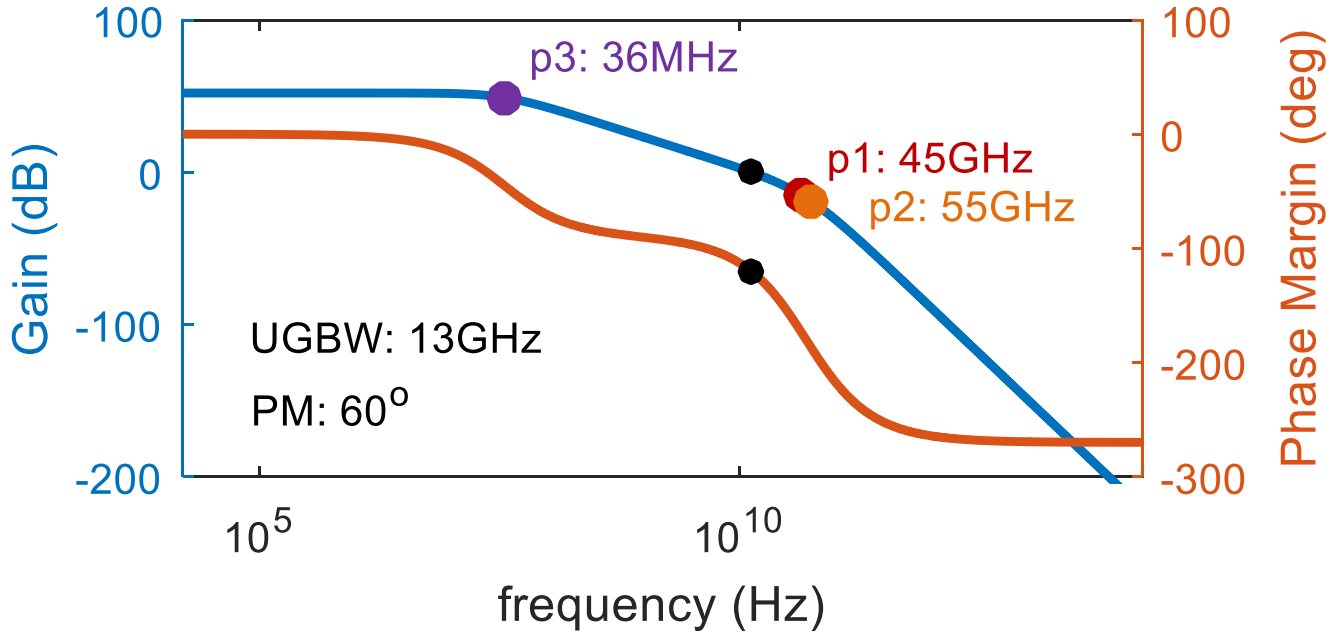
RING AMPLIFIER

BASIC PRINCIPLES

- Make p1 & p2 as fast as technology will allow
  - p1 & p2 constrained by technology limits, not kT/C_{LOAD} noise requirement
  - Scales well into nanoscale CMOS

- Stabilize with p3
  - ring oscillator → ring amplifier

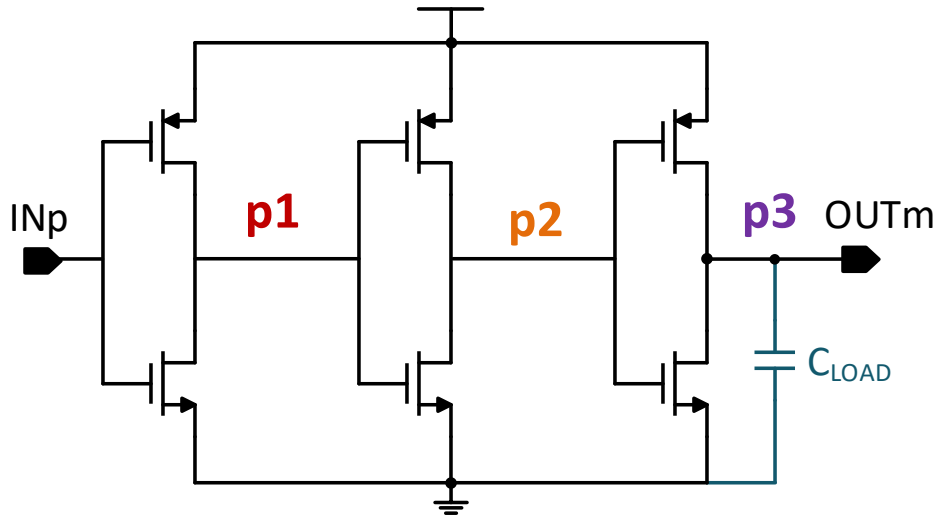




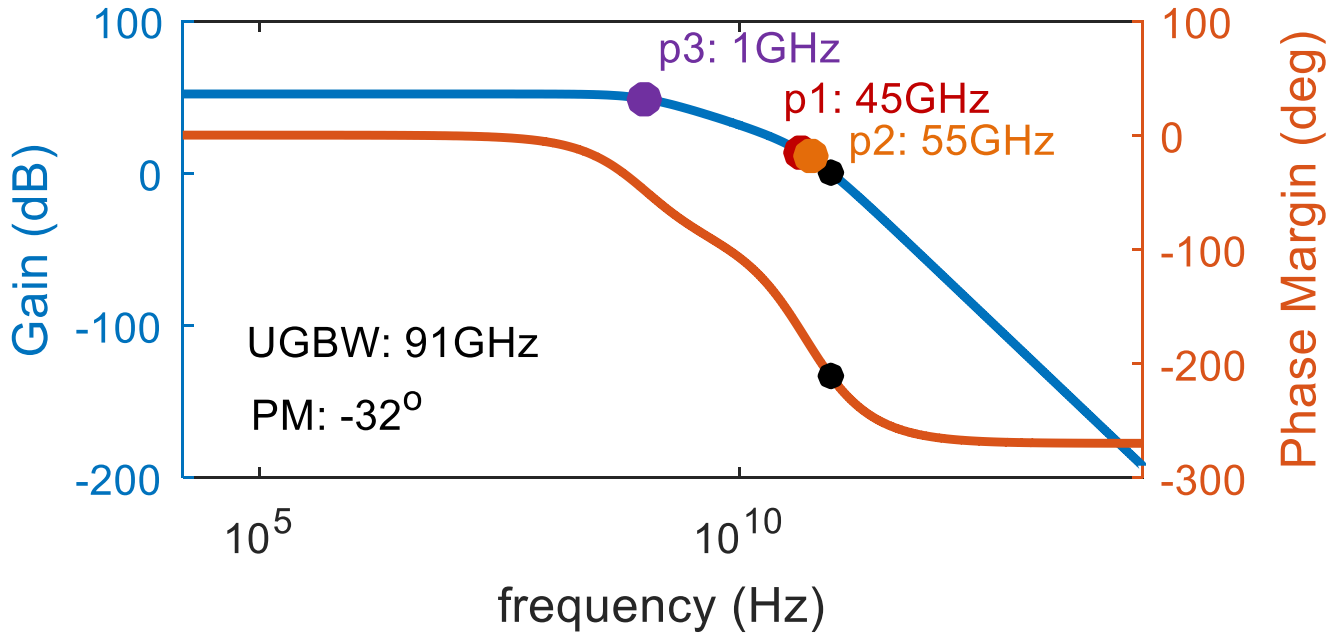
RING AMPLIFIER

BASIC PRINCIPLES

- But we can do even better
  - Dynamic biasing



Begin very fast but unstable:



RING AMPLIFIER

BASIC PRINCIPLES

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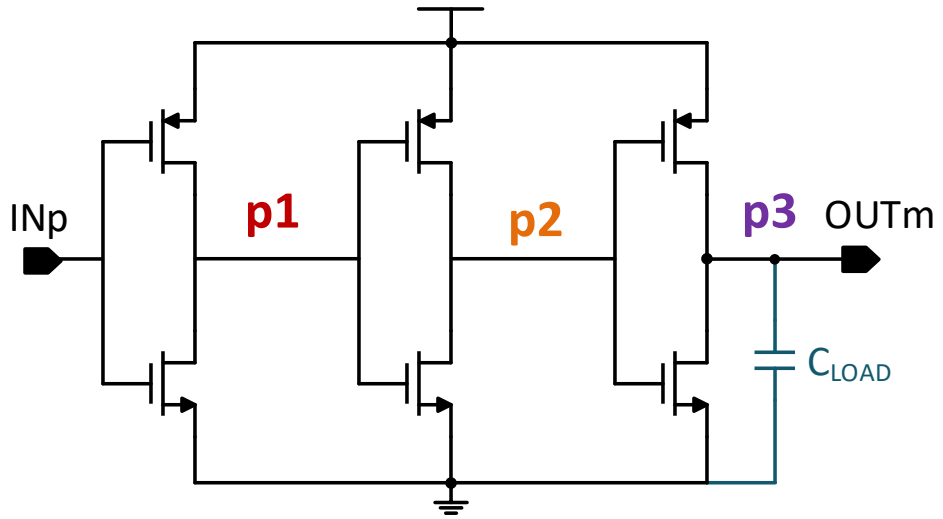
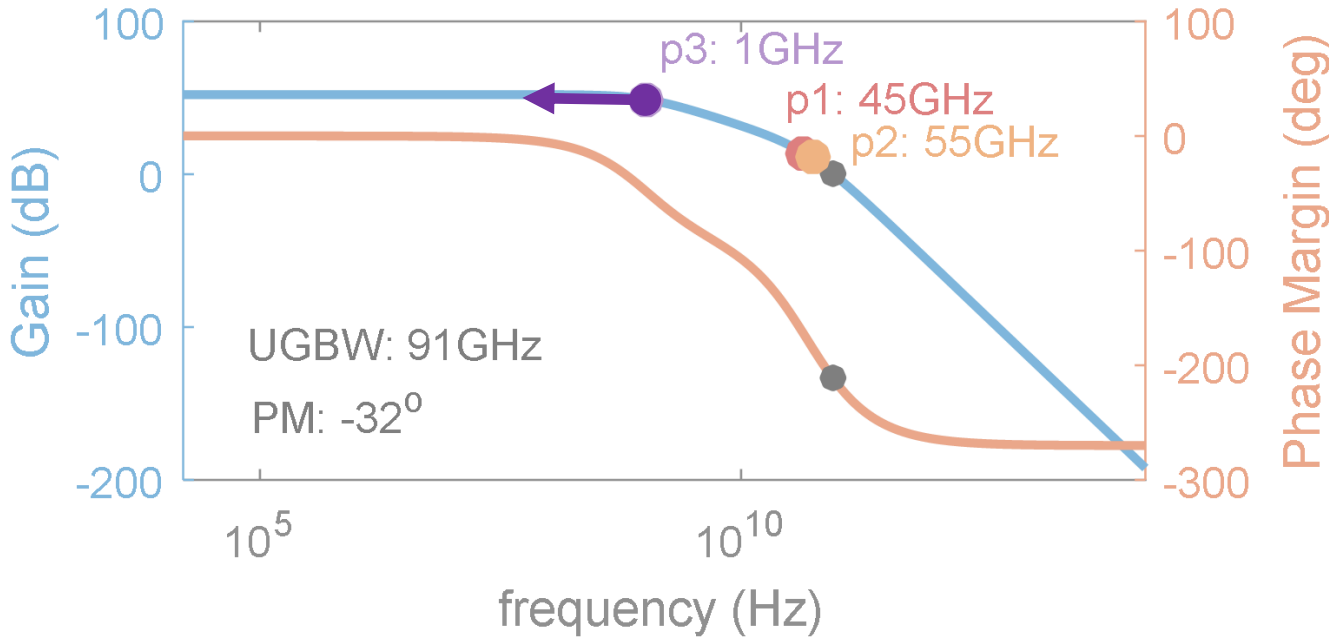


Dynamically shift output pole:



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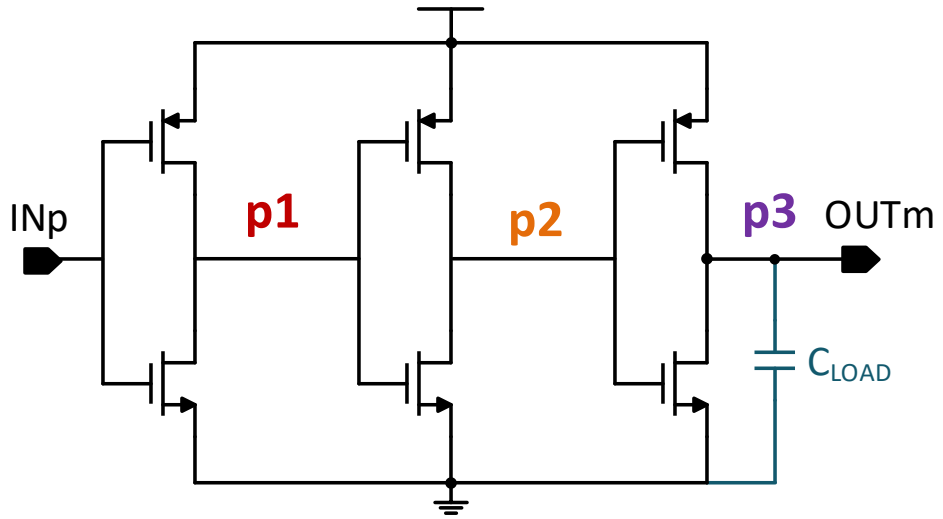
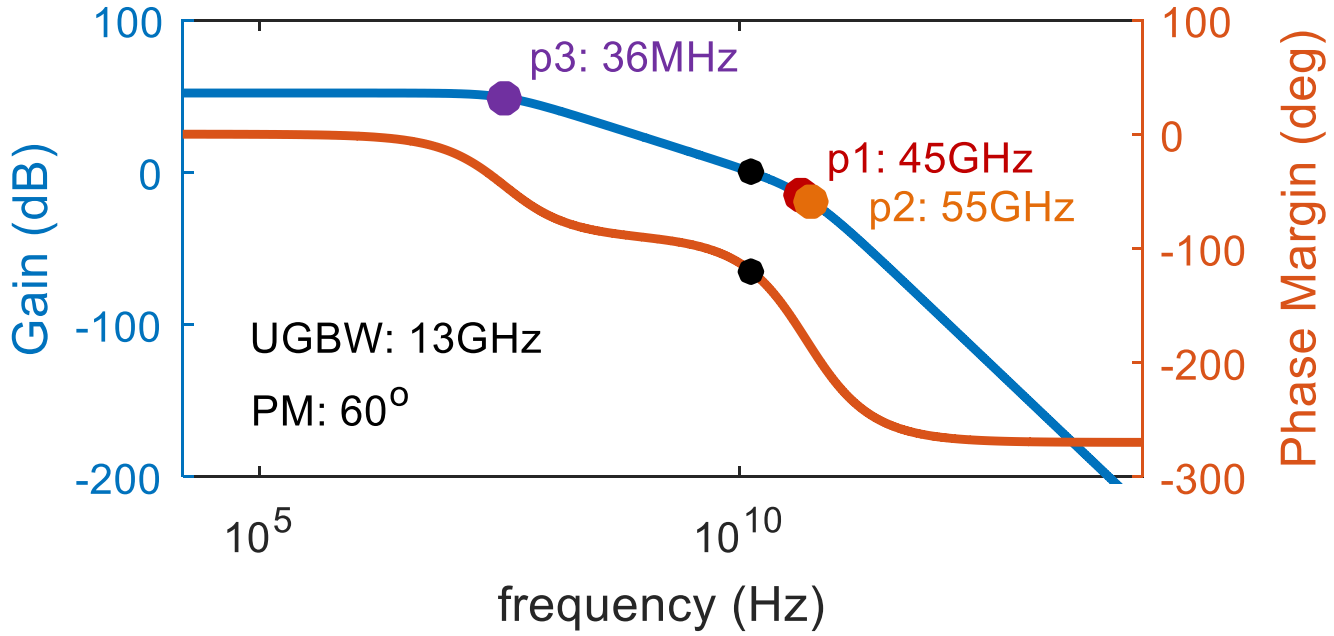


Stable steady-state:

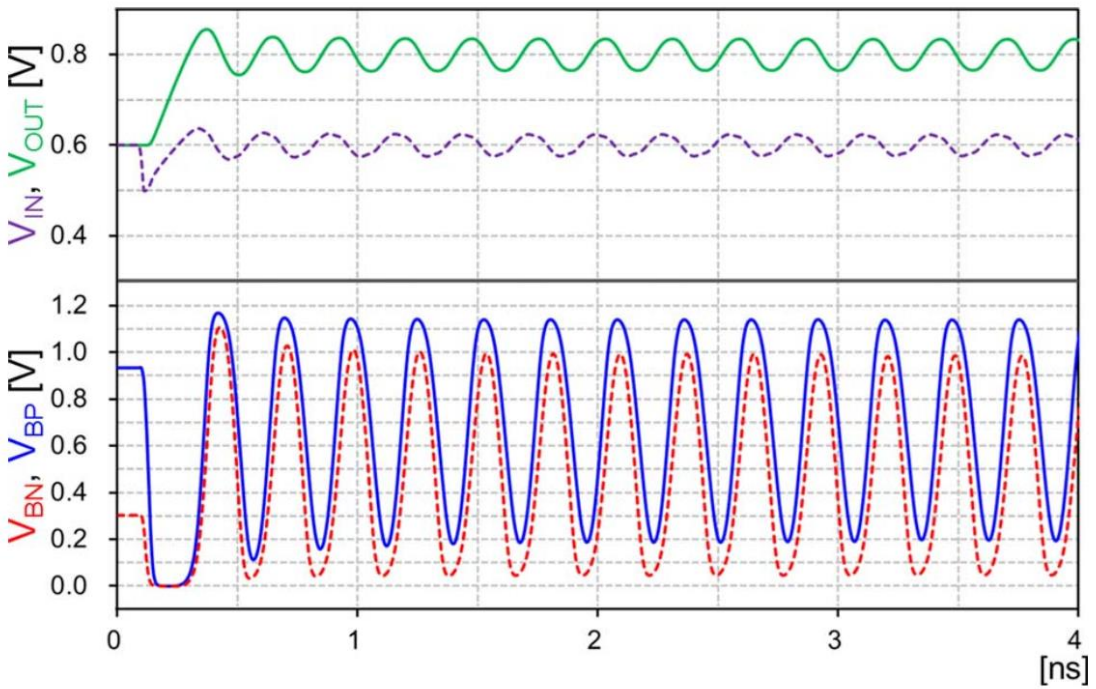


RING AMPLIFIER

BASIC PRINCIPLES

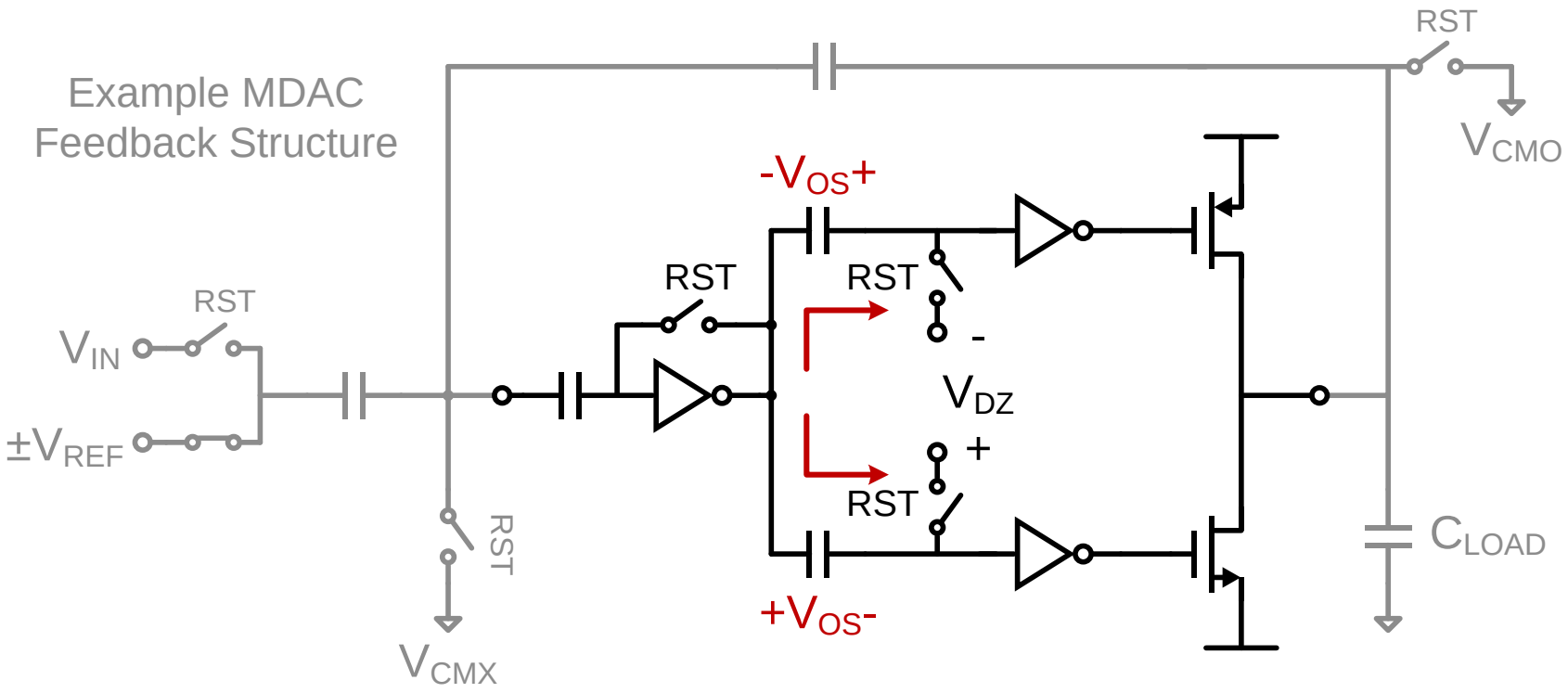
- AC analysis only explains steady-state
  - How do we *get* to steady state?
  - Do we *ever* get to steady state?
- Must also consider
  - DC
  - Transient

A “stable” ringamp with 73^{o} phase margin:



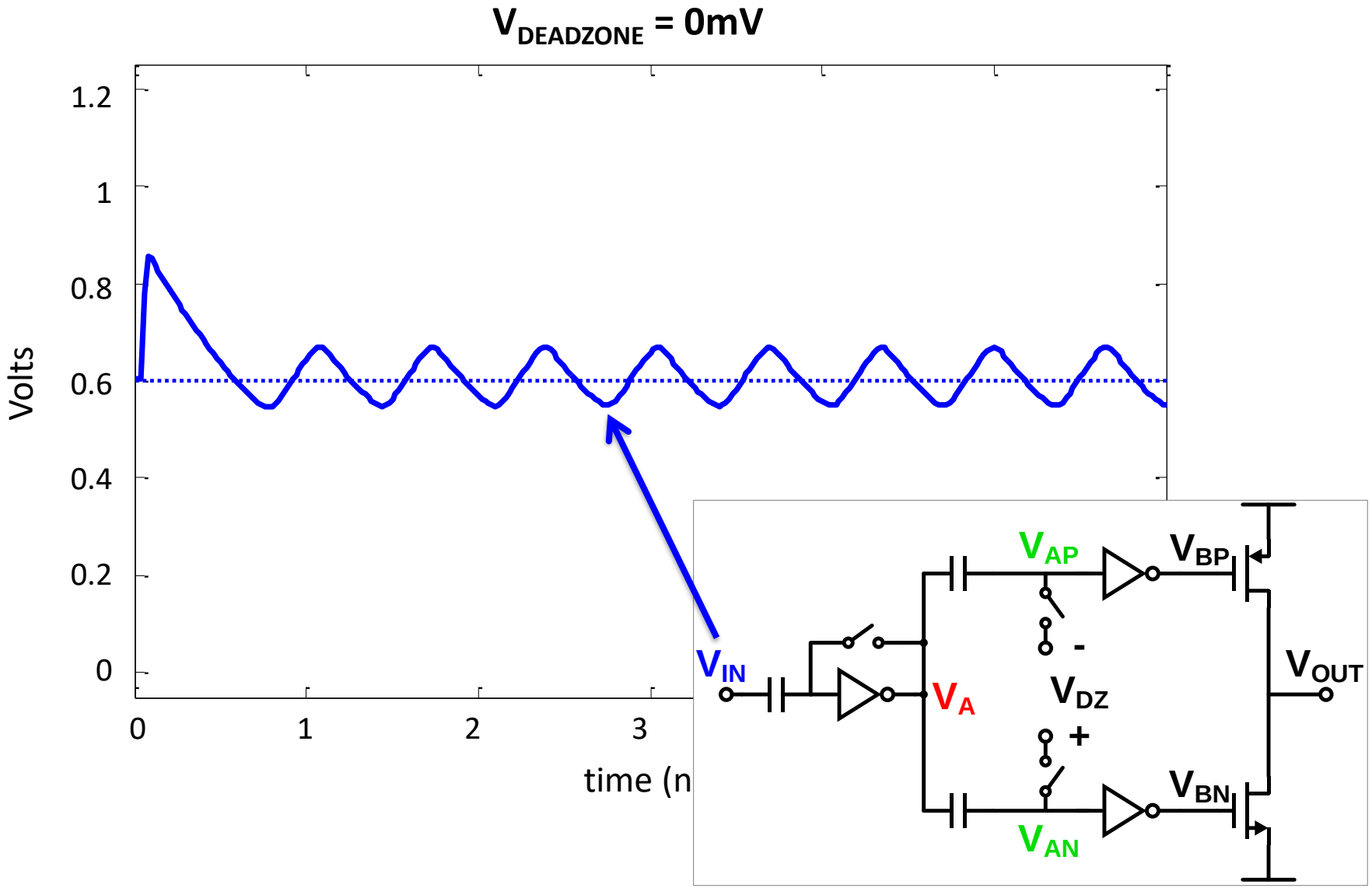
[Lim, JSSC 2015]

DYNAMIC LARGE-SIGNAL STABILIZATION



- Split signal into two paths
- Shift DC level (of transient wave) differently in each path

DYNAMIC LARGE-SIGNAL STABILIZATION



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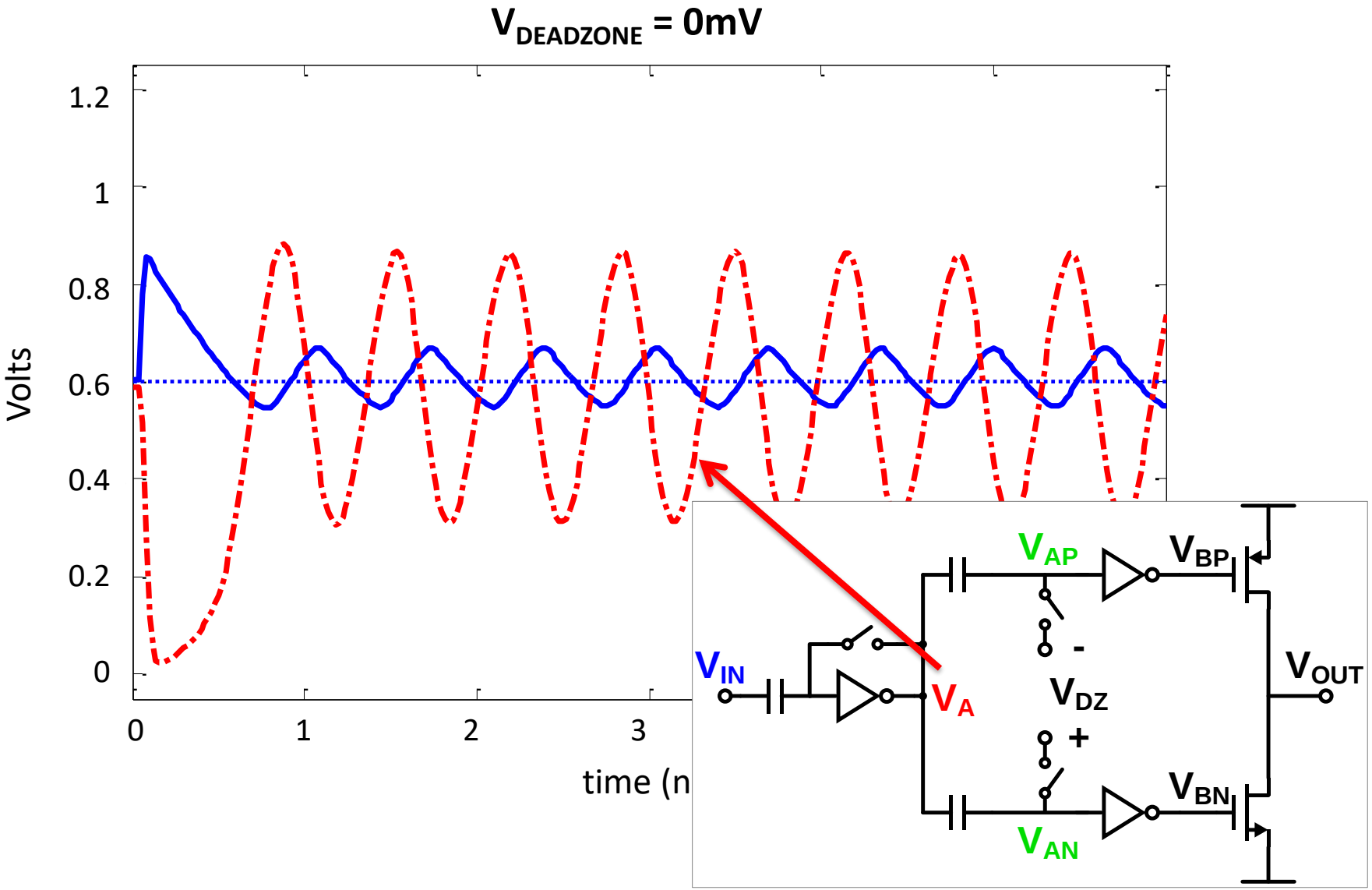

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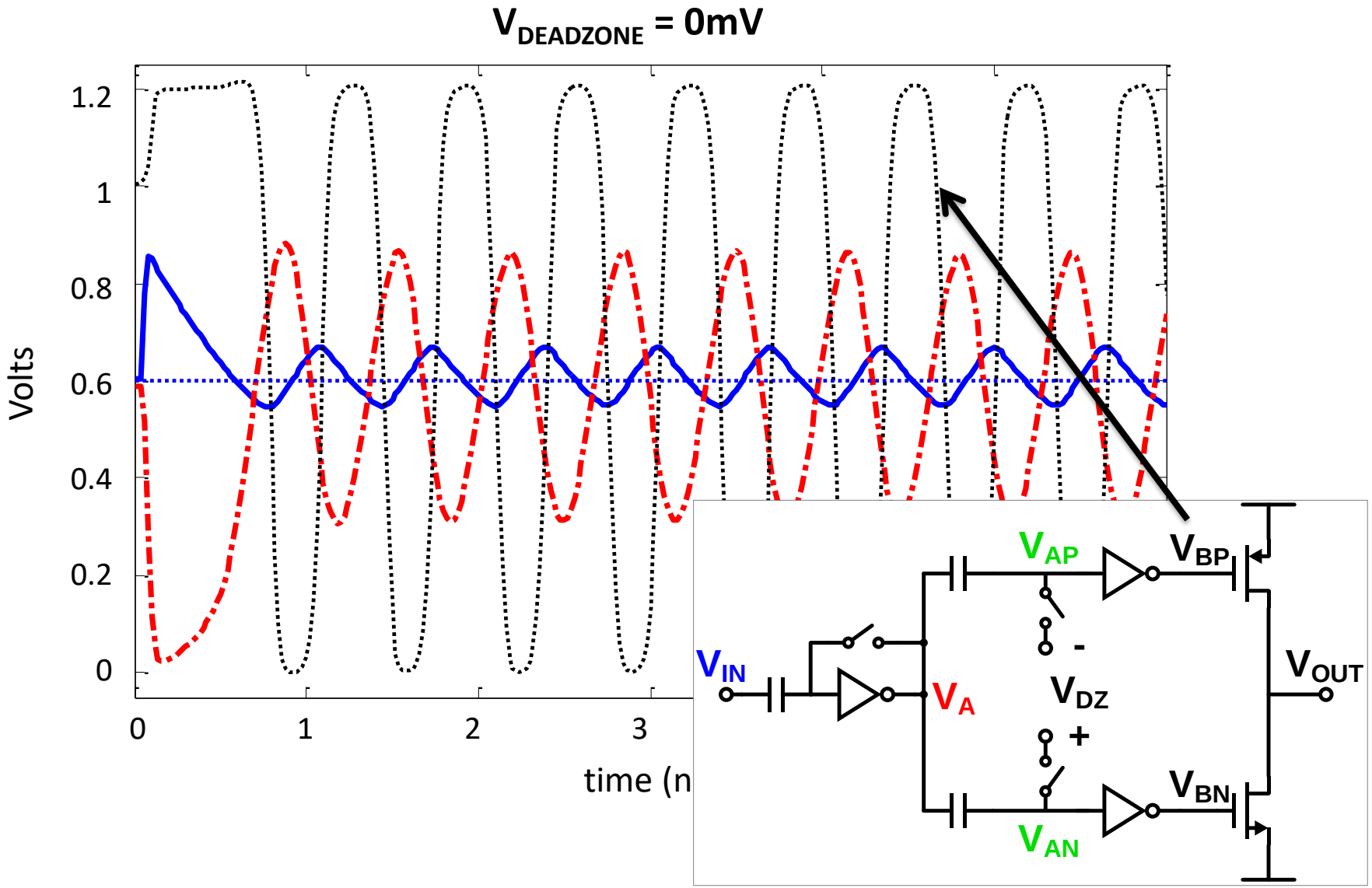

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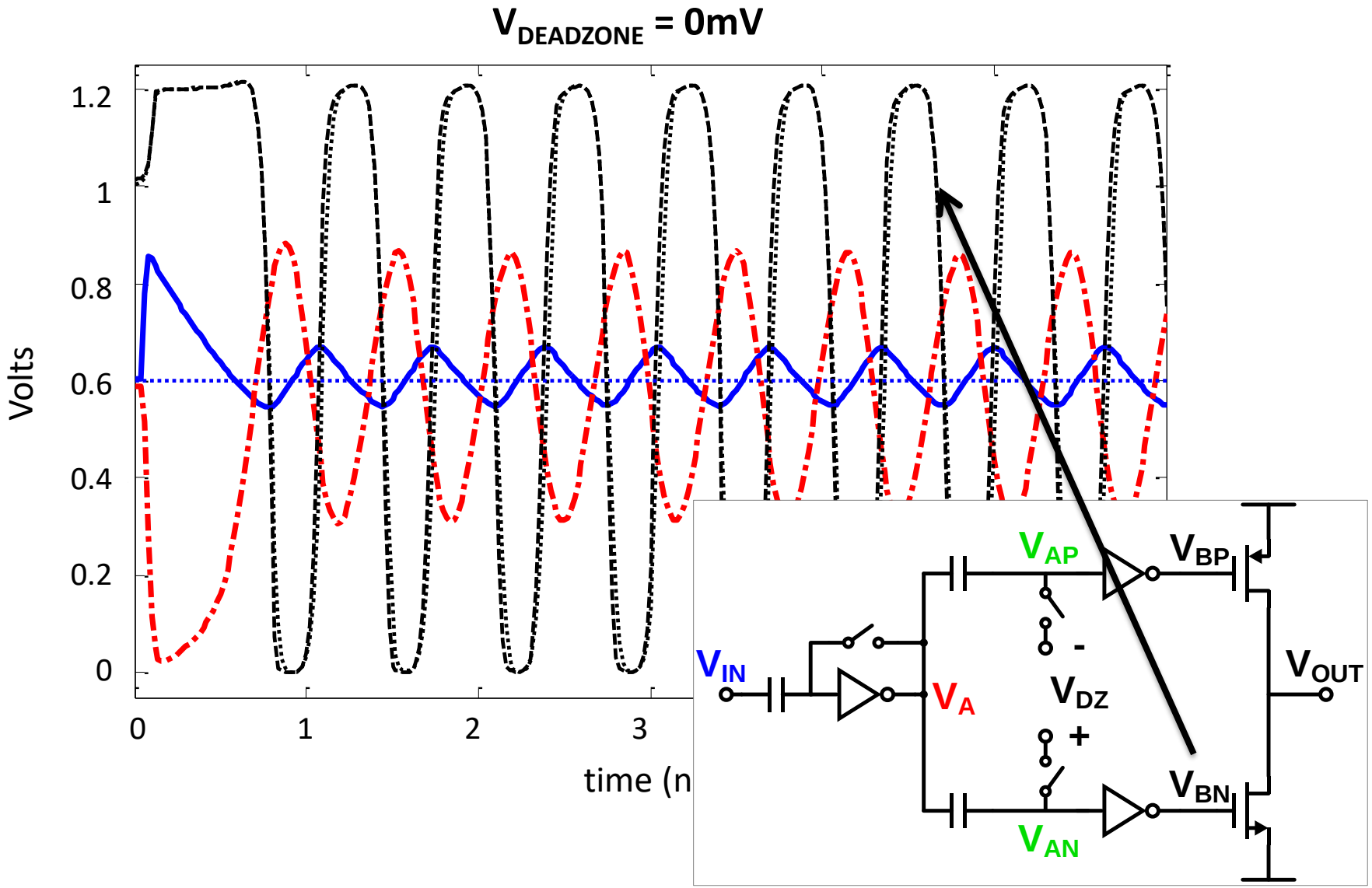

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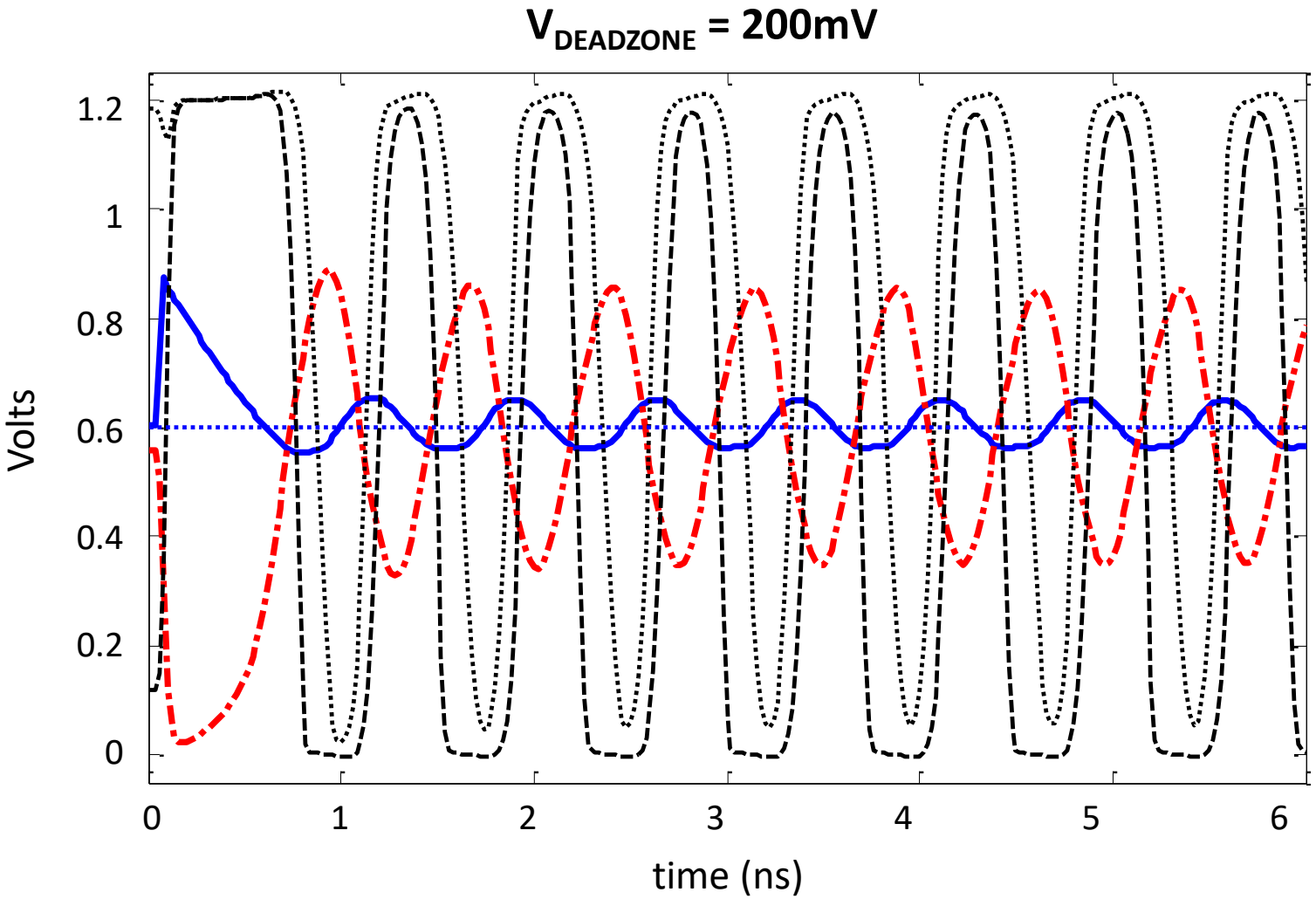

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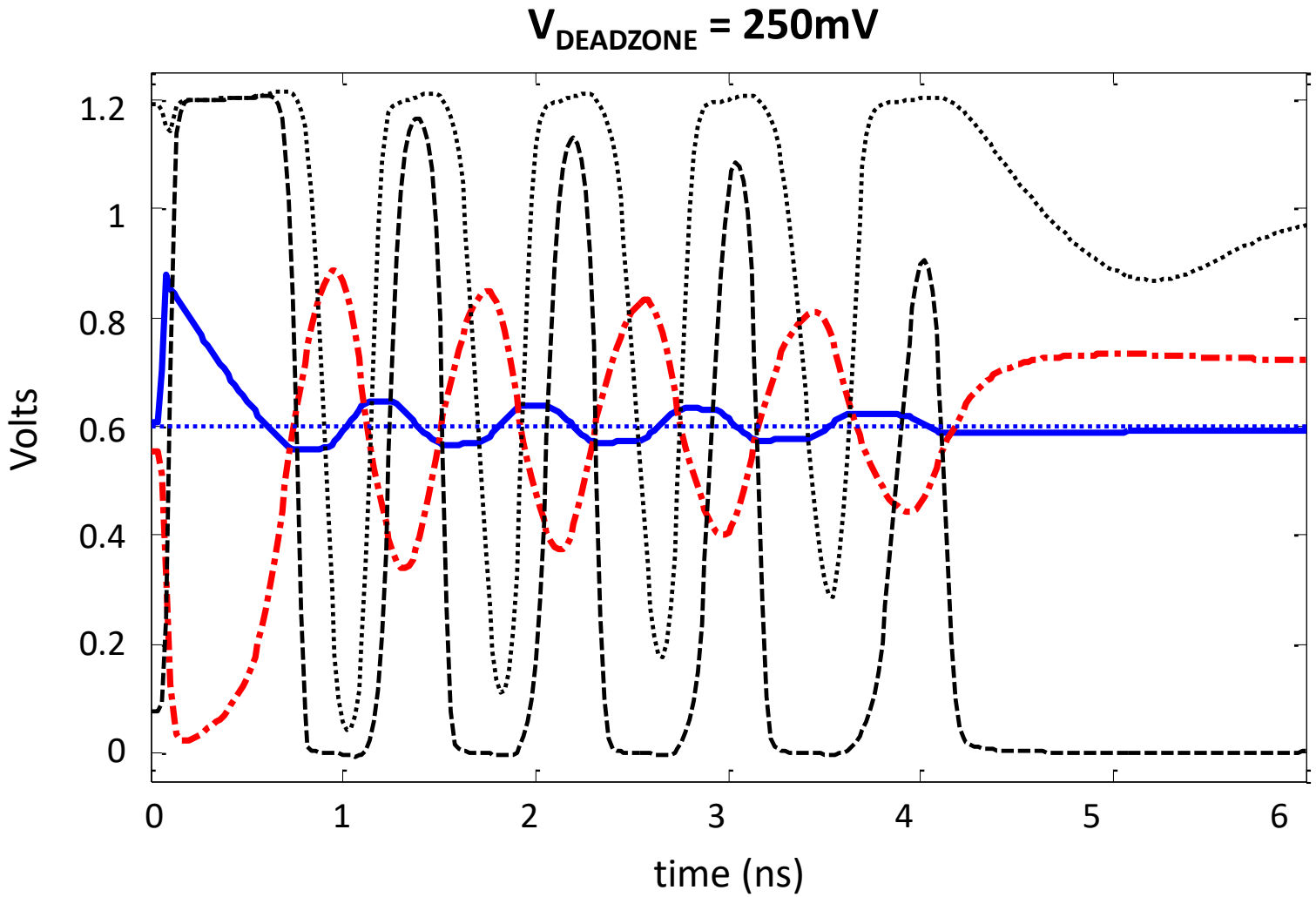

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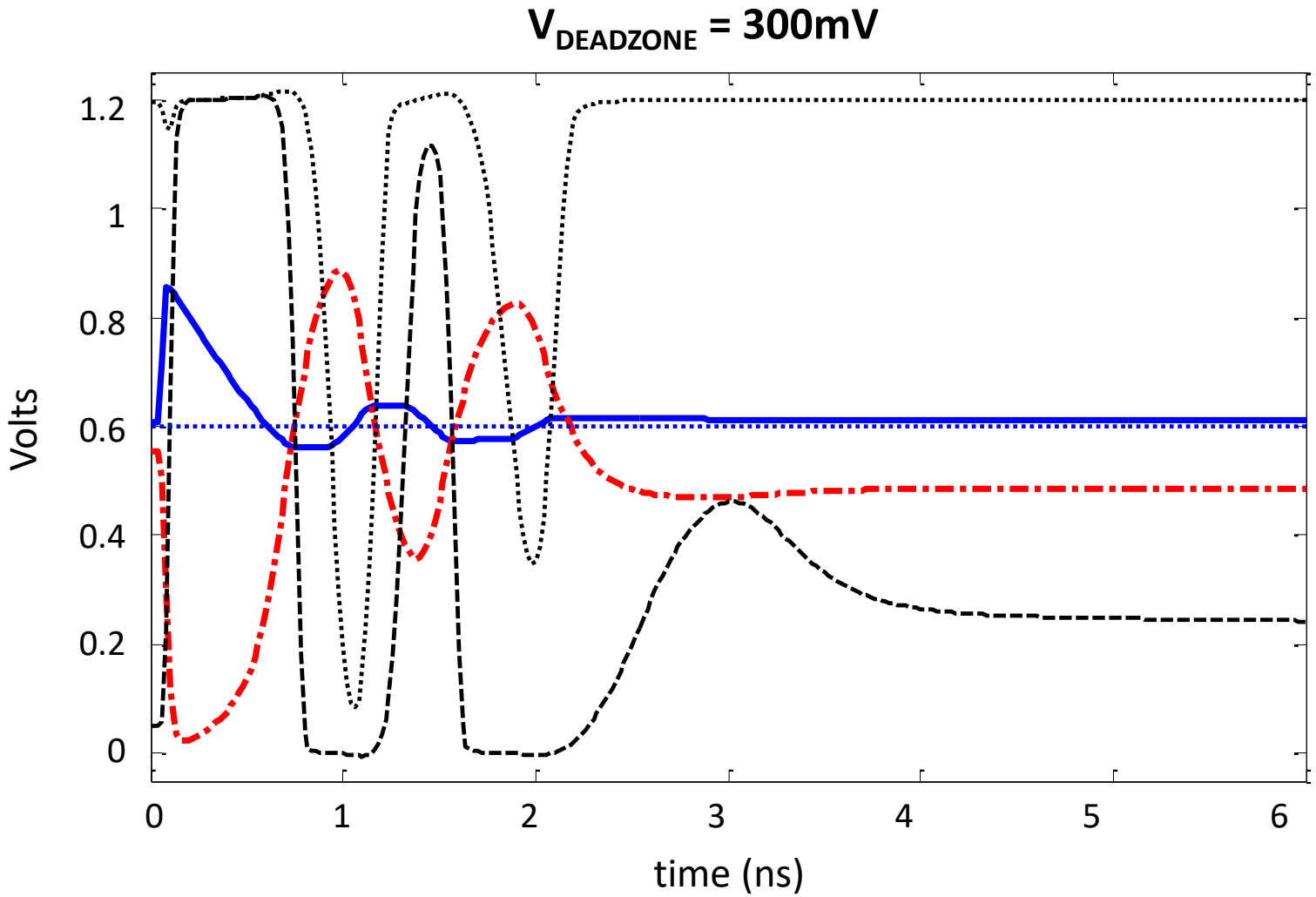

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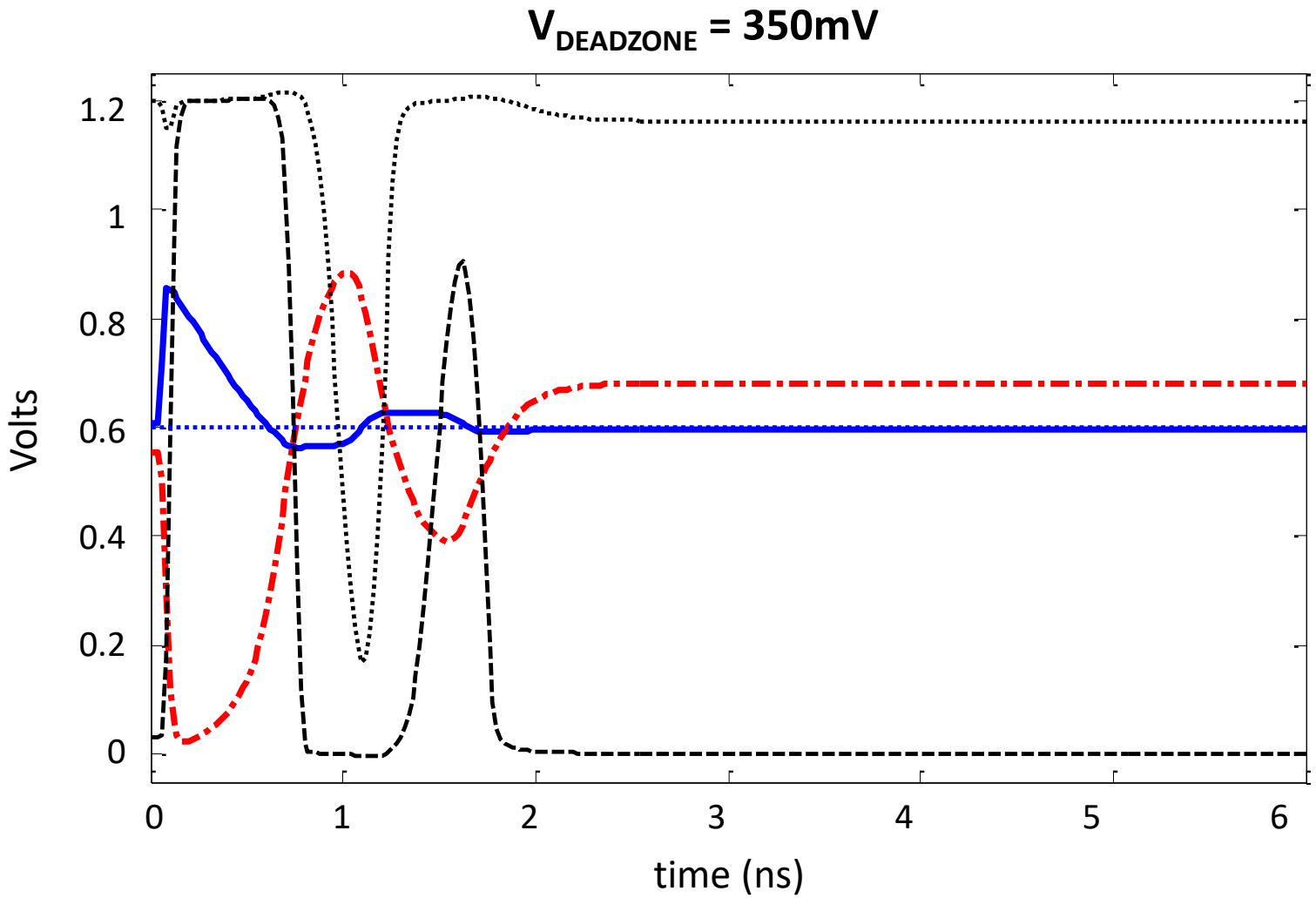

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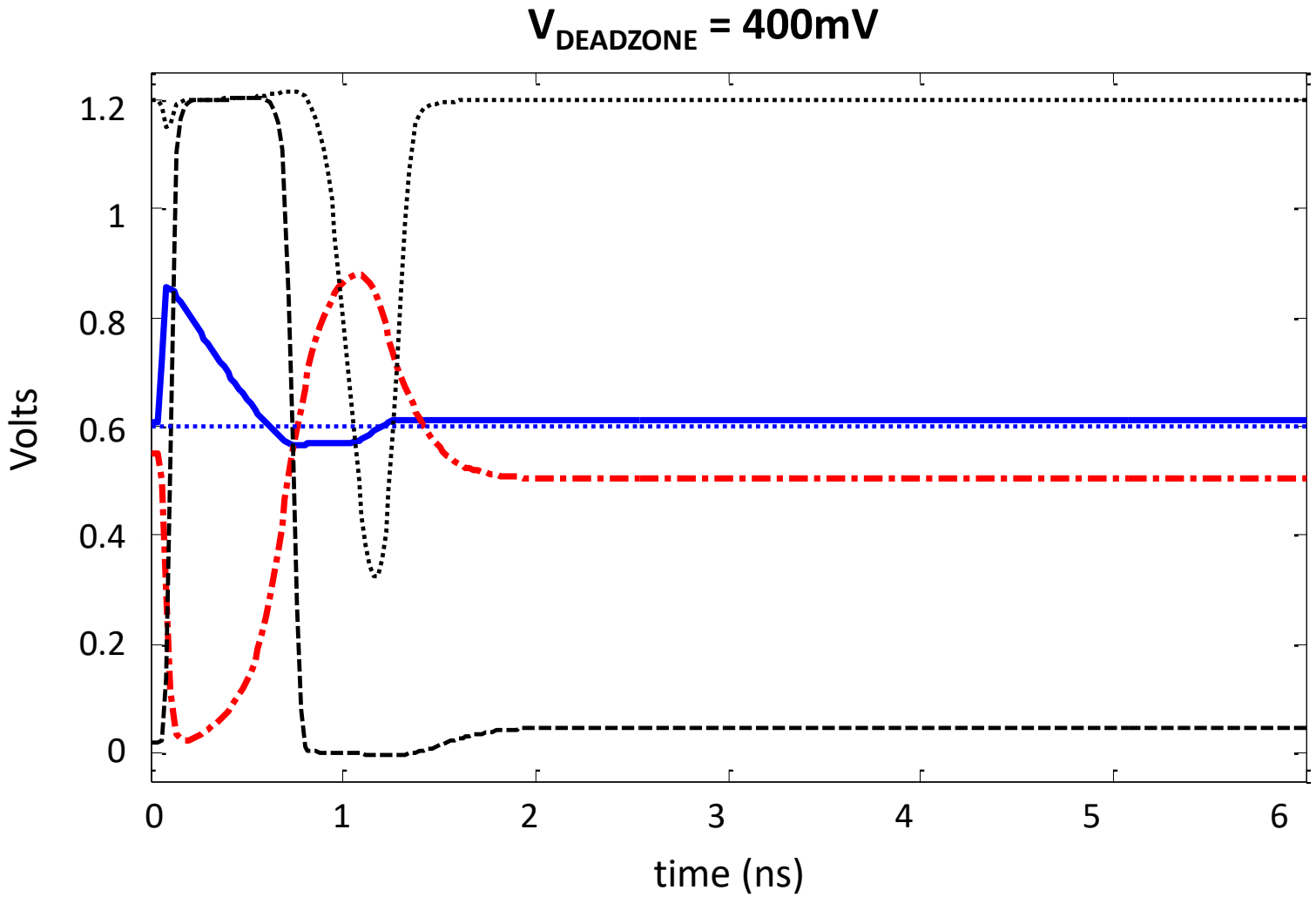
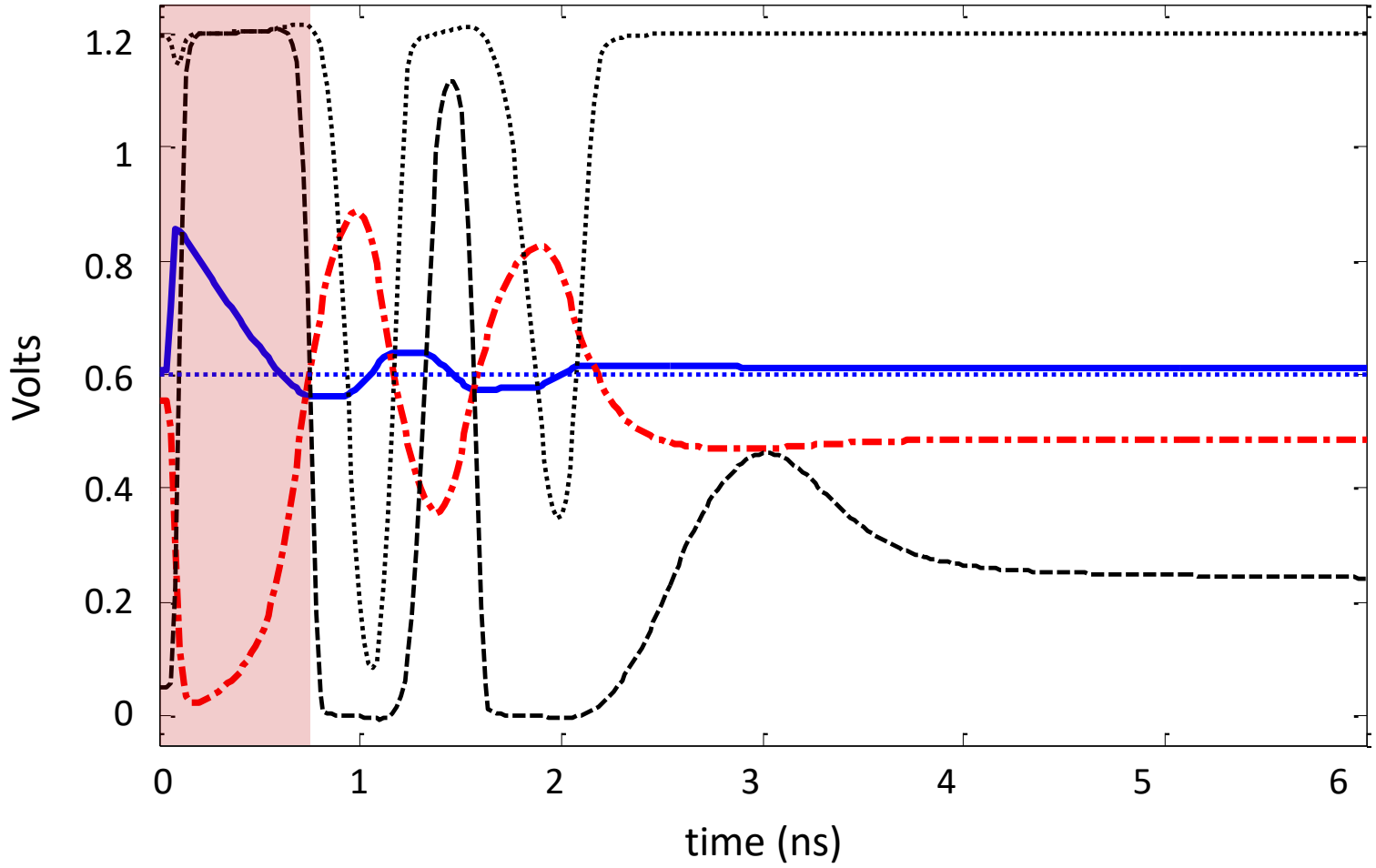


DYNAMIC LARGE-SIGNAL STABILIZATION

THREE OPERATION PHASES

- Slewing



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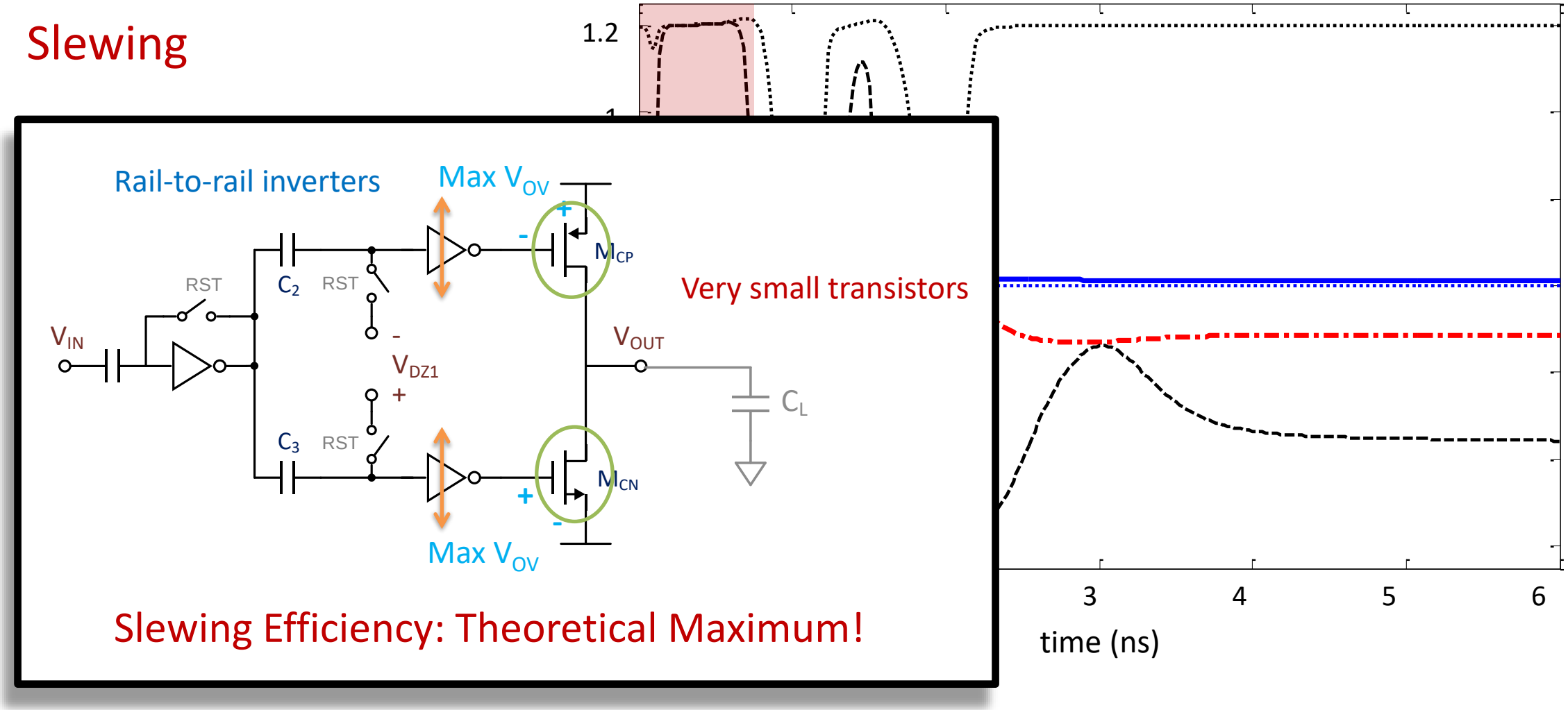

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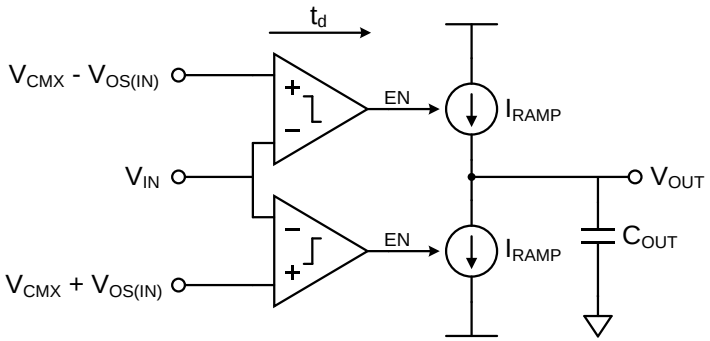
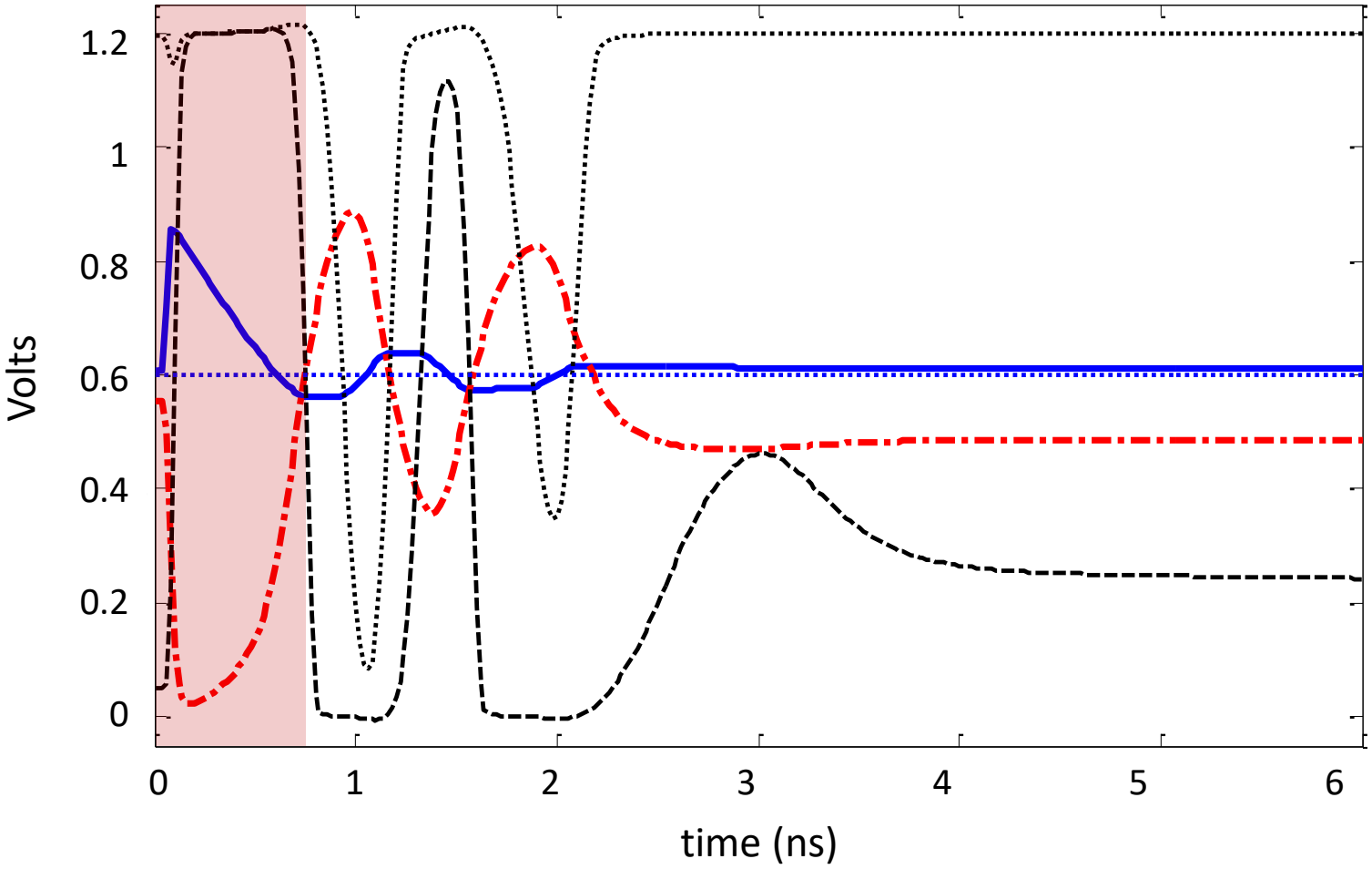


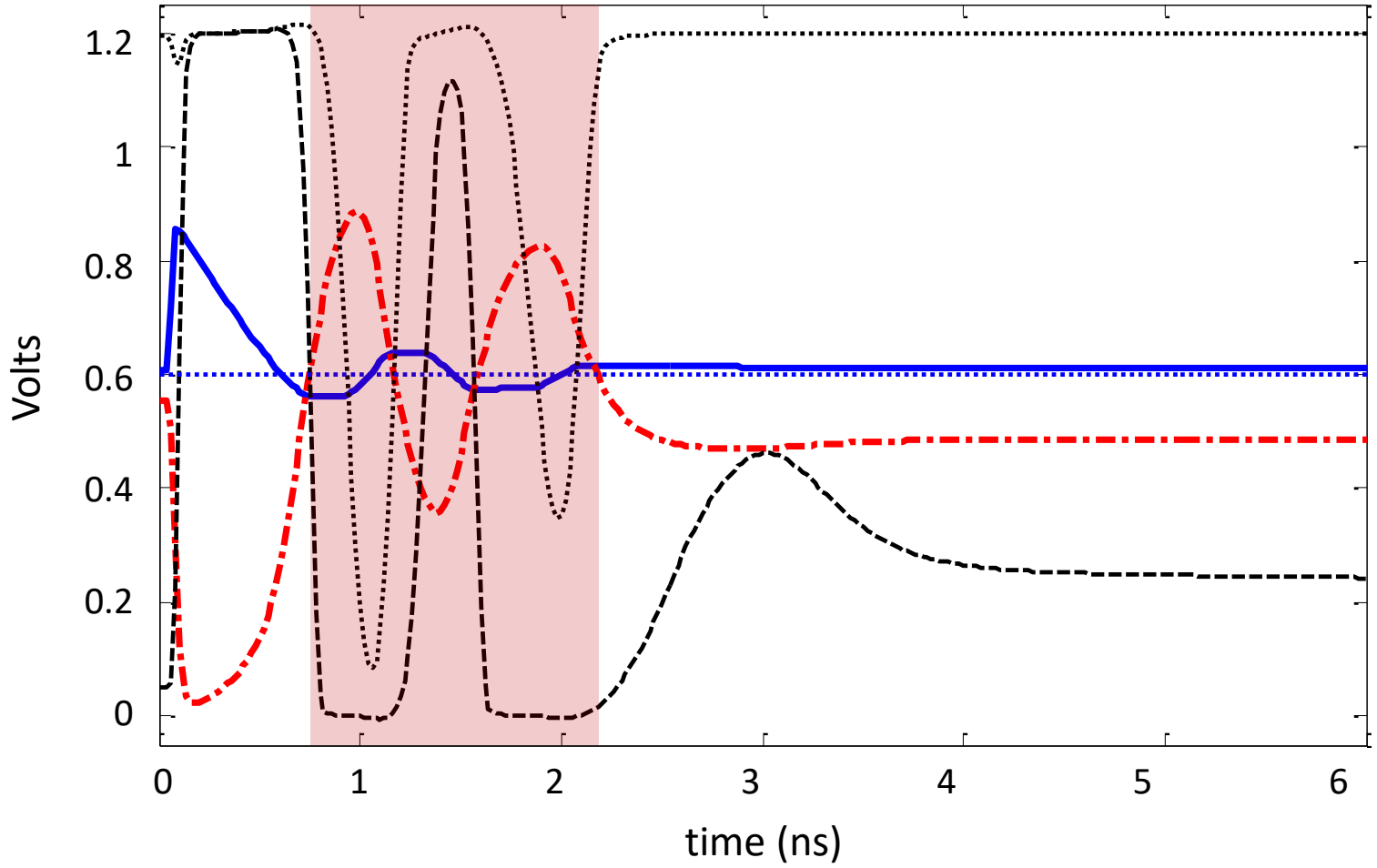
Acts like bi-directional switchable current source



DYNAMIC LARGE-SIGNAL STABILIZATION

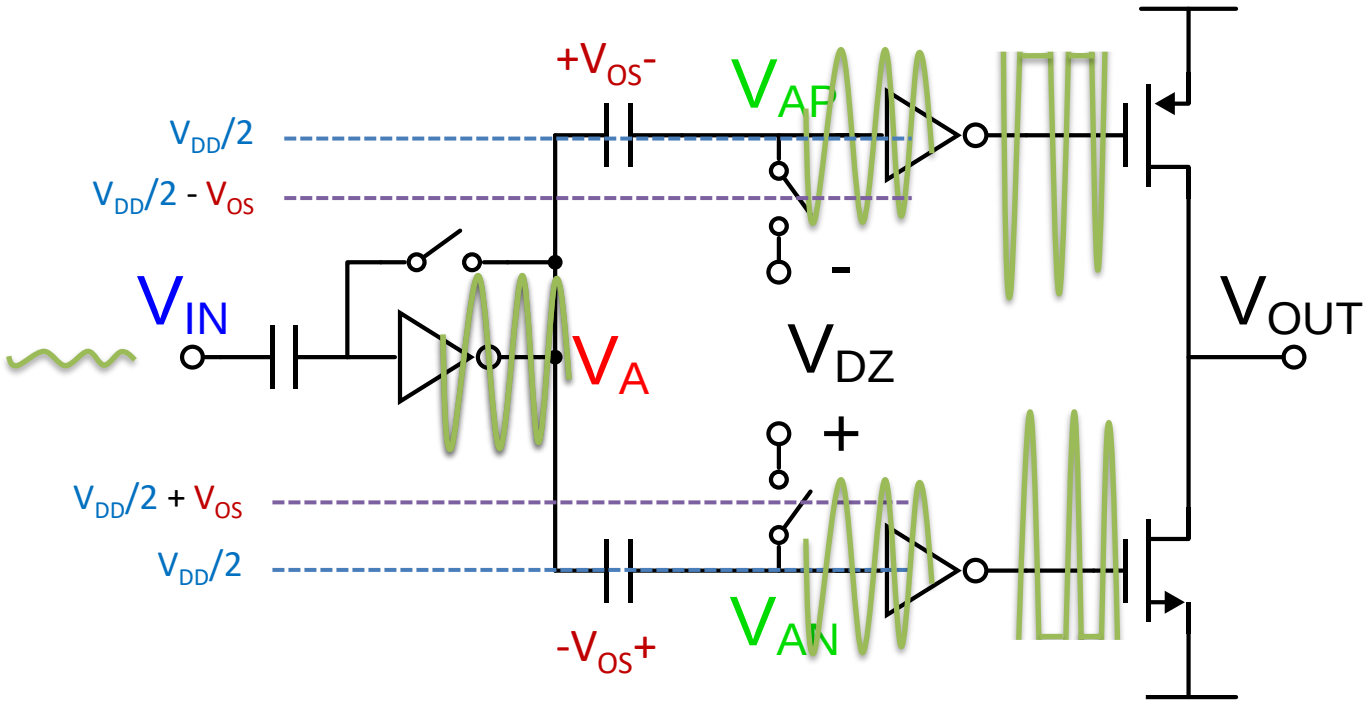
THREE OPERATION PHASES

- Slewing
- Stabilization



DYNAMIC LARGE-SIGNAL STABILIZATION

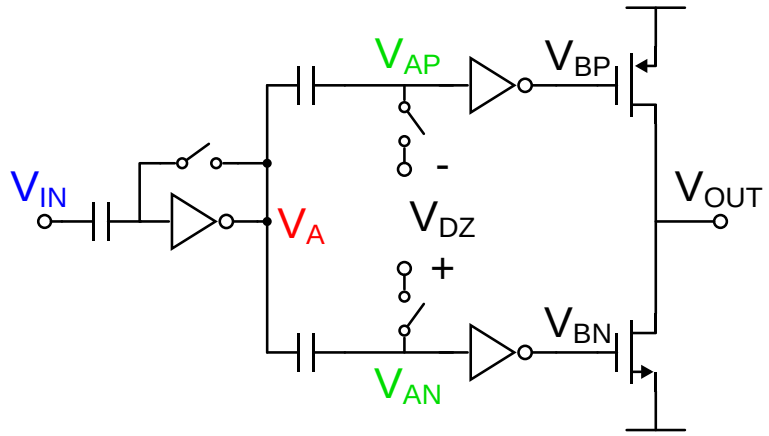
STABILIZATION



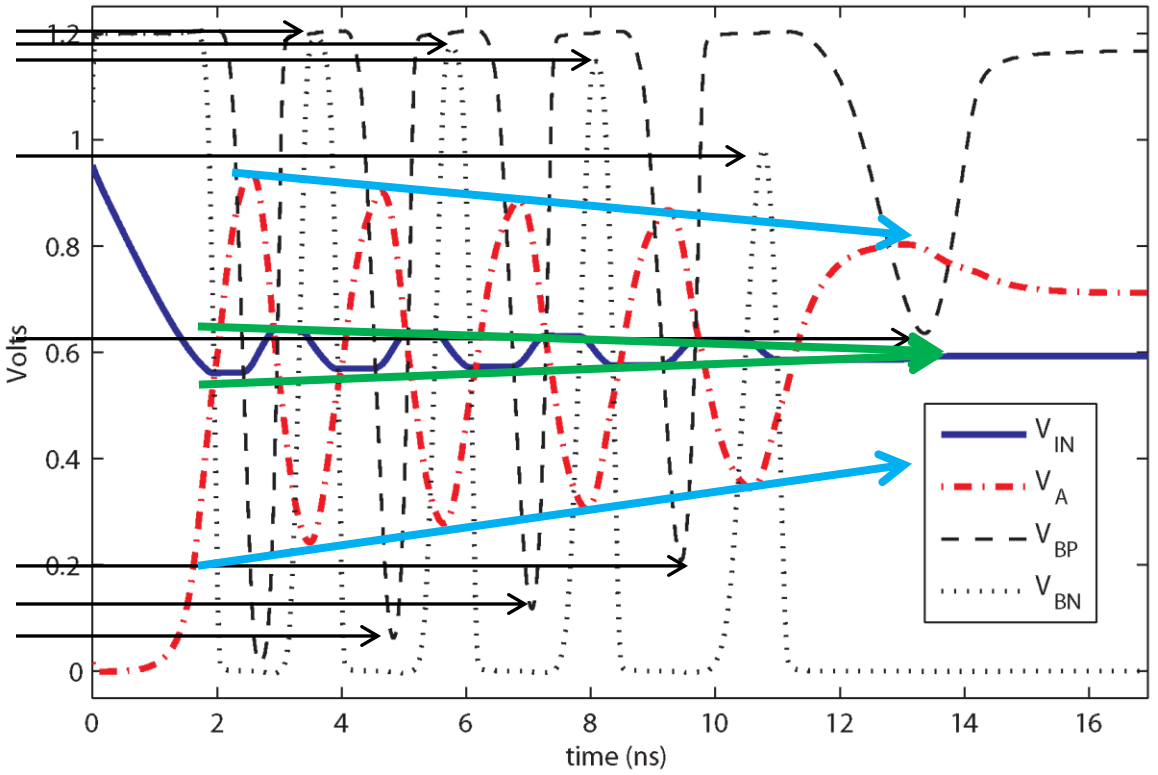
DYNAMIC LARGE-SIGNAL STABILIZATION

STABILIZATION

1. Reduced avg. overdrive voltage
2. Reduced output current
3. Reduced oscillation amplitude



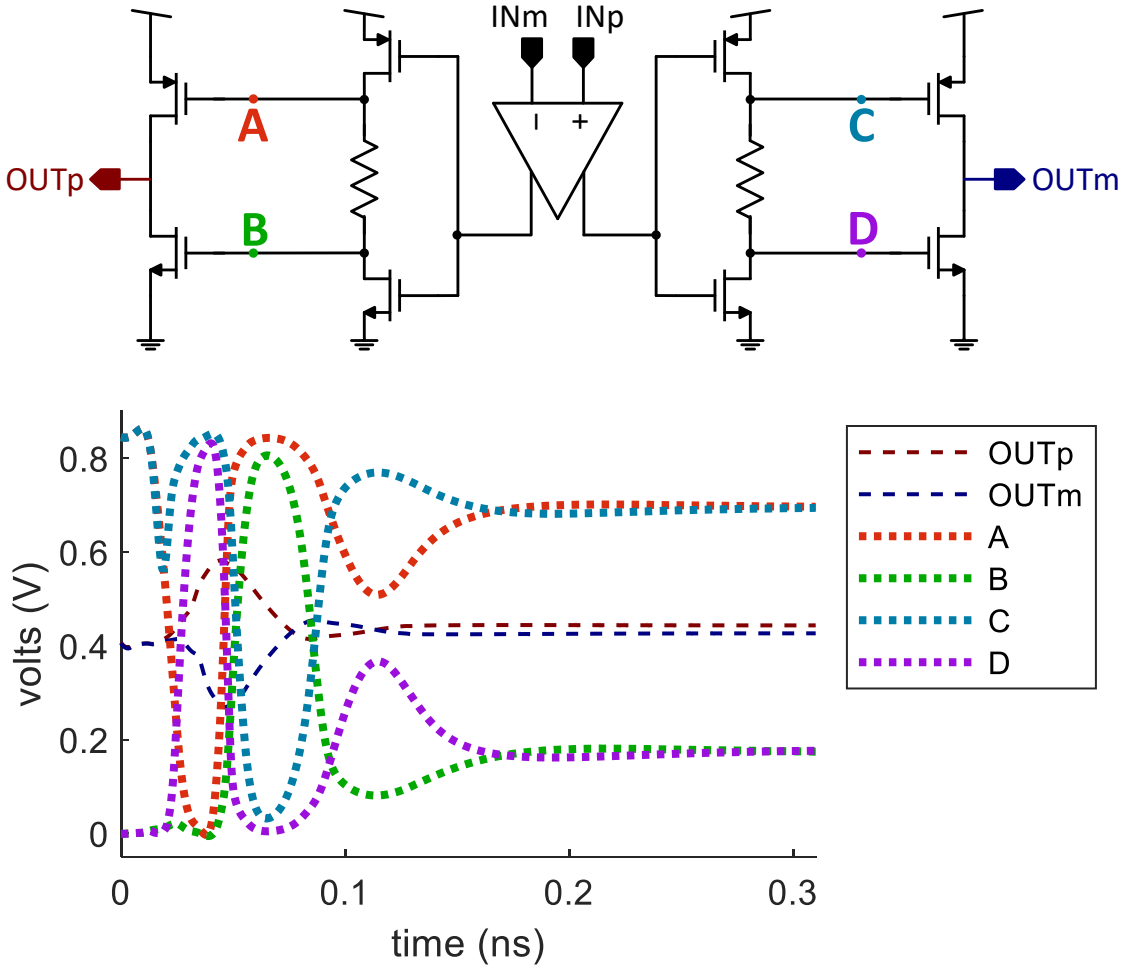
Example here: operation on the edge of stability



DYNAMIC LARGE-SIGNAL STABILIZATION

STABILIZATION (IN NANOSCALE)

- Modern example in 16nm FinFET CMOS
  - Less intrinsic gain
  - Different dynamic biasing mechanism (resistor)
  - Class-AB biasing (outputs in weak-inversion at steady-state)
- But fundamental idea & behavior still the same



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  - Less intrinsic gain
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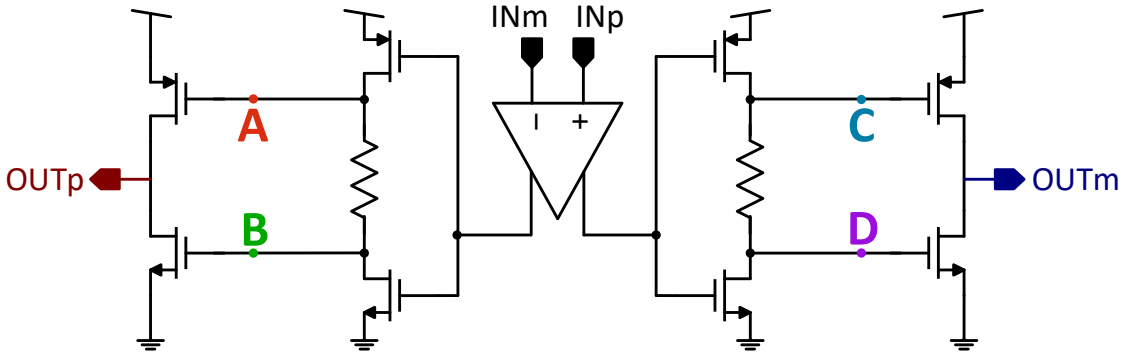
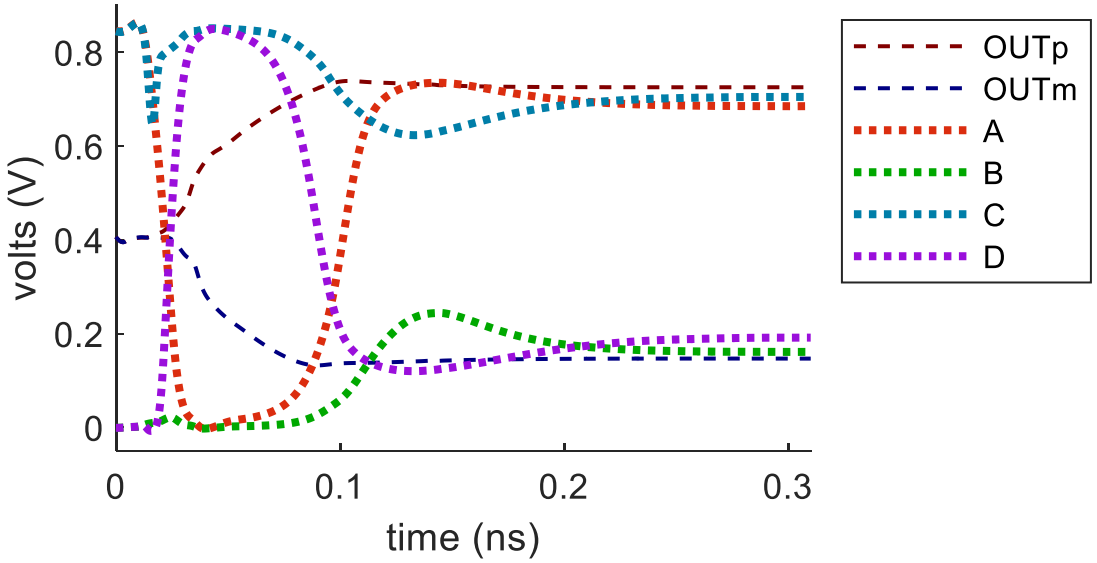
  - Class-AB biasing (outputs in weak-inversion at steady-state)
- But fundamental idea & behavior still the same
- V_{OUT} affects stability!
  - V_{DS} varies w.r.t. V_{OUT}
  - Thus, output pole location varies w.r.t. V_{OUT}

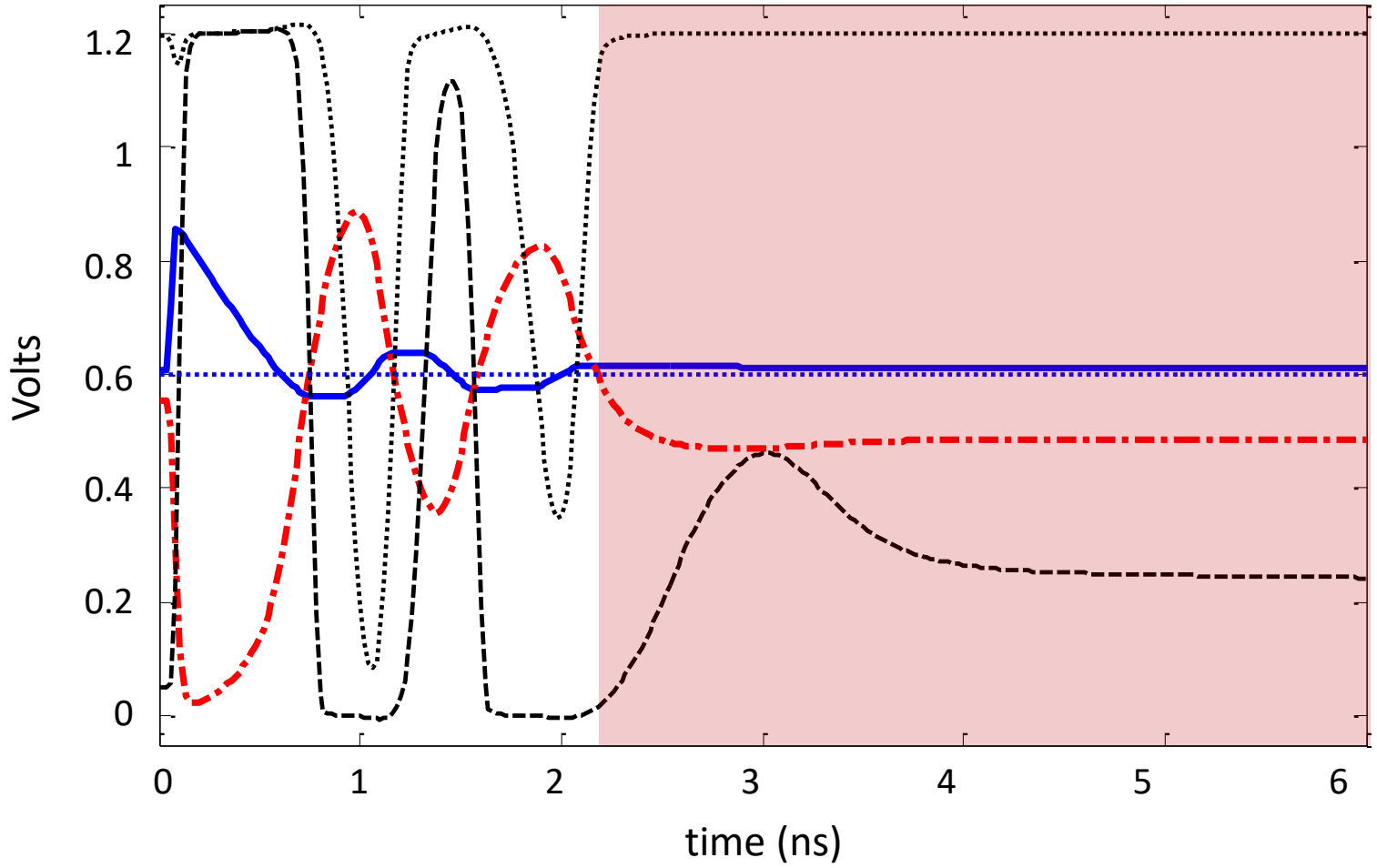




DYNAMIC LARGE-SIGNAL STABILIZATION

THREE OPERATION PHASES

- Slewing
- Stabilization
- Settling

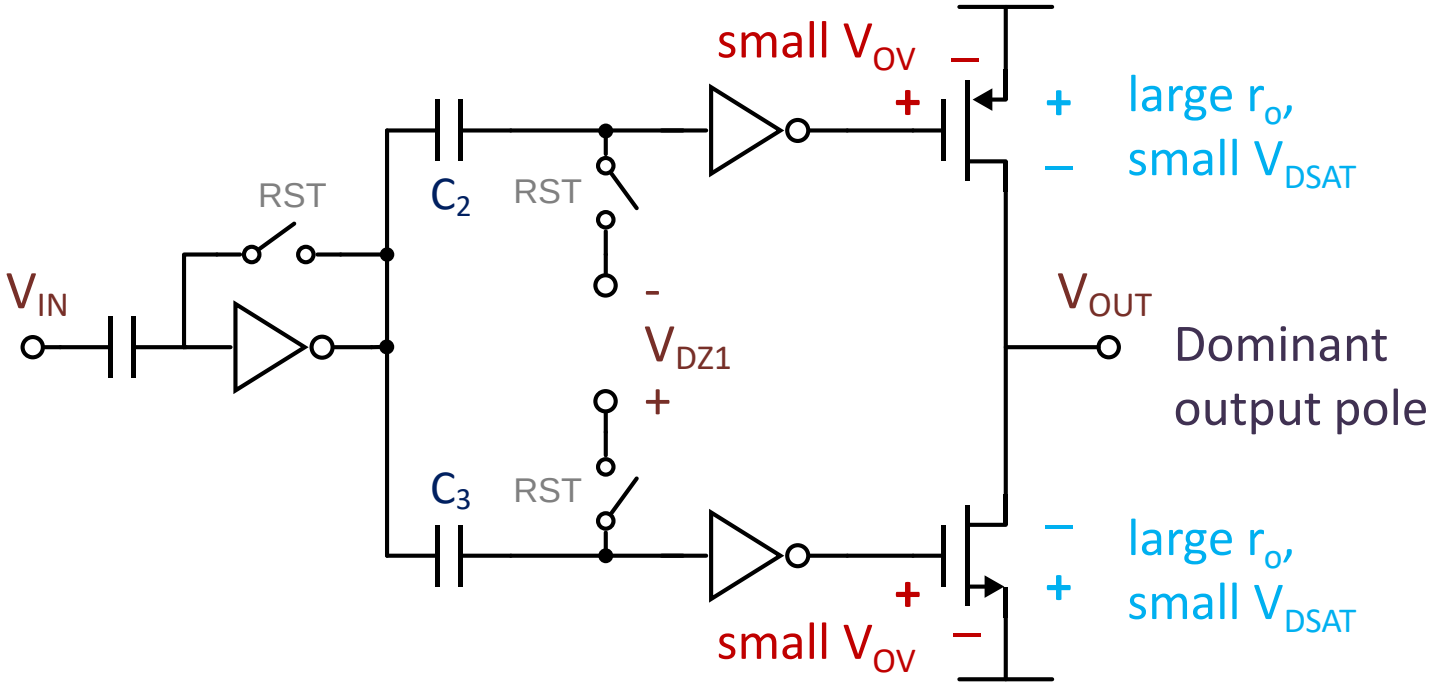


DYNAMIC LARGE-SIGNAL STABILIZATION

SETTLING

- Weak-inversion steady-state

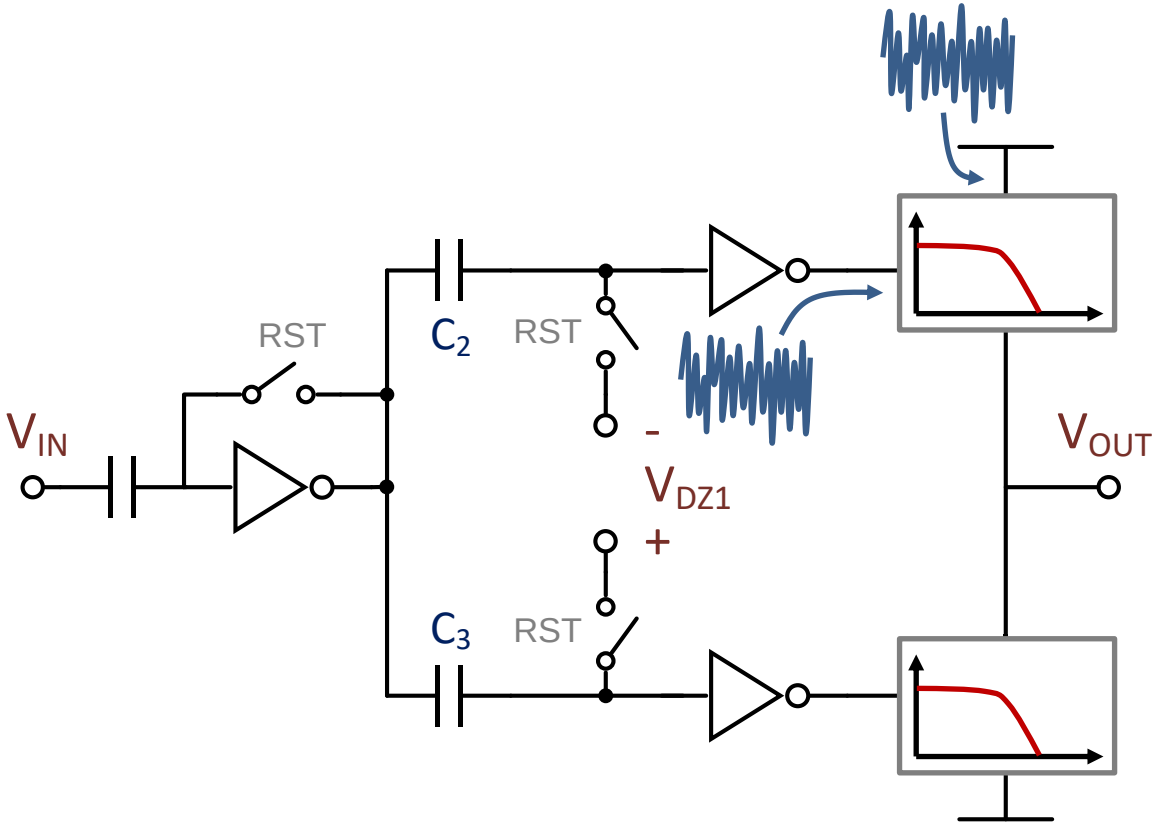
- Min V_{OV}
  - ☺ Low quiescent current
  - ☺ Noise filtering
- Min V_{DSAT}
  - ☺ Wide swing
  - ☺ High linearity
- Max r_o
  - ☺ High gain
  - ☺ High linearity



DYNAMIC LARGE-SIGNAL STABILIZATION

NOISE

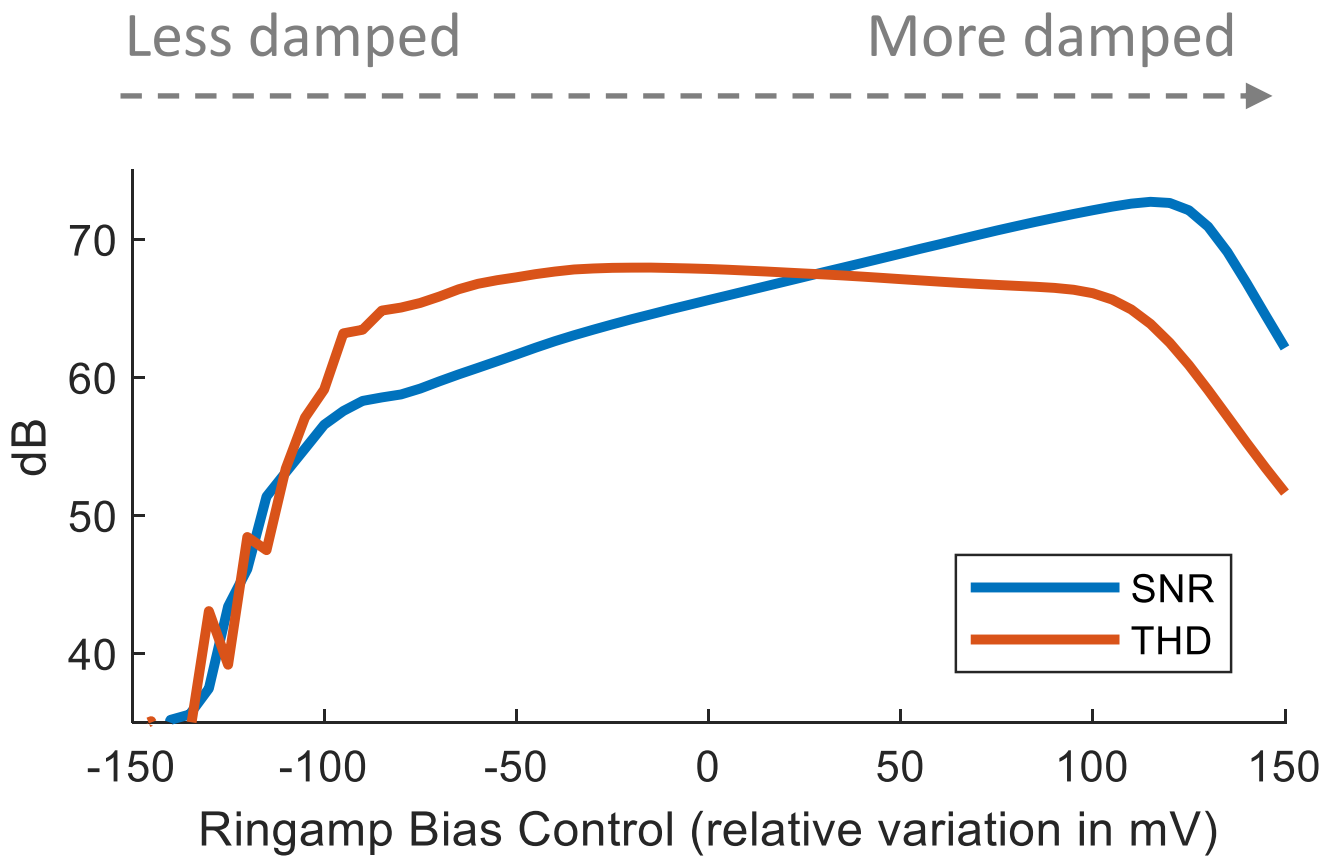
- Noise at output filtered by steady-state g_m
  - Internal noise
  - Supply noise
- With smart design, noise at least as good as opamp
  - But much faster
  - But much more efficient



DYNAMIC LARGE-SIGNAL STABILIZATION

NOISE

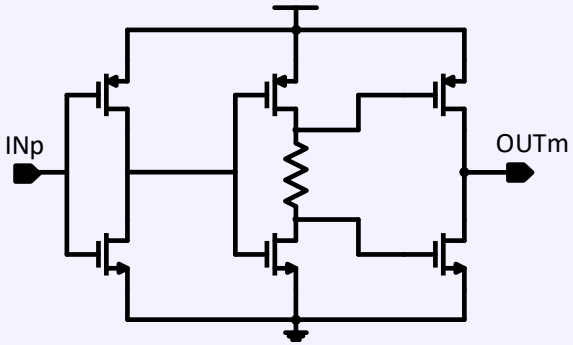
- SNR and THD may have different bias optimums
- Noise
  - Best when over-damped
  - lowest g_m for most filtering
- Linearity
  - Best when critically-damped
  - Fastest settling



THE “IDEAL AMPLIFIER” WISHLIST

So ... how did we do?

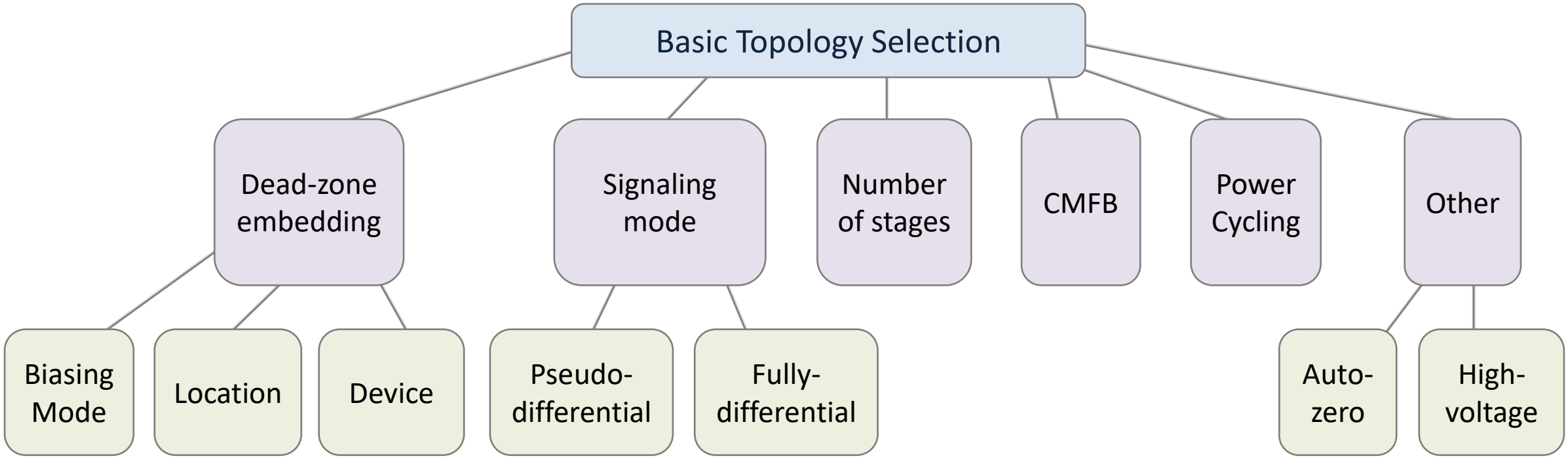
Ring Amplifier
(ringamp)



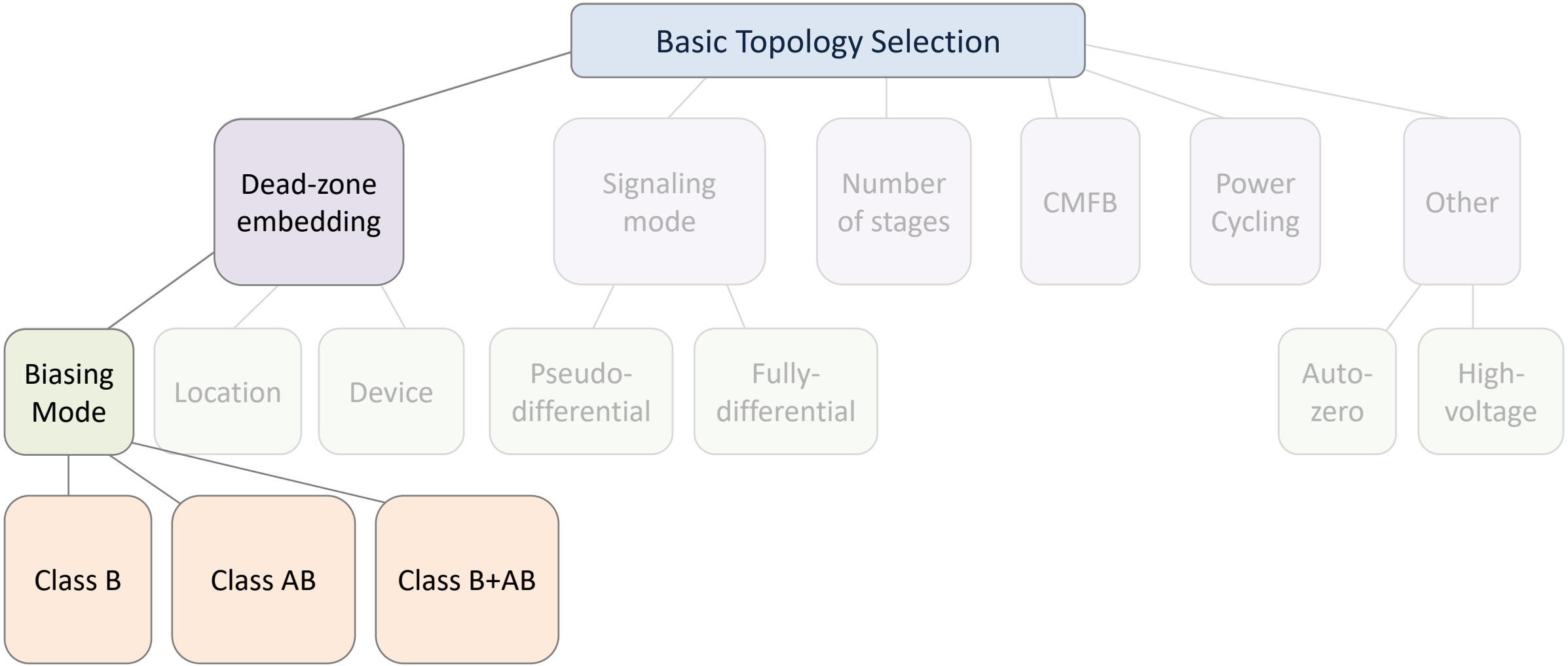
- High bandwidth
- Fast slewing
- Performance scales like digital CMOS
- class-AB
- Fully dynamic (switchable)
- High linearity
- High gain
- Low noise
- Rail-to-rail output swing
- Small area
- Low design effort

TOPOLOGY SELECTION

TOPOLOGY SELECTION



TOPOLOGY SELECTION



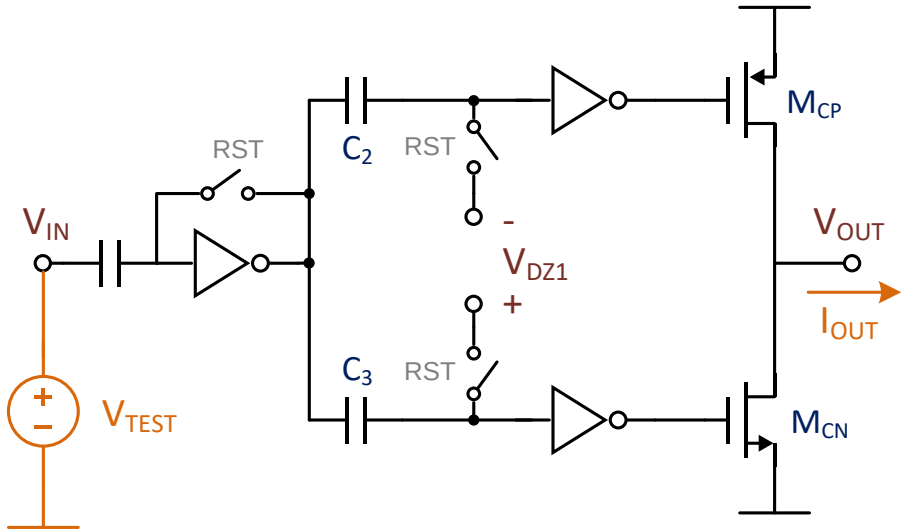
BIASING MODE

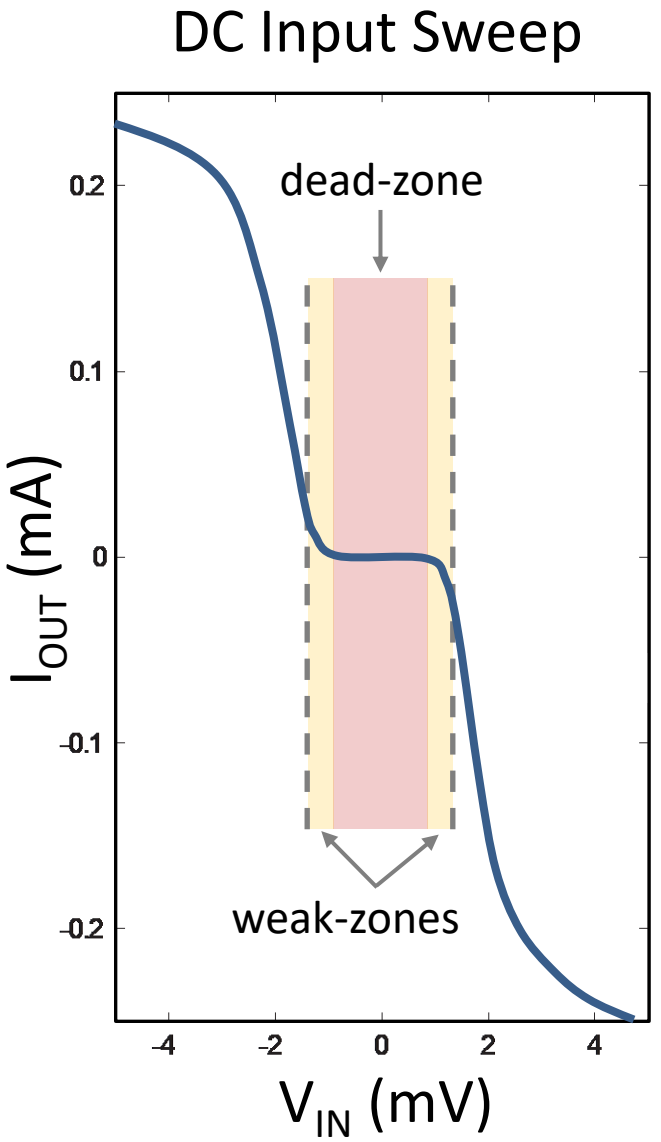
TOPOLOGY SELECTION

- Class-B
  - Sub-threshold “dead-zone”
  - Surrounded by “weak-zone”

☺ Fastest, most stable

☹ Dead-zone distortion





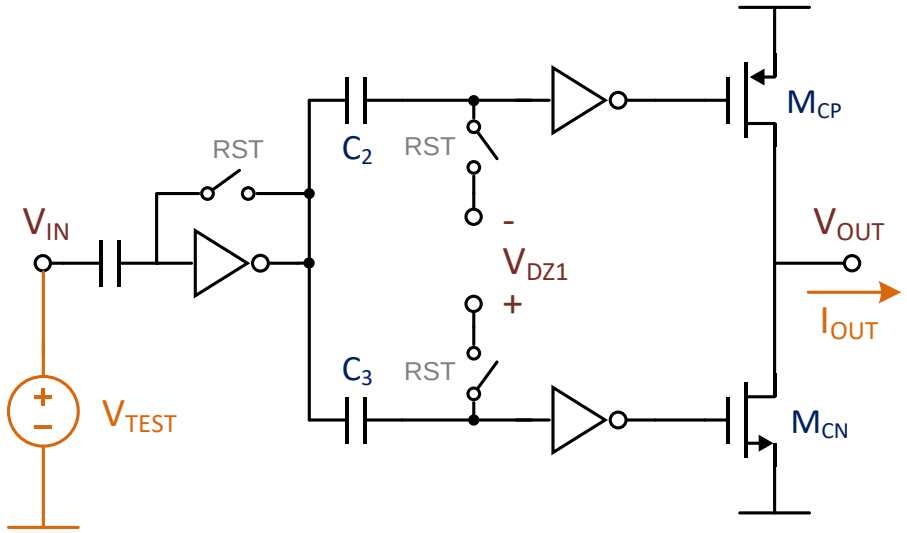
BIASING MODE

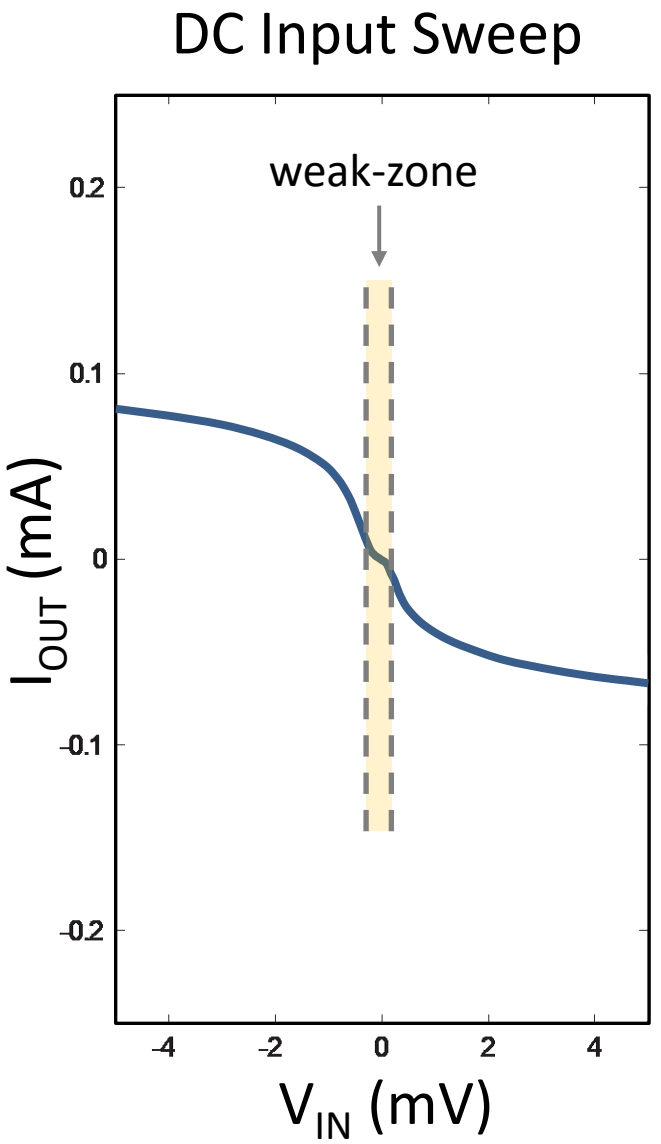
TOPOLOGY SELECTION

- Class-AB
  - Only “weak zone”
  - Always conducting

☺ Highest accuracy

☹ Slower

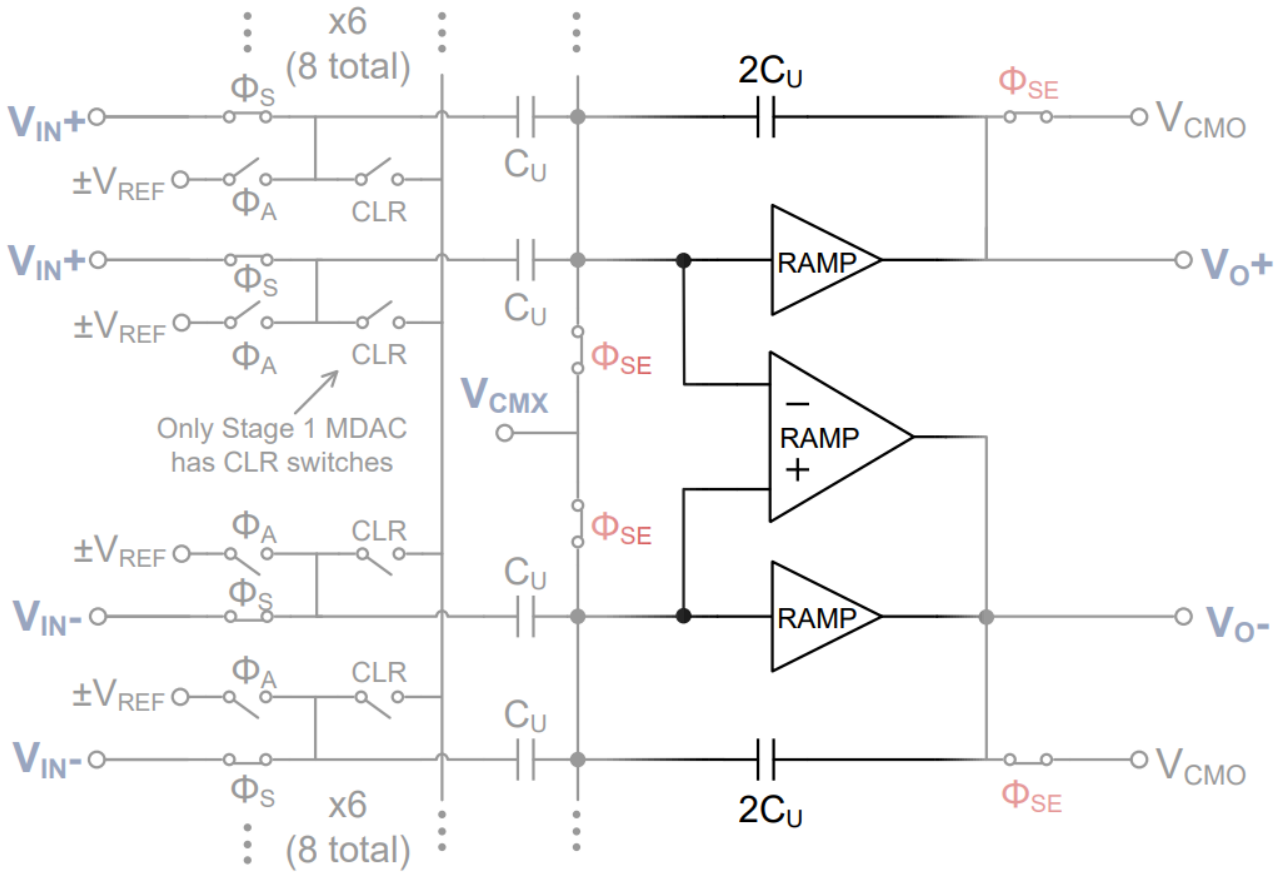




BIASING MODE

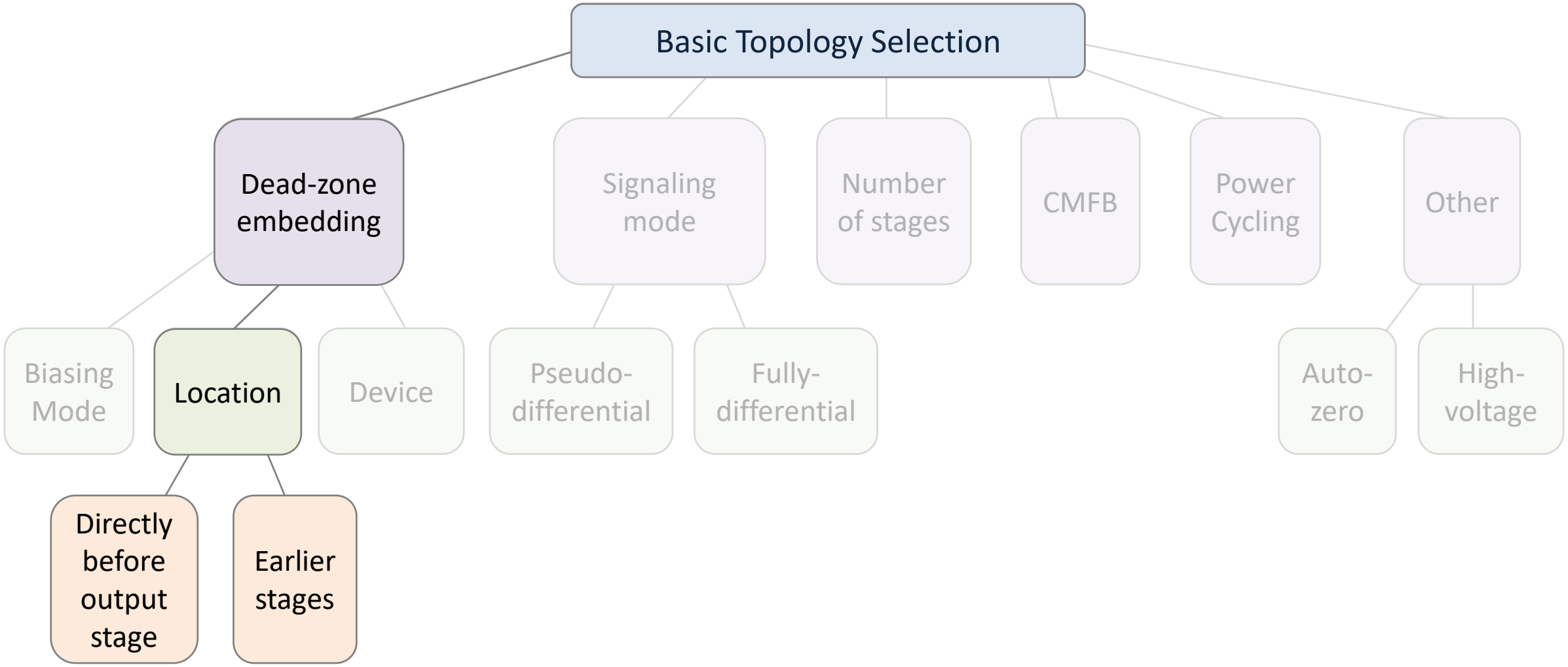
TOPOLOGY SELECTION

- Class-B + AB
  - Class-B coarse charge
  - Class-AB fine settle



[Hershberg, VLSI 2013]

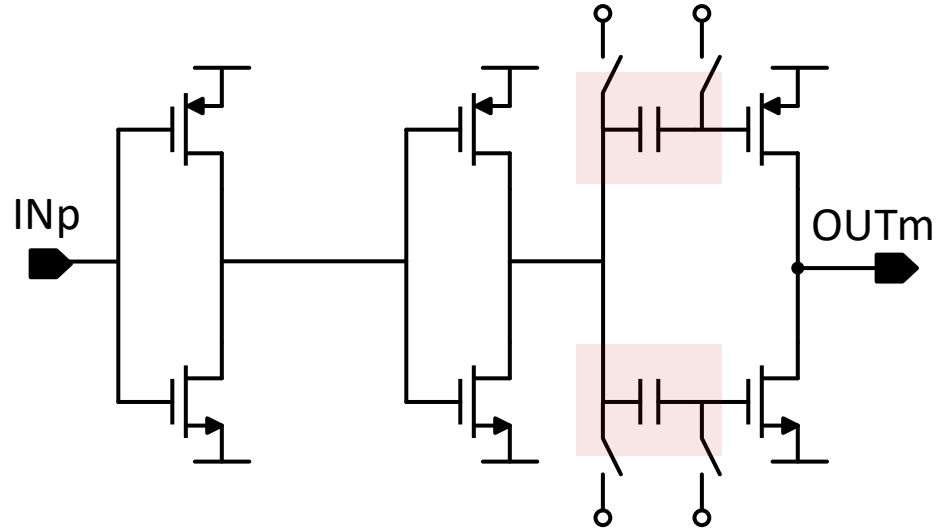
TOPOLOGY SELECTION



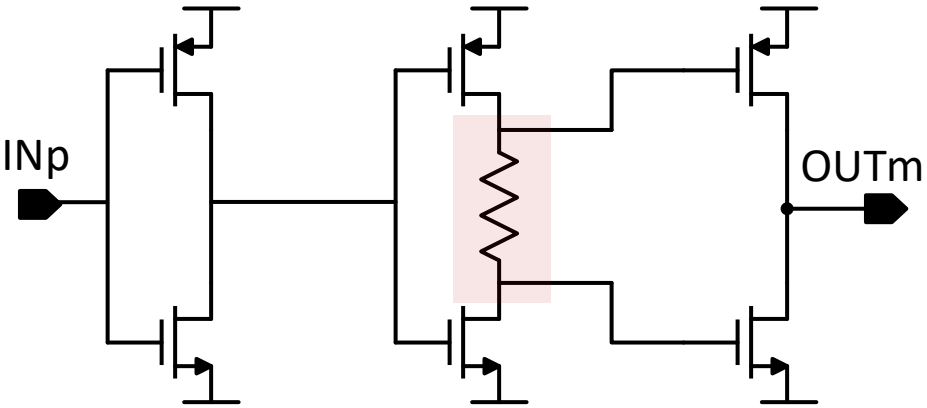
EMBEDDING LOCATION

TOPOLOGY SELECTION

- Directly before output stage
  - Precise control of output stage biasing
- Best for:
  - Class-AB operation
  - High accuracy & linearity
  - Low gain technologies
  - Nanoscale CMOS 👍



[Hershberg, VLSI 2013]

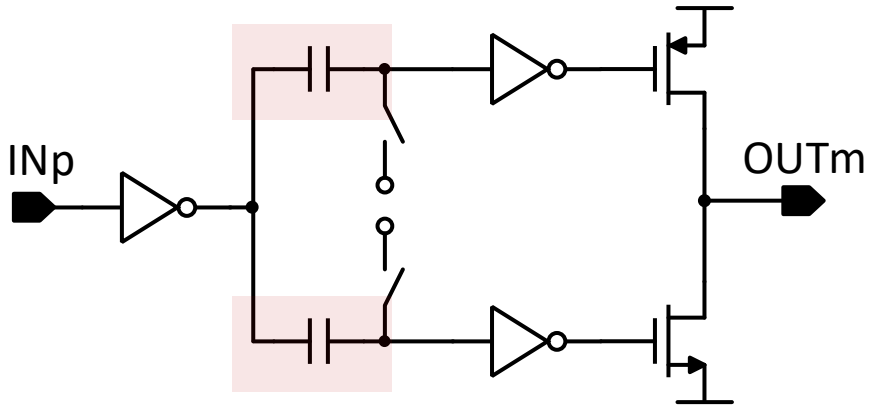


[Lim, JSSC Oct. 2015]

EMBEDDING LOCATION

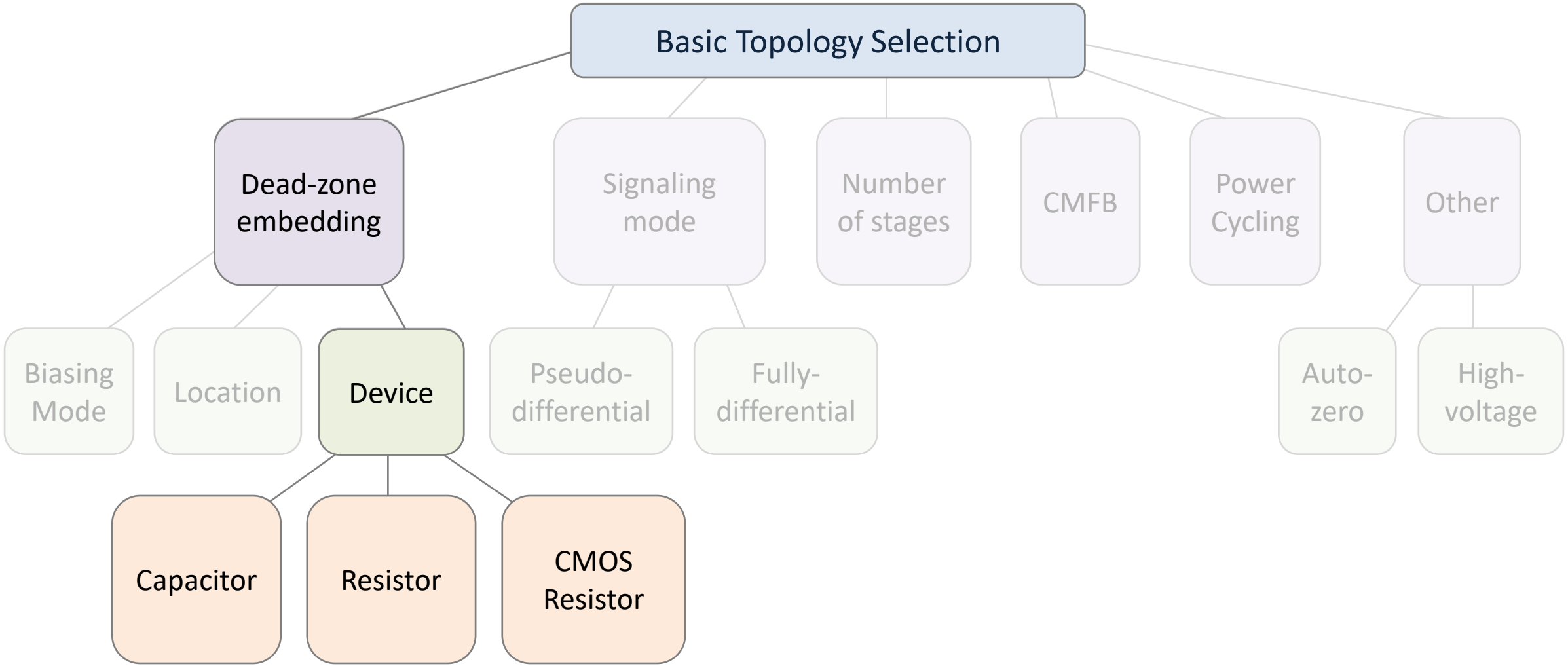
TOPOLOGY SELECTION

- Before second-to-last stage
  - Decouples stability from large signal biasing of output stage
- Best for:
  - Class-B operation
  - High speed
  - Coarse charging



[Hershberg, JSSC 2012]

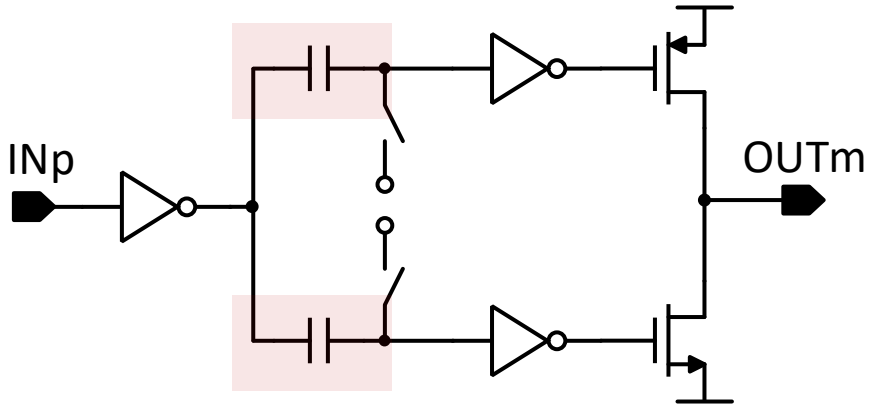
TOPOLOGY CHOICES



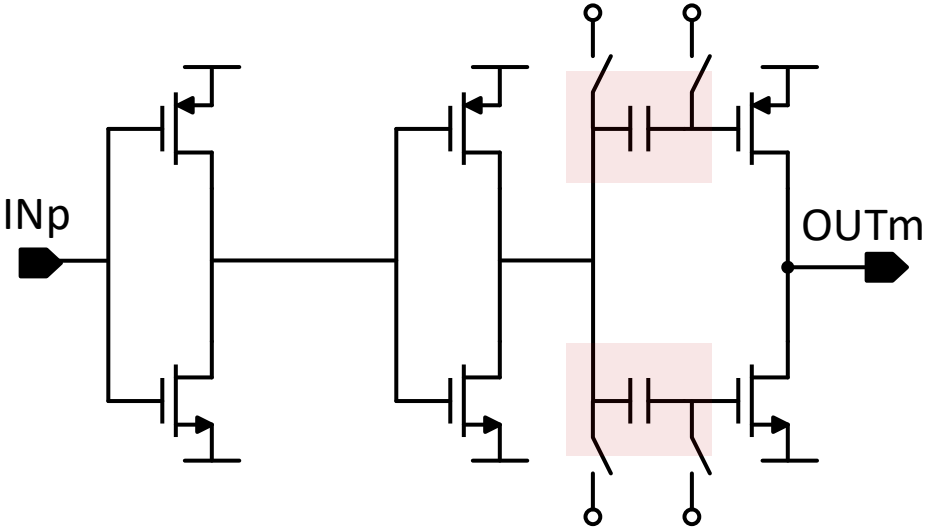
CAPACITOR EMBEDDING

TOPOLOGY SELECTION

- Direct voltage-mode control
- Best for
  - Class-B biasing
  - High-voltage applications
- Limitations
  - If embedding in last stage, will reduce max slewing efficiency



[Hershberg, JSSC 2012]

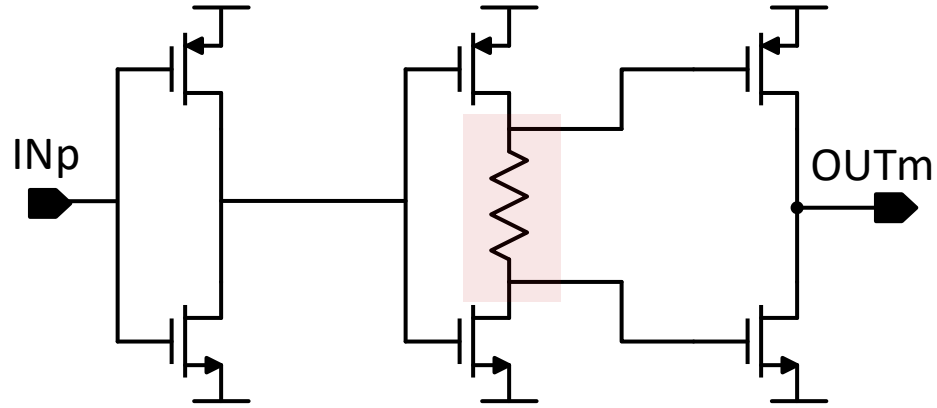


[Hershberg, VLSI 2013]

RESISTOR EMBEDDING

TOPOLOGY SELECTION

- Dynamically creates offset during stabilization
- Best for
  - PVT robust design
  - Nanoscale CMOS
  - Slewing efficiency
- Limitations
  - Speed problems if large V_{DZ} offset needs to be embedded



[Lim, JSSC Oct. 2015]

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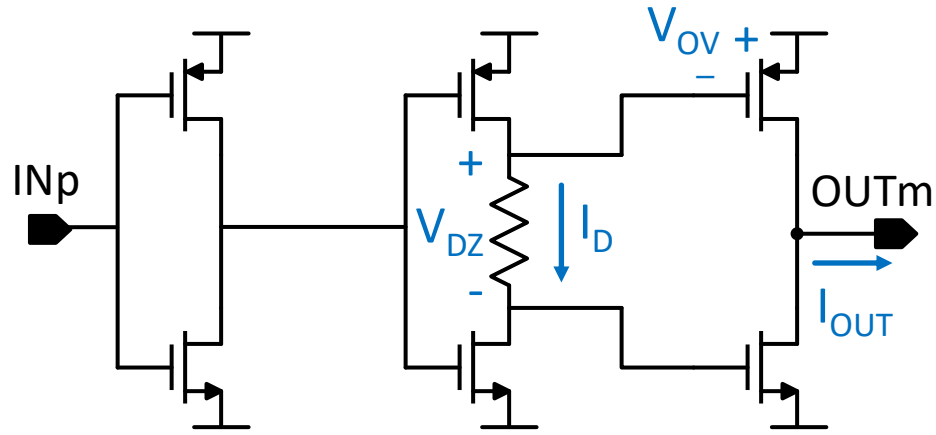

[Lim, JSSC Oct. 2015]

If V_{DD} increases → I_D increases → V_{DZ} increases → I_{OUT} stable

If Temp decreases → I_D increases

RESISTOR EMBEDDING

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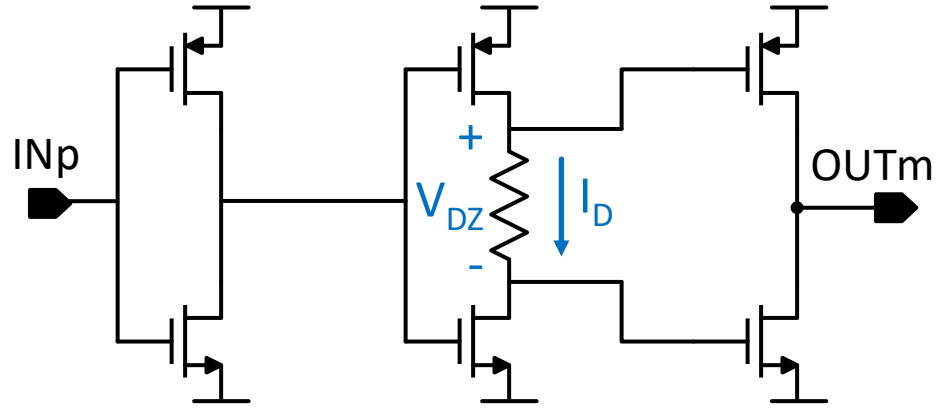
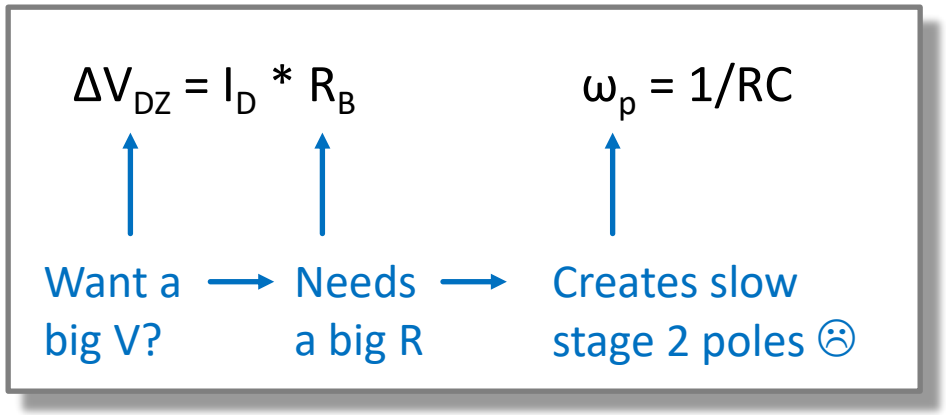


[Lim, JSSC Oct. 2015]



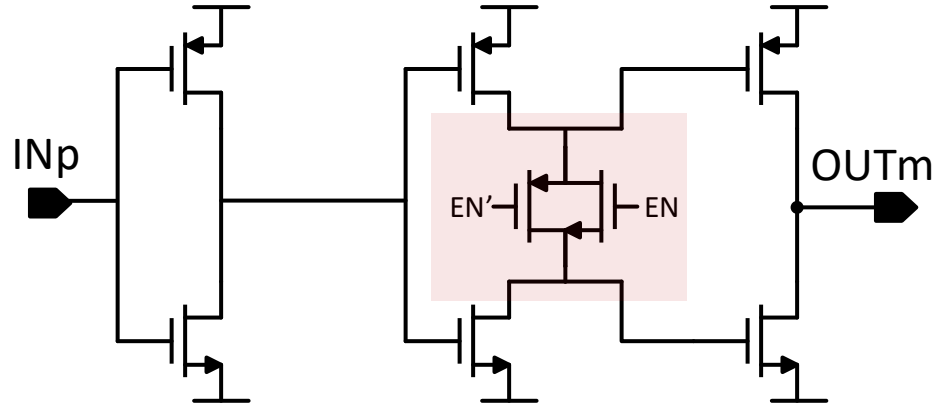
CMOS RESISTOR EMBEDDING

TOPOLOGY SELECTION

- Tunable on-state resistance
- Switchable (off-state)

- Best for
  - Power-cycling
  - Optimal biasing
  - Nanoscale CMOS

- Limitations
  - Less PVT robust than static resistor

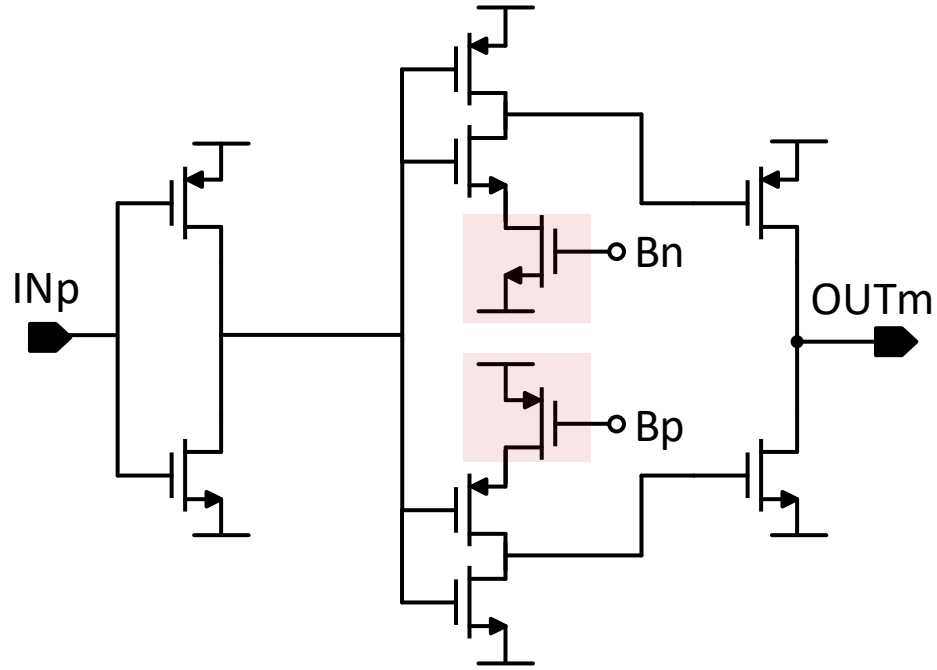


[Lagos, JSSC Feb. 2019]

OTHER EMBEDDINGS

TOPOLOGY SELECTION

- Current starved inverters
- Best for
  - Dynamic control
  - Analog PVT tracking schemes
- Limitations
  - Slower (lowers 2nd stage output poles)



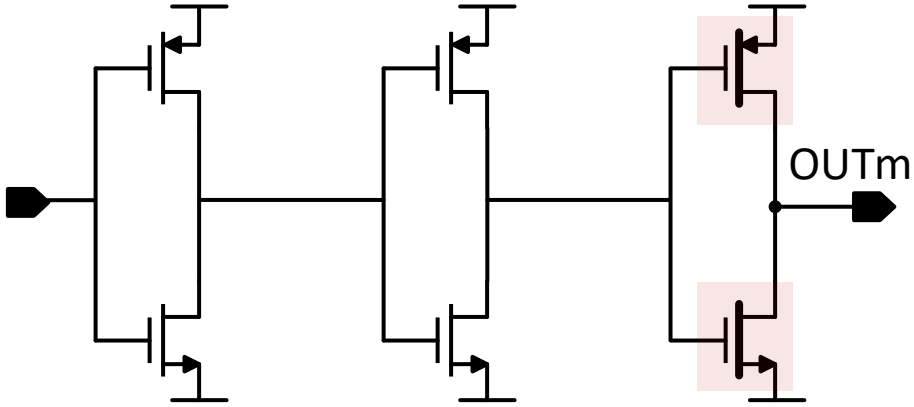
[Hershberg, PhD Thesis 2012]

[Leuenberger, CICC 2017]

OTHER EMBEDDINGS

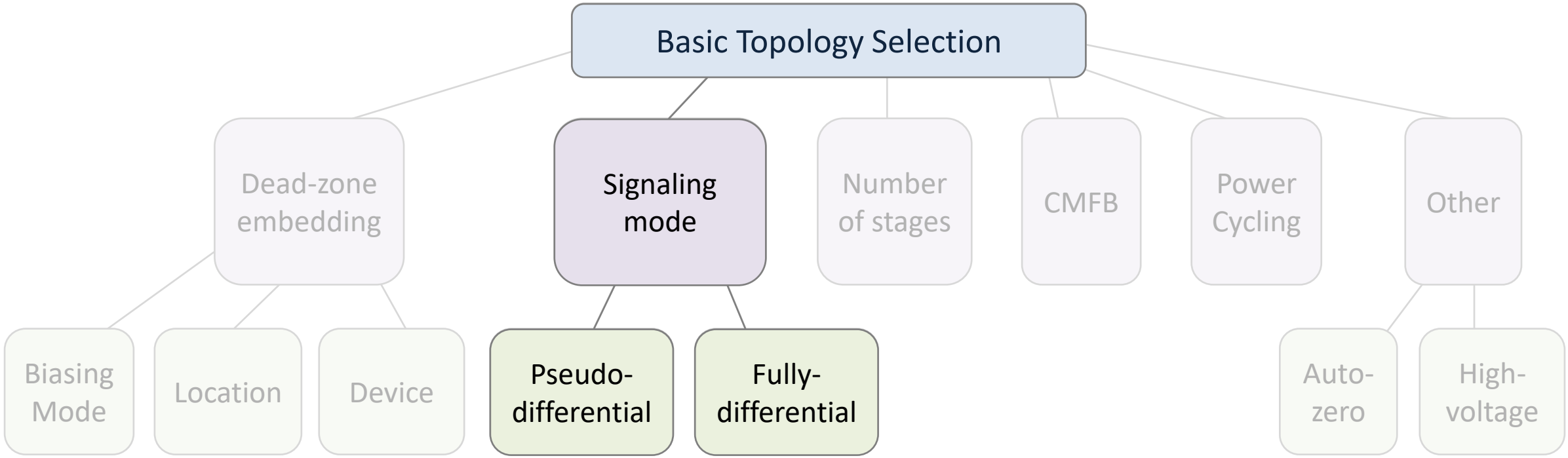
TOPOLOGY SELECTION

- Threshold voltage of output stage
- Best for
  - Low supply voltages
  - High speed
  - Simplicity
  - Area
- Limitations
  - PVT variation
  - Not with high supply voltages



[Lim, JSSC Oct. 2015]

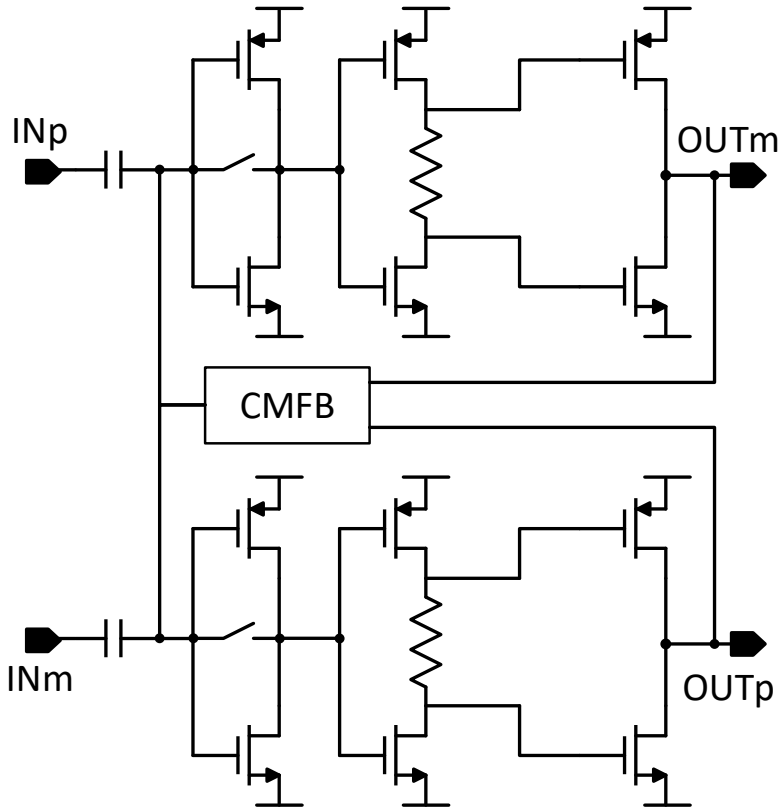
TOPOLOGY SELECTION



PSEUDO DIFFERENTIAL

TOPOLOGY SELECTION

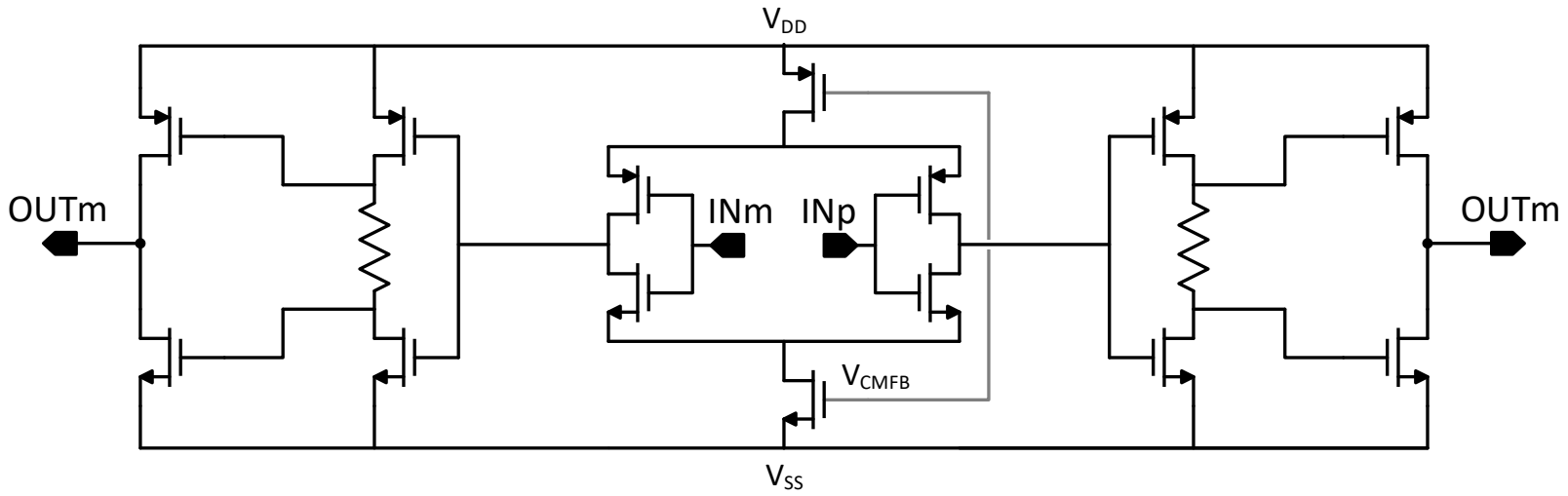
- Can be purely inverter-based, most dynamic
- Best for
  - Speed
- Limitations
  - Large input offset must be canceled
  - Limited accuracy



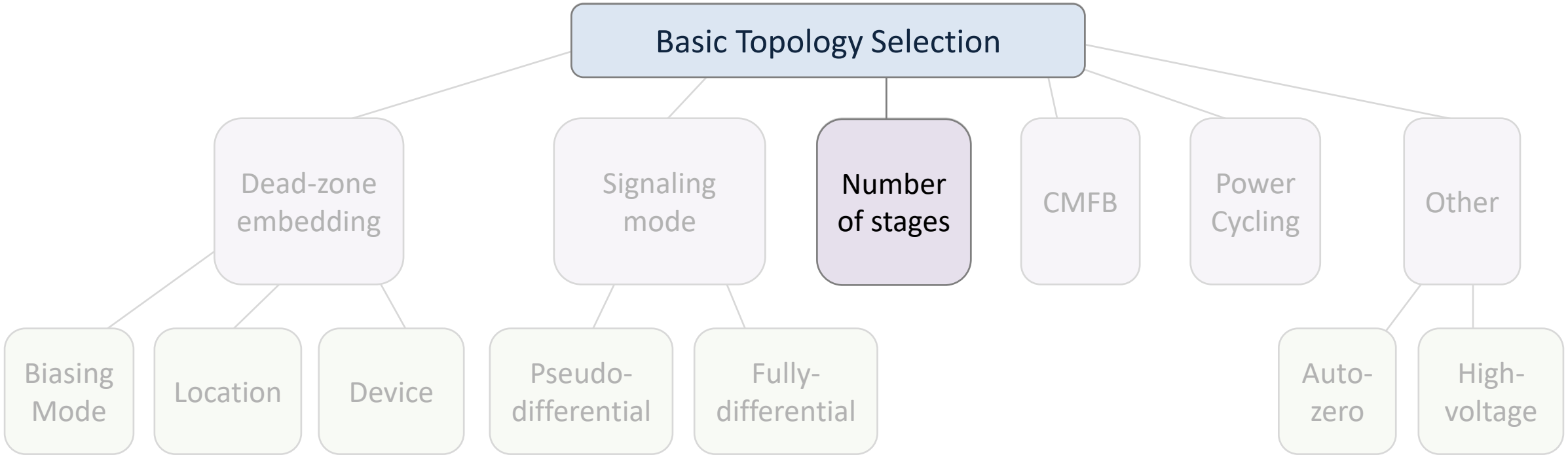
FULLY DIFFERENTIAL

TOPOLOGY SELECTION

- Fully-differential
- Best for
  - General purpose
  - Highest accuracy
- Limitations
  - Moderate speed /power penalty
    (front stage becomes slower)



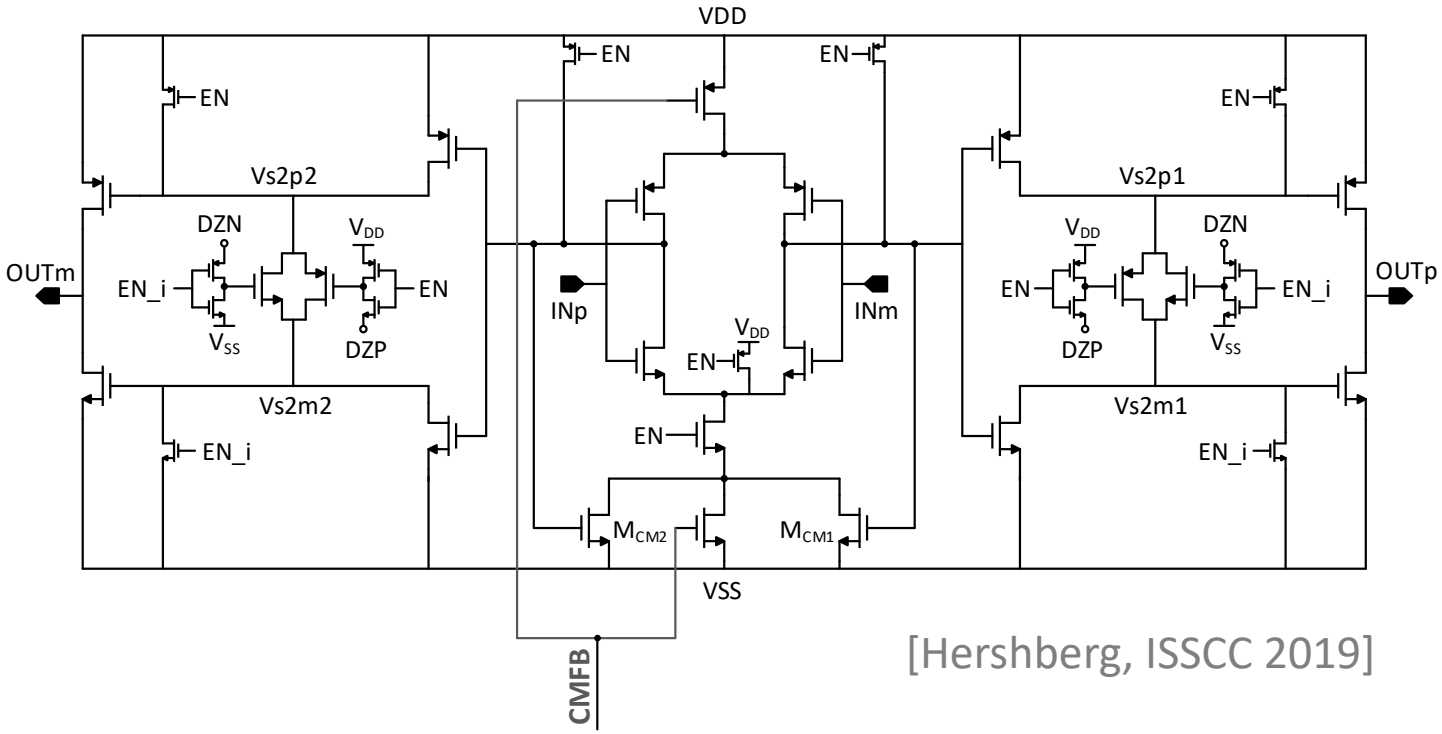
TOPOLOGY SELECTION



THREE-STAGE

TOPOLOGY SELECTION

- The “workhorse”
- Best for
  - Most applications
- Limitations
  - Might not give enough gain in some technologies to support calibration-free operation
  - CMFB can be a little tricky in fully-differential topologies

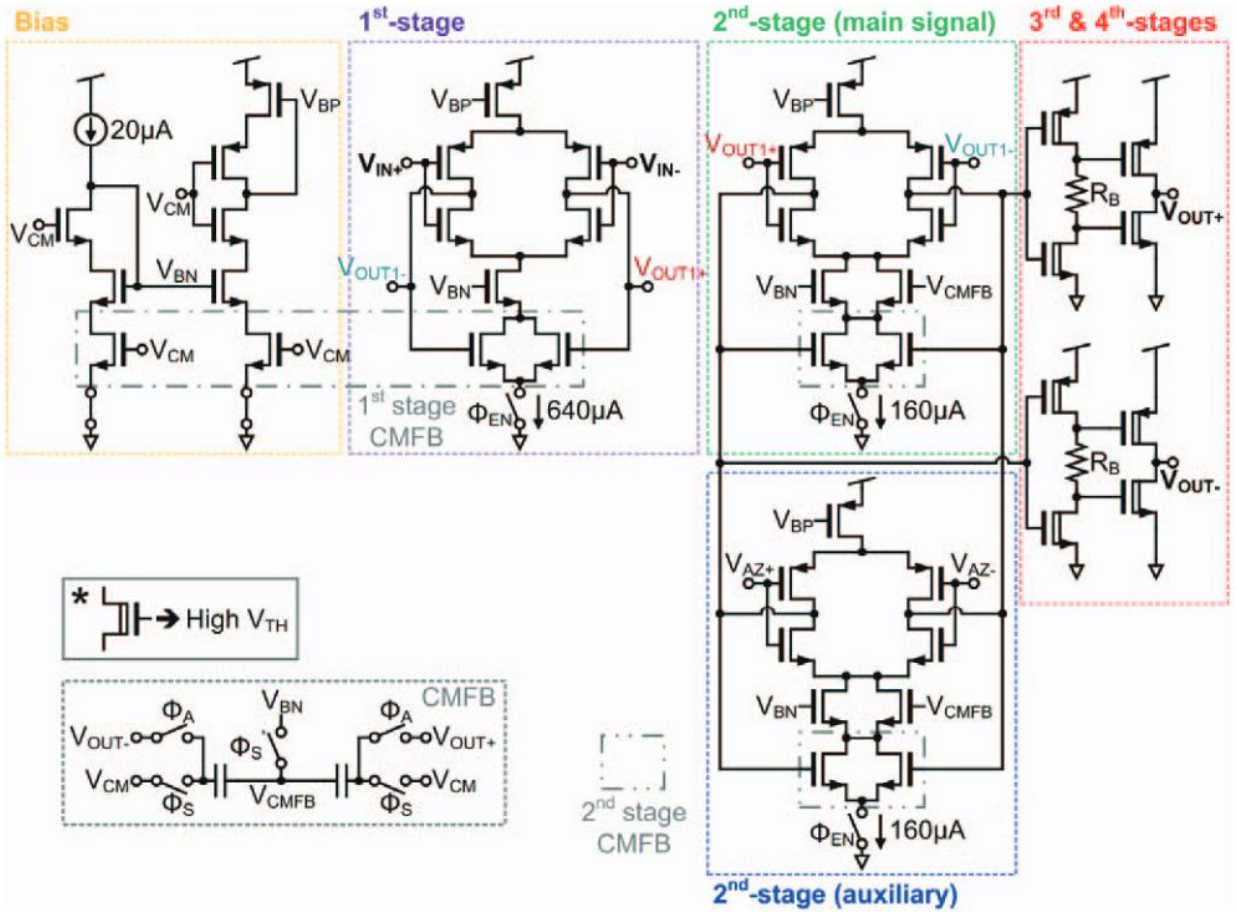


[Hershberg, ISSCC 2019]

FOUR-STAGE

TOPOLOGY SELECTION

- When more gain is needed
- Best for
  - High precision
  - Calibration-free
- Limitations
  - CMFB and latch-up require careful consideration
  - A little less speed (extra internal pole)

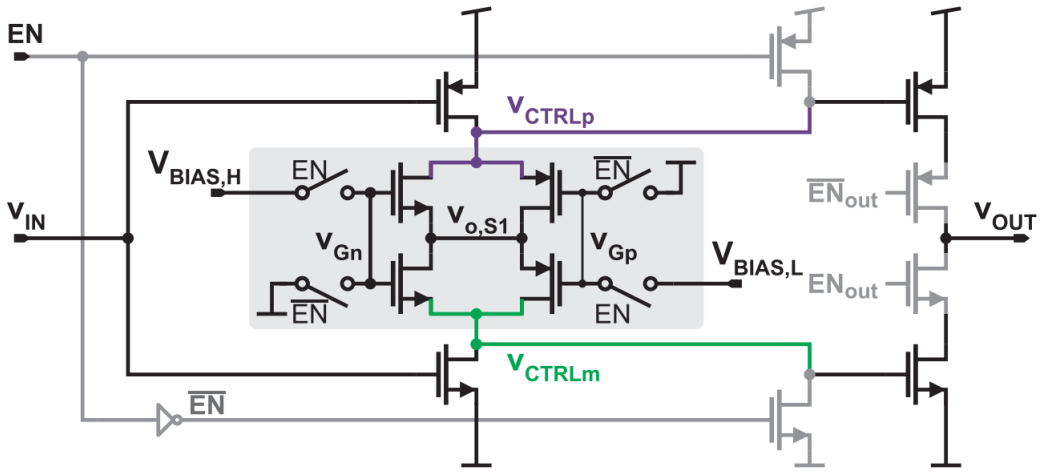


[Lim, VLSI 2017]

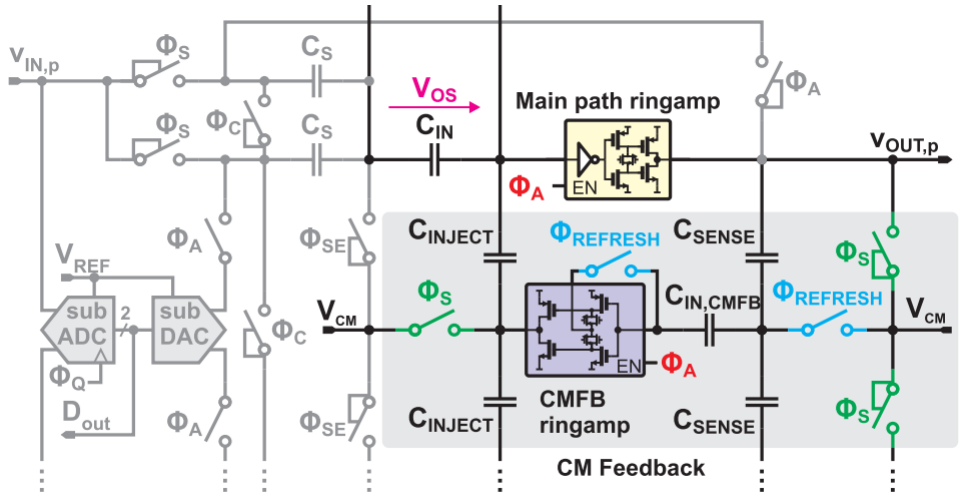
TWO-STAGE

TOPOLOGY SELECTION

- Special purpose
- Best for
  - Non-inverting feedback loop (e.g. CMFB)
  - Low precision applications
- Limitations
  - Low gain



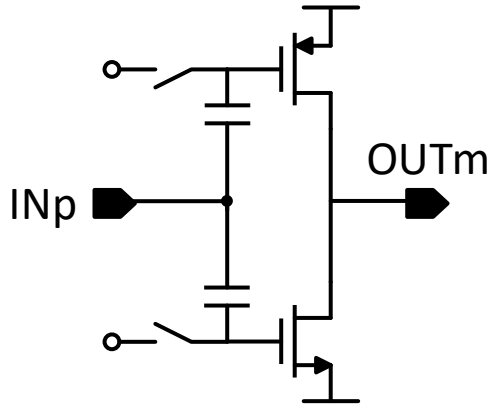
[Lagos, JSSC Feb. 2019]



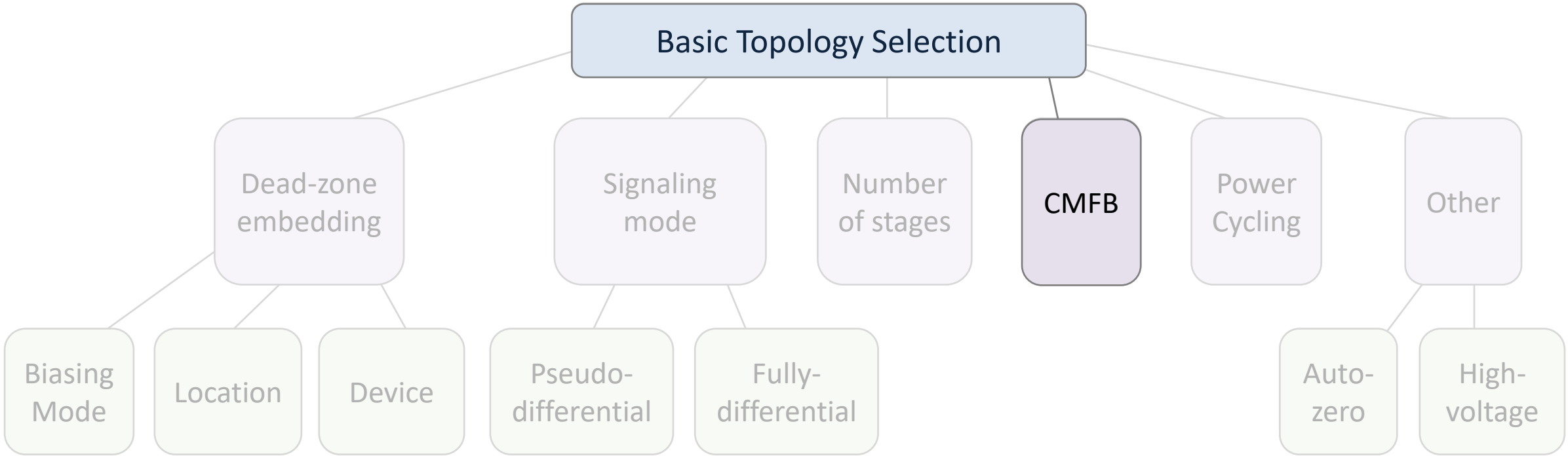
ONE STAGE?

TOPOLOGY SELECTION

- “Inverter based amplifier”
- Best for
  - Specialty applications
- Limitations
  - Low gain
  - Low gain-bandwidth
  - Low slew rate / slew efficiency
  - No gain before output stage (no large-signal effects)
- *A multi-stage ringamp is generally faster and more efficient.*



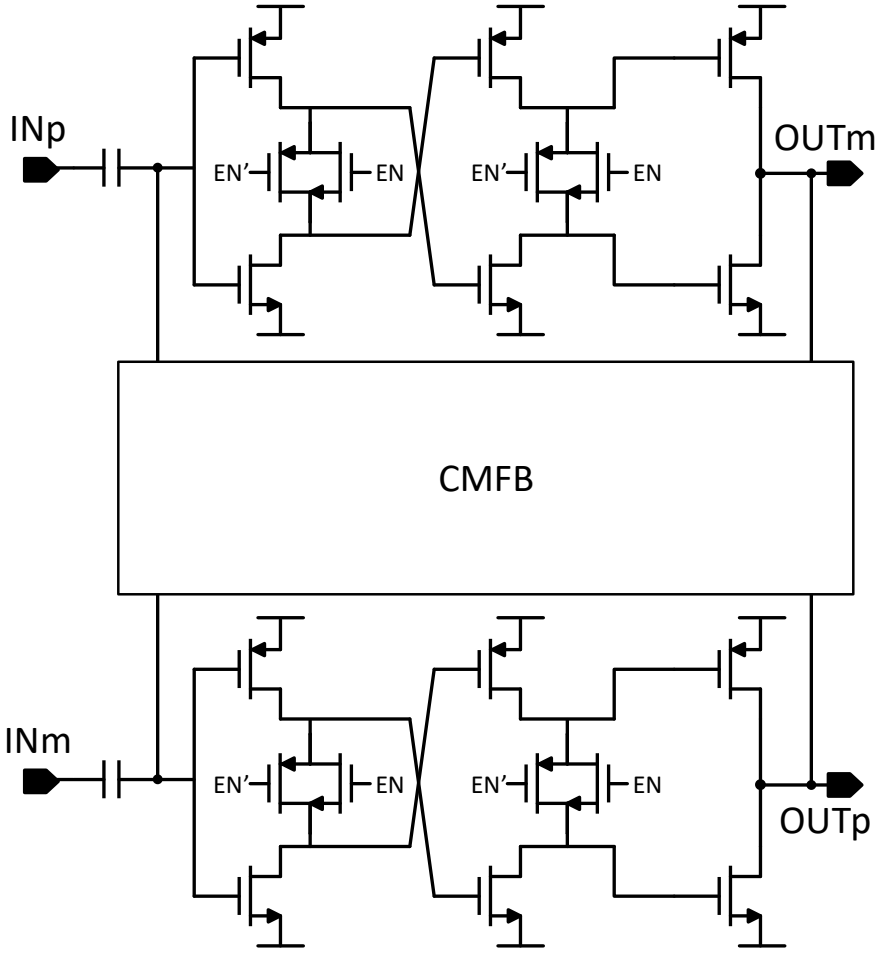
TOPOLOGY SELECTION



TOPOLOGY SELECTION

CMFB

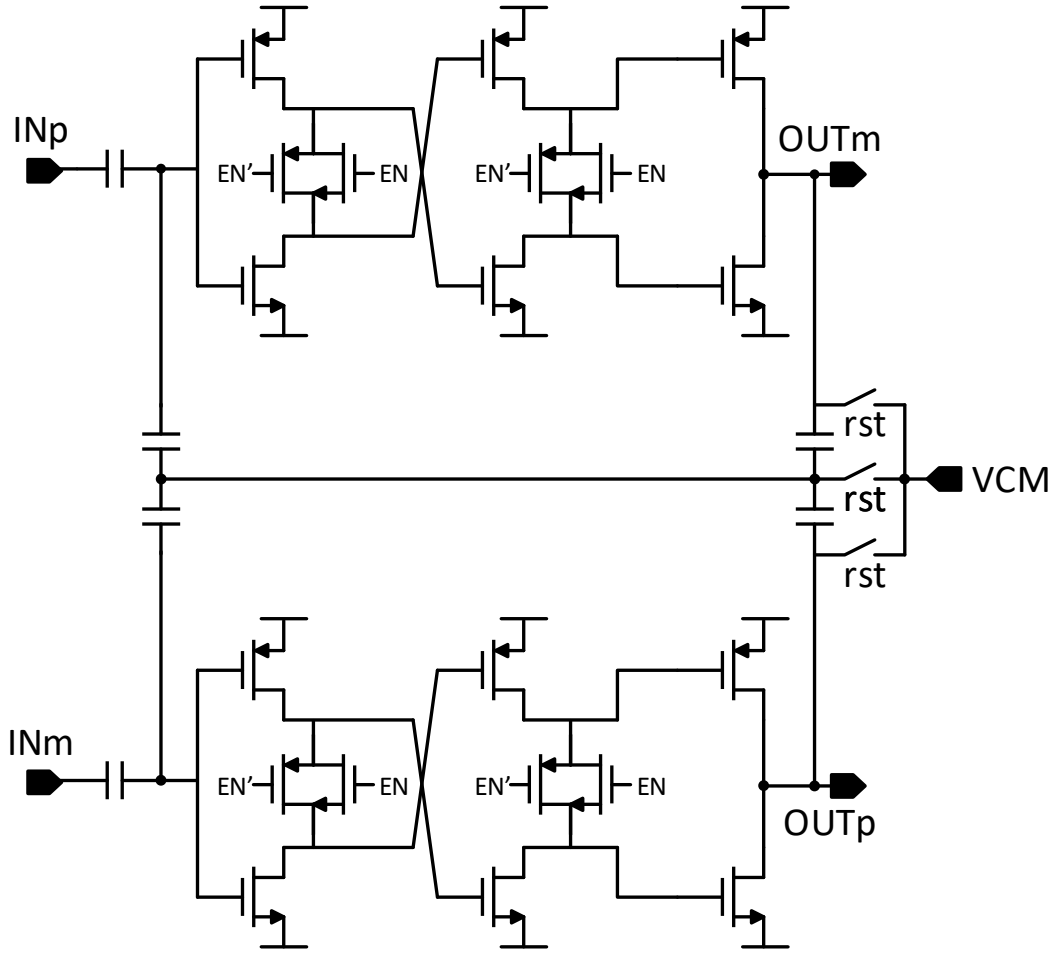
- Approach varies depending on topology
  - Psuedo-differential
  - Fully-differential
  - Level of CM rejection needed



TOPOLOGY SELECTION

CMFB

- Approach varies depending on topology
  - Psuedo-differential
  - Fully-differential
  - Level of CM rejection needed
- Passive CMFB
  - Simple
  - Often good enough

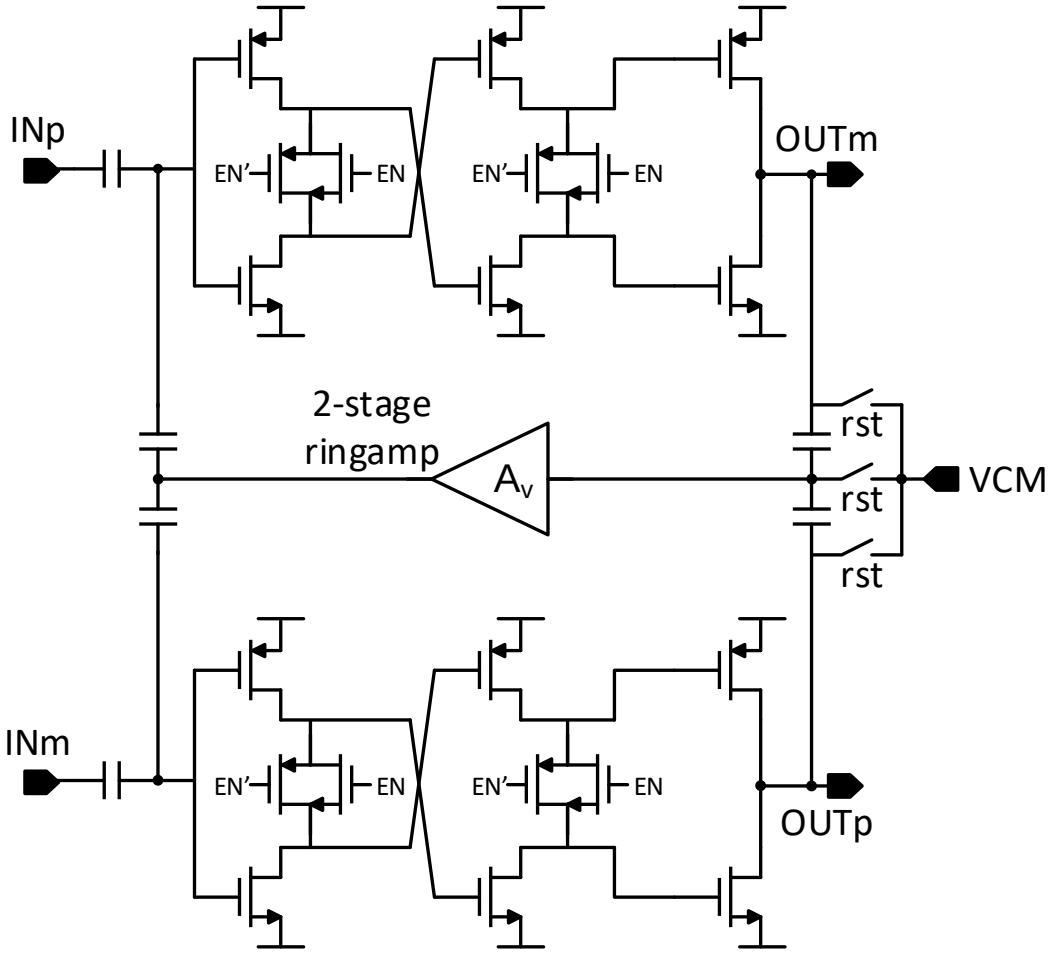


[Hershberg, JSSC 2012]

TOPOLOGY SELECTION

CMFB

- Approach varies depending on topology
  - Psuedo-differential
  - Fully-differential
  - Level of CM rejection needed
- Passive CMFB
  - Simple
  - Often good enough
- Active CMFB
  - Add gain
  - Higher accuracy
  - Larger rejection range

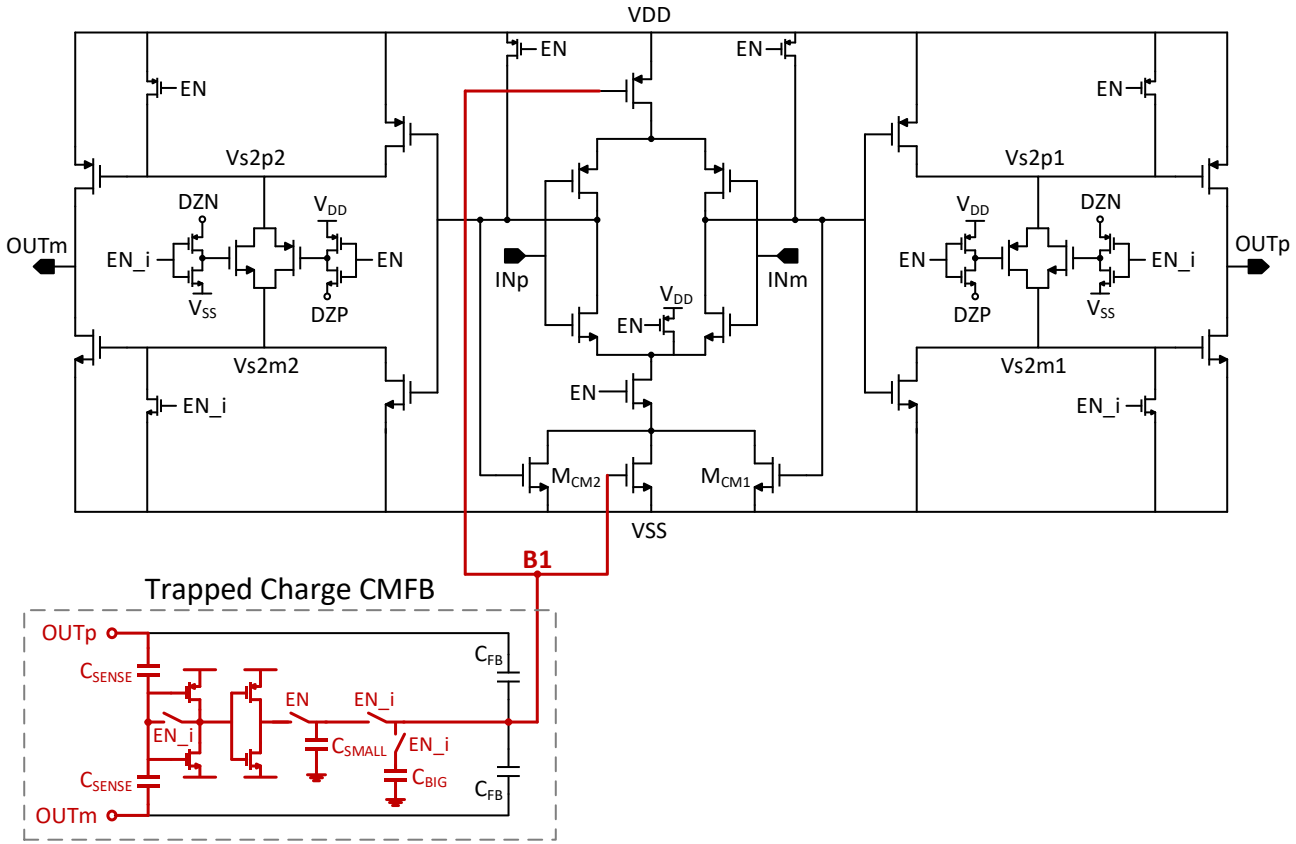


[Lagos, JSSC Feb. 2019]

TOPOLOGY SELECTION

CMFB

- Fully differential
  - Often requires global *and* local loops
- 3 paths
  - DC bias
  - Fast global feedback
  - Fast local feedback



[Hershberg, ISSCC 2019]

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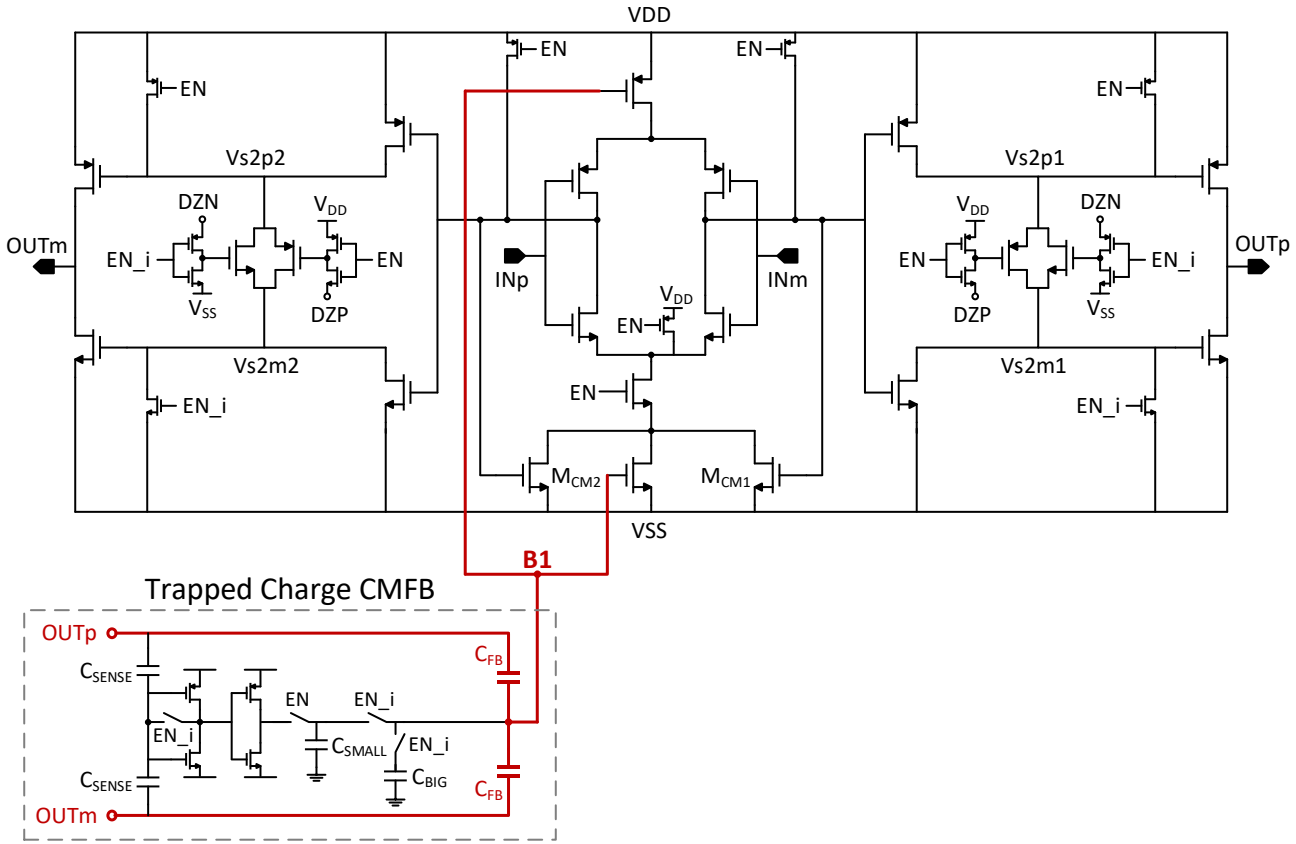

[Hershberg, ISSCC 2019]

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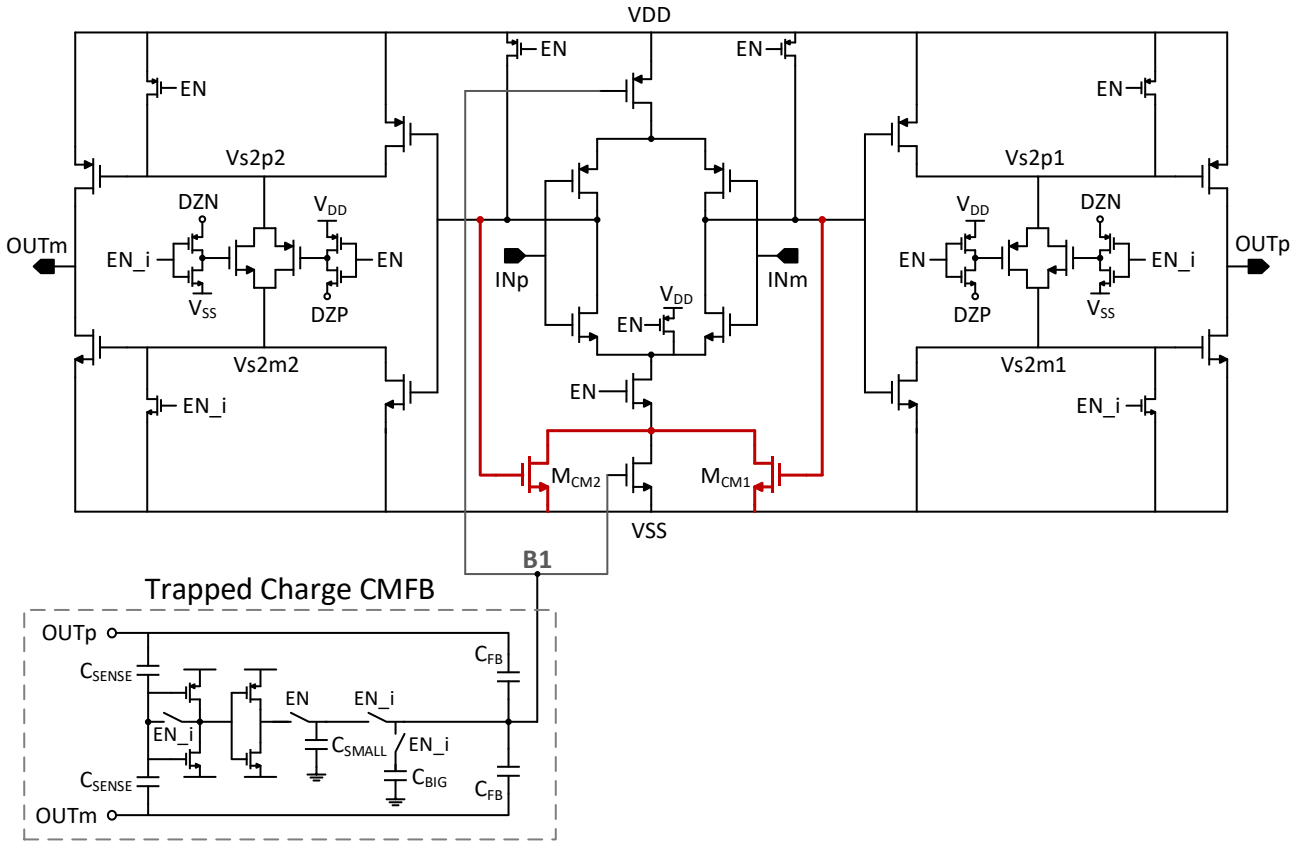
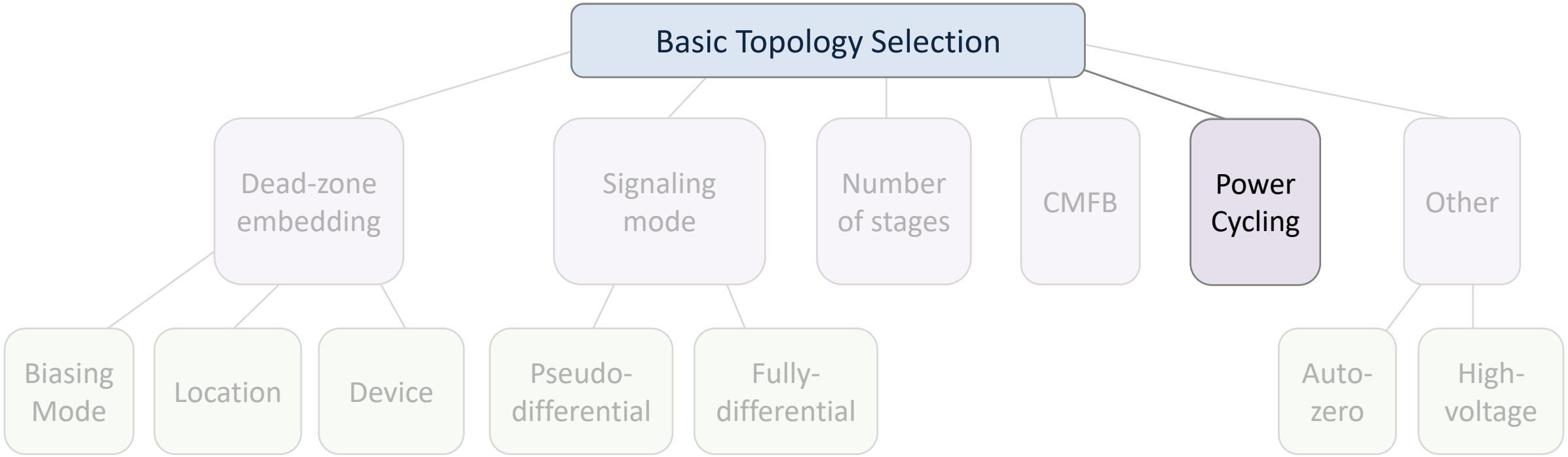


[Hershberg, ISSCC 2019]

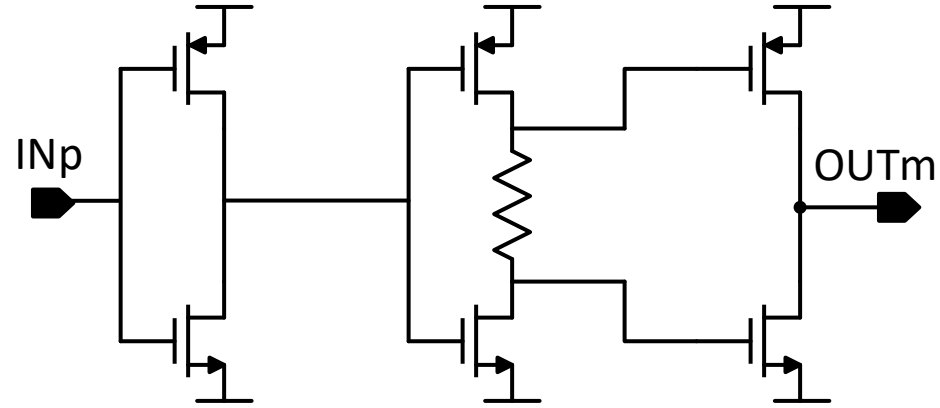
TOPOLOGY SELECTION



TOPOLOGY SELECTION

POWER CYCLING

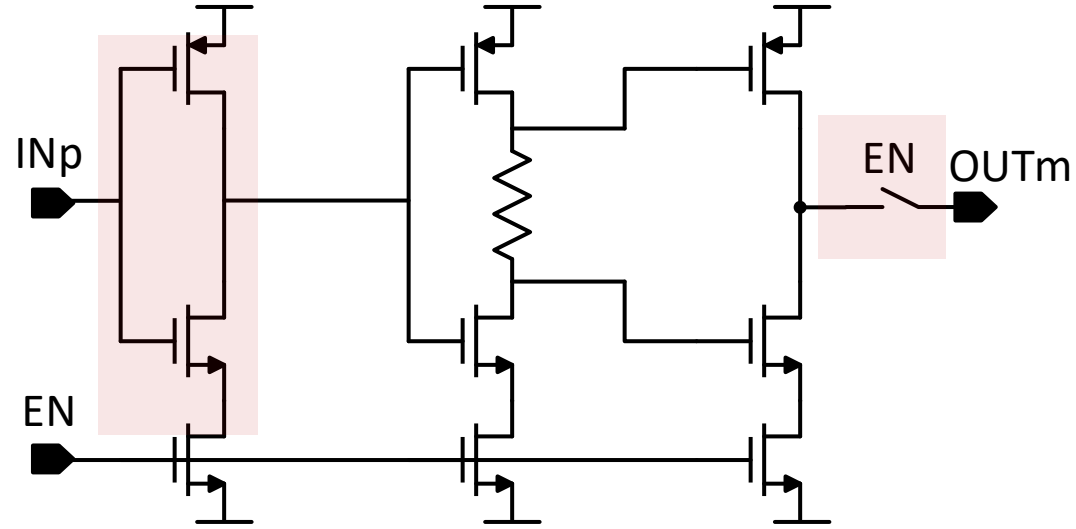
- Only operate when needed
  - Save power
- Best solution very architecture dependent



TOPOLOGY SELECTION

POWER CYCLING

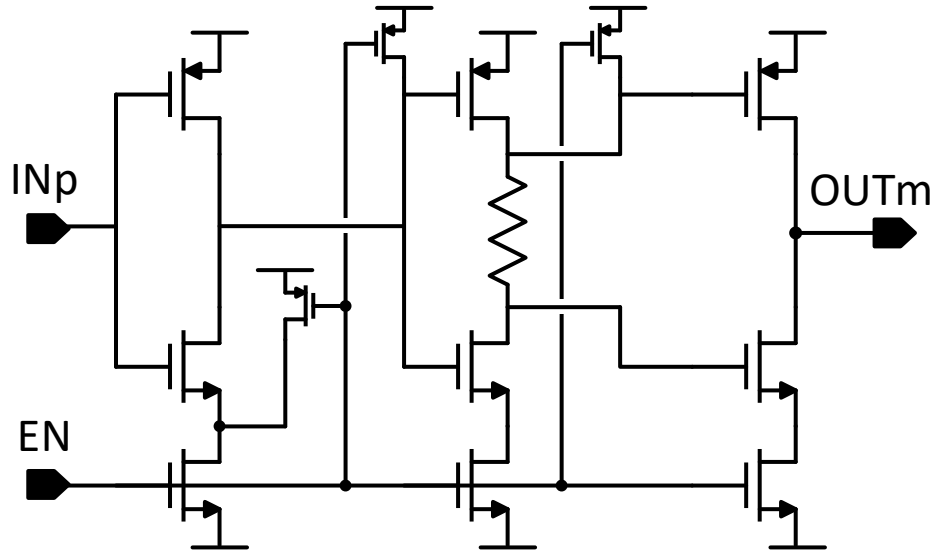
- Only operate when needed
  - Save power
- Best solution is very architecture dependent
- **A naive solution:** power gate + output switch
  - Extra switch in feedback path ☹
  - Undefined internal reset state ☹
  - Signal dependent charge kickback ☹
  - Clock must drive all switches on EN line ☹
  - Headroom reduced by power gating switches ☹



TOPOLOGY SELECTION

POWER CYCLING

- Only operate when needed
  - Save power
- Best solution is very architecture dependent
- **A better solution:** full-reset, self-disconnect
  - Extra parasitics from pullup/pulldown switches ☹
  - Clock must drive all switches on EN line ☹
  - Headroom reduced by power gating switches ☹



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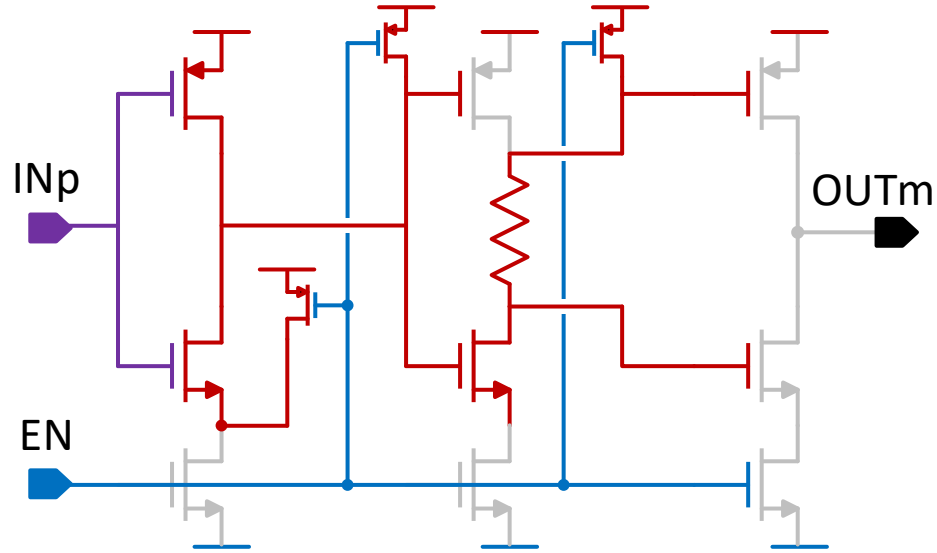
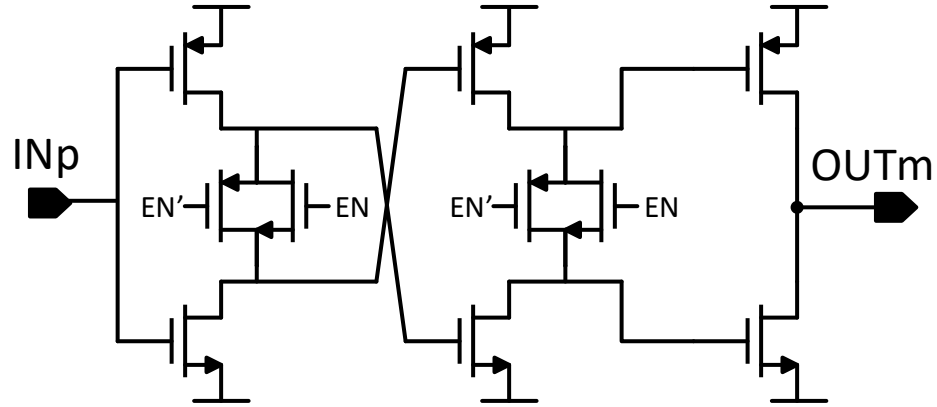


TOPOLOGY SELECTION

POWER CYCLING

- **A very elegant solution:** self-resetting
- Requires
  - Bias-enhancement (we'll get to this later)
  - CMOS resistors
- Best of all worlds
  - No power-gating switches
  - No pull-up or pull-down switches
  - Small switches (CMOS resistors) minimize clock loading



[Lagos, JSSC Mar. 2019]

TOPOLOGY SELECTION

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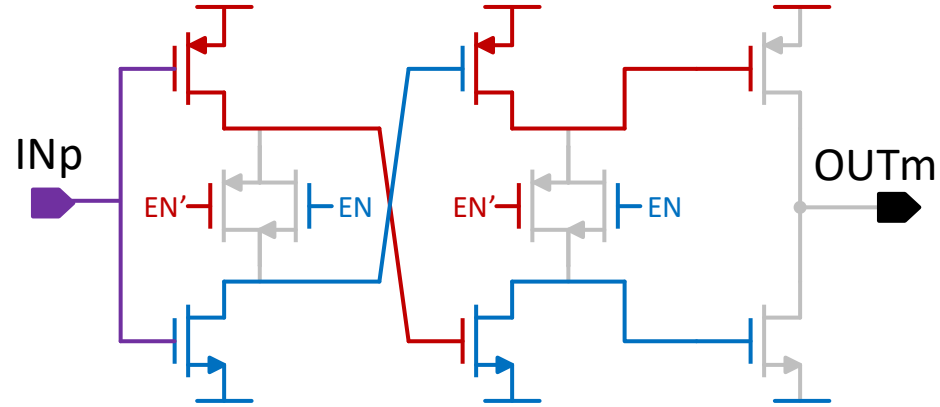
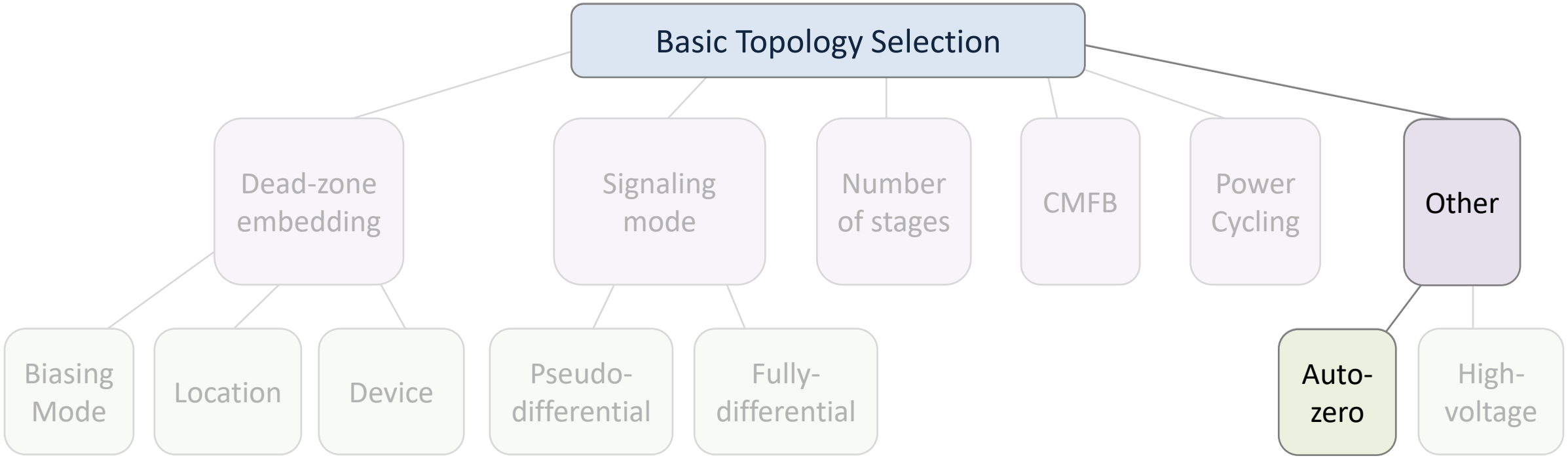
  - No pull-up or pull-down switches
  - Small switches (CMOS resistors) minimize clock loading



[Lagos, JSSC Mar. 2019]

TOPOLOGY SELECTION



TOPOLOGY SELECTION

AUTO-ZERO

- Not for free
  - Extra complexity
  - Sometimes extra power
- Some applications / topologies require it
  - Pseudo-differential ringamps
  - Zero-offset applications
- Most applications / topologies can avoid it
  - Offset tolerant and “good enough” use cases
  - System level methods

TOPOLOGY SELECTION

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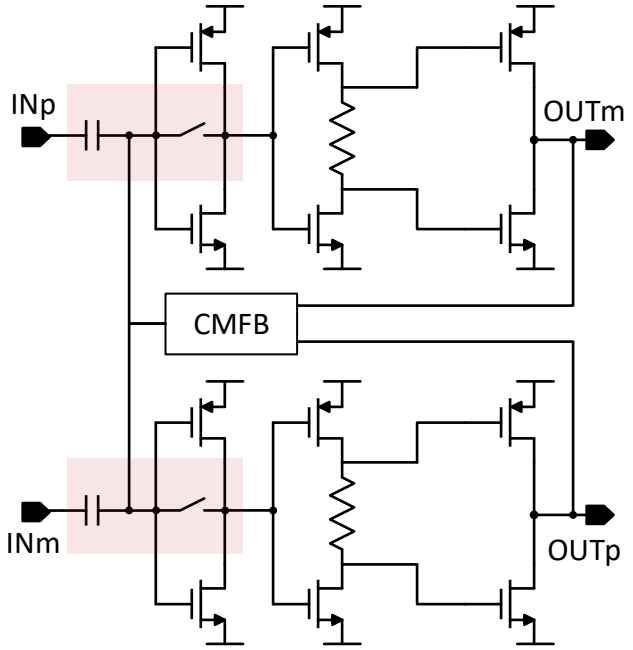

“Good enough” partial cancellation:

1. Inverter trip-point offset
   (tech. dependent V_{TH} mismatch)
2. Stage 1 random offset
   (largest source of random offset)

TOPOLOGY SELECTION

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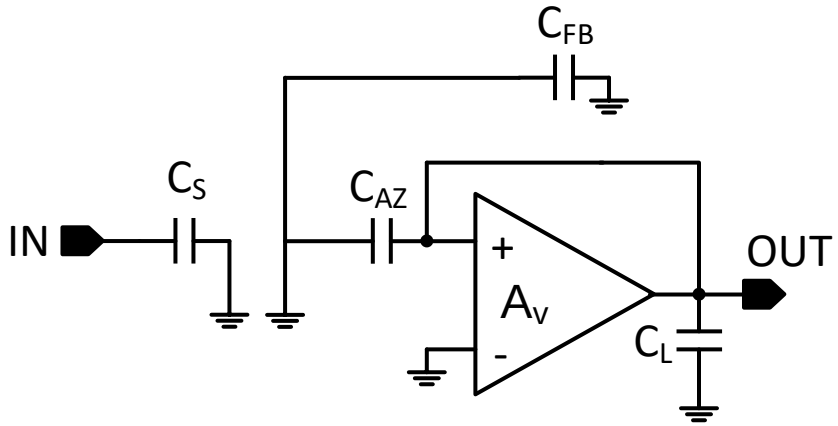

$$\beta = 1$$

$$C_{LOAD} = C_L + C_{AZ}$$

Be careful with C_{AZ} sizing :

Stability

Noise

[Lim, Oct. 2015]

TOPOLOGY SELECTION

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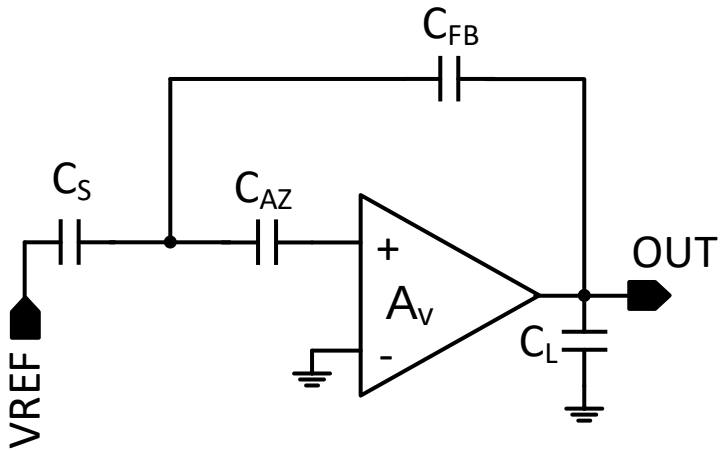

$$\beta = C_S / C_{FB}$$

$$C_{LOAD} = C_L + C_{FB}//C_S$$

[Lim, Oct. 2015]

TOPOLOGY SELECTION

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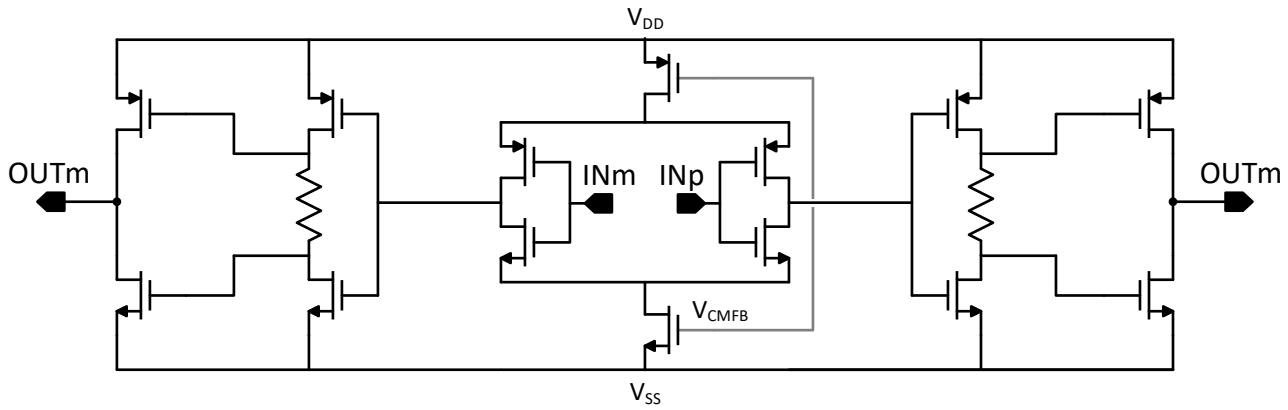

Differential topologies:

- No inverter trip-point offset ☺
- Only random mismatch offset

TOPOLOGY SELECTION

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  - Sometimes extra power
- Some applications / topologies require it
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  - Zero-offset applications
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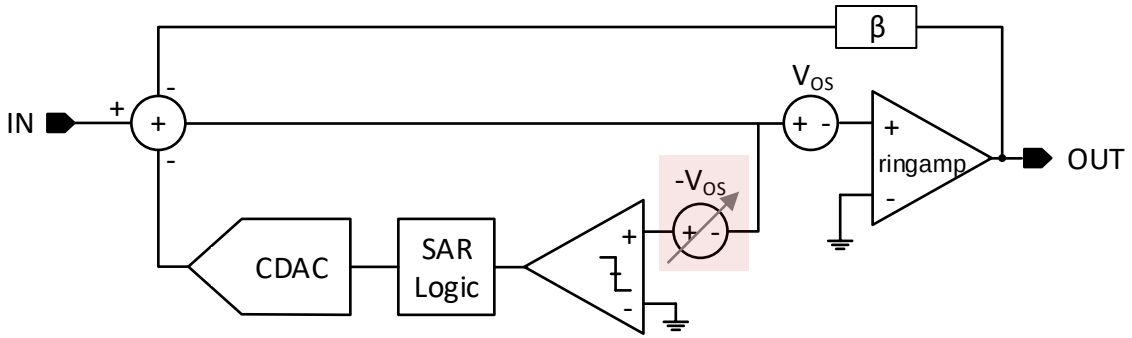
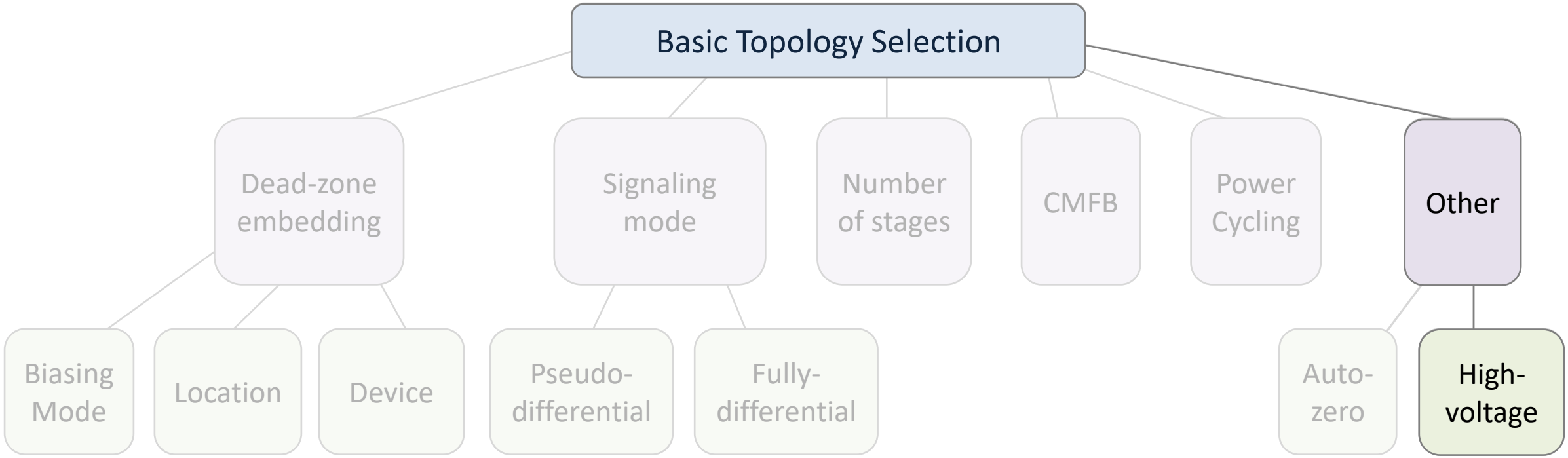
  - Offset tolerant and “good enough” use cases
  - System level methods

Example: Pipelined SAR stage



Can often find simple methods to cancel ringamp offset somewhere else in the system

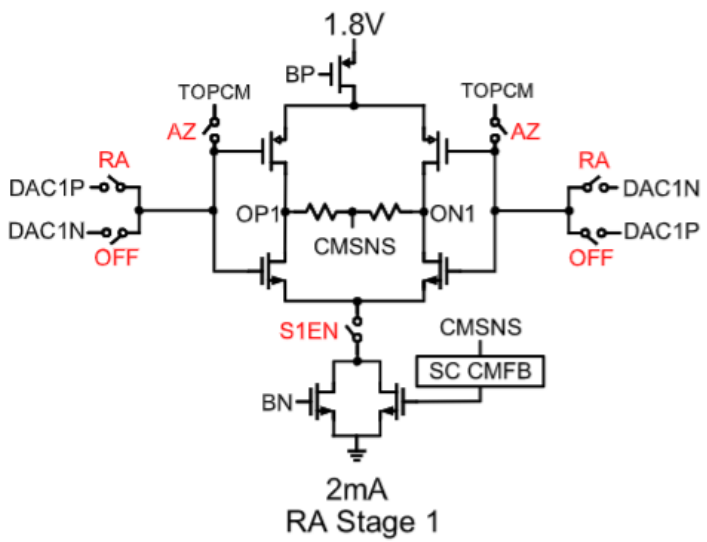
TOPOLOGY SELECTION

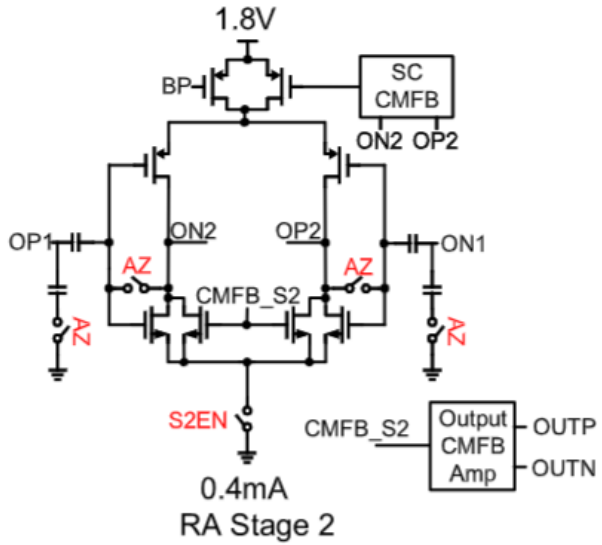


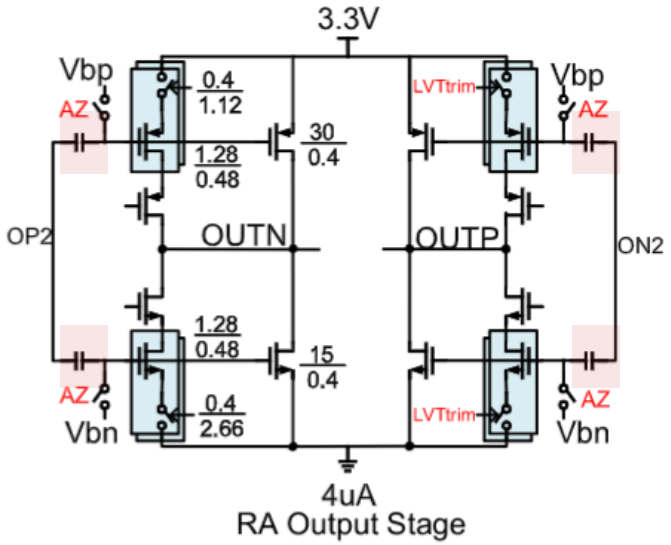
TOPOLOGY SELECTION

HIGH-VOLTAGE

- Capacitor embedding is best
  - Can store large ΔV needed to generate dead-zone
  - Can level shift between different VDDs
  - Can couple in multiple output paths (coarse/fine)



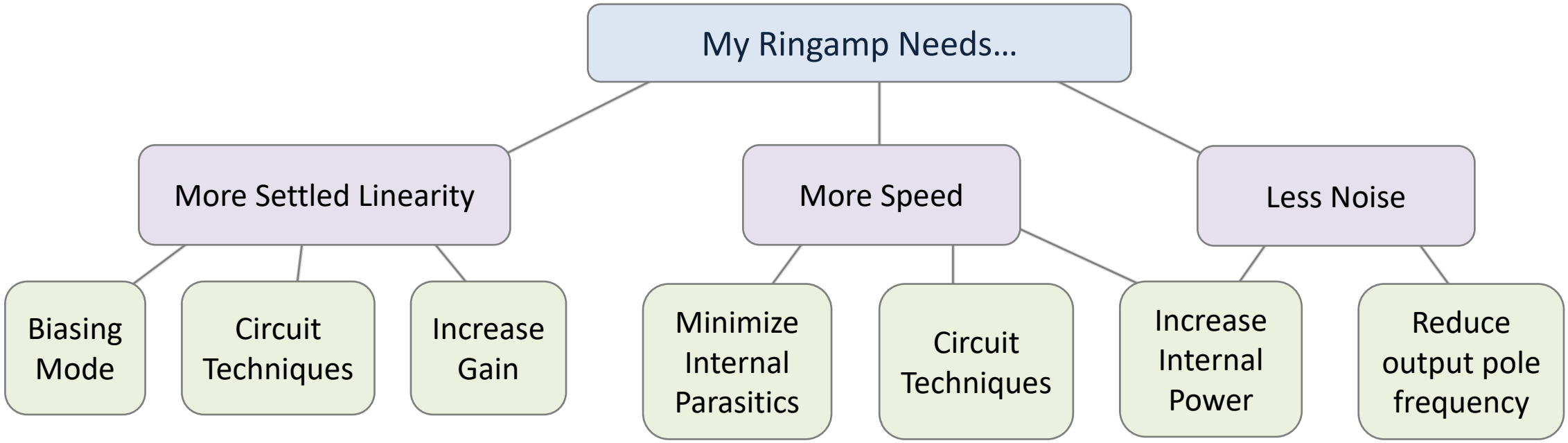




[ElShater, JSSC 2019]

PATHWAYS TO PERFORMANCE

PATHWAYS TO PERFORMANCE



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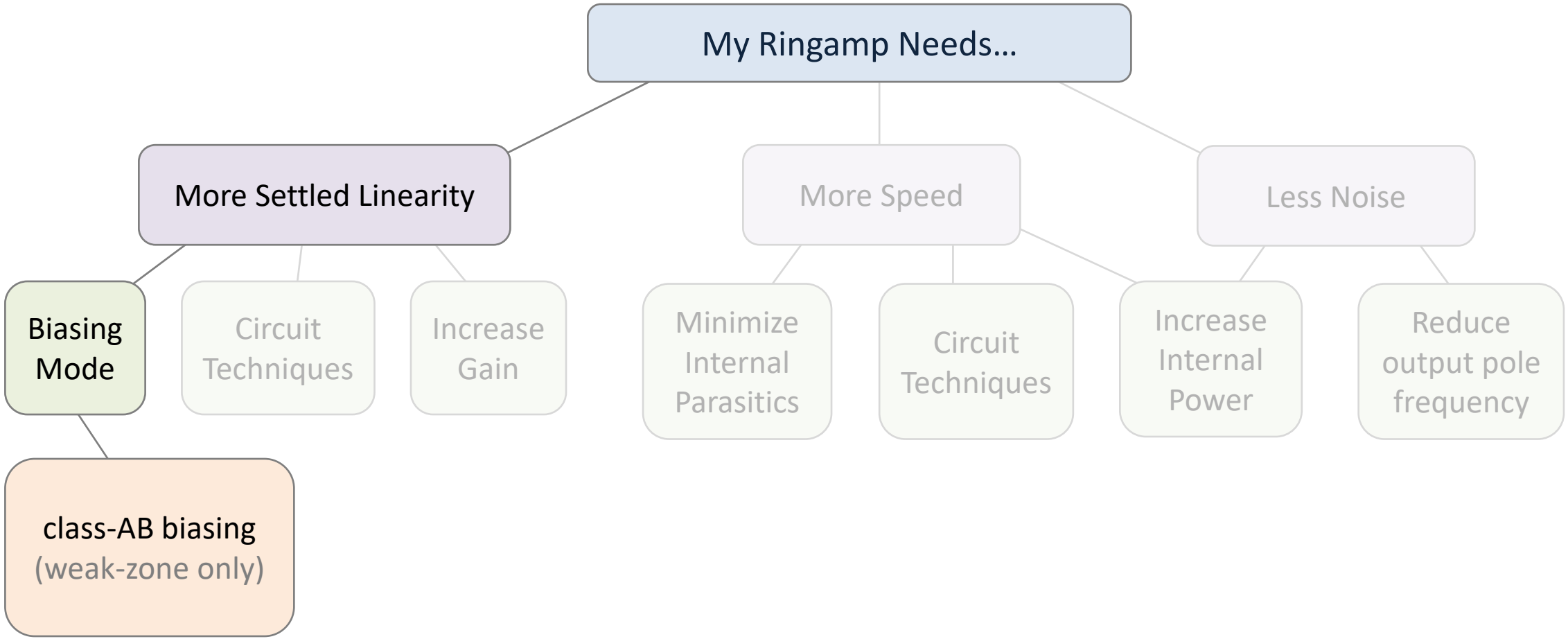

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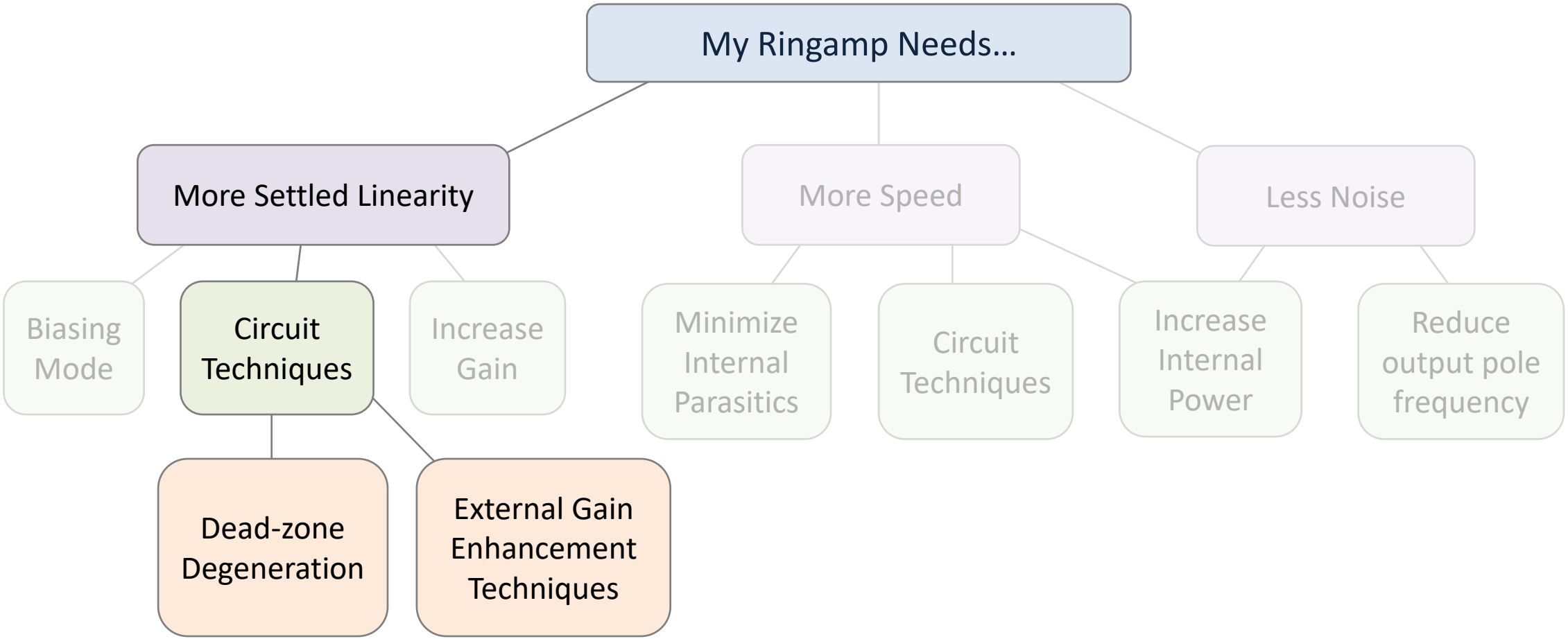
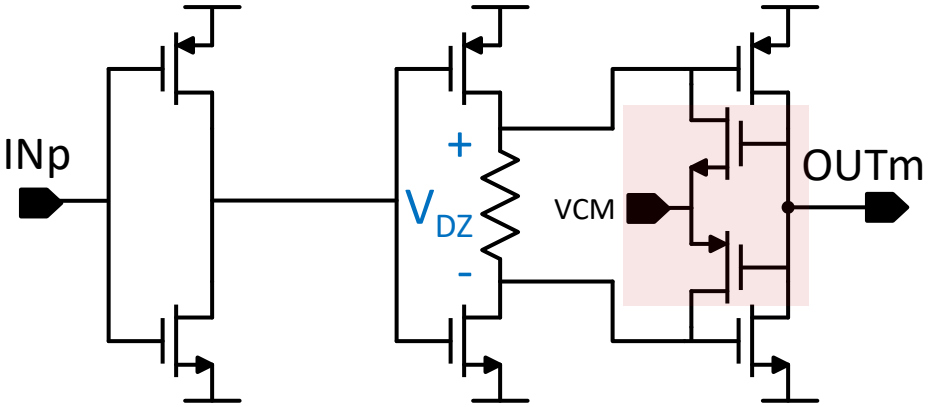


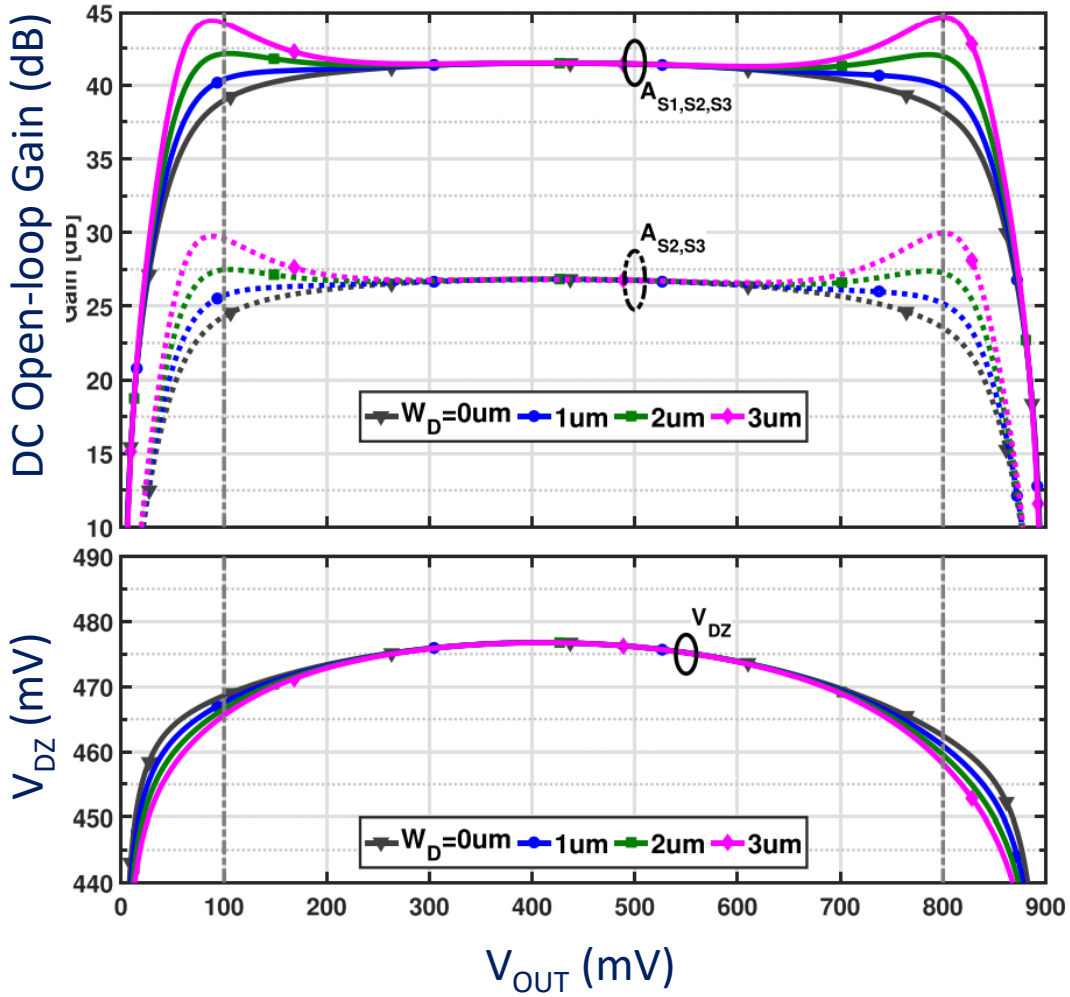
DEAD-ZONE DEGENERATION

LINEARITY ENHANCEMENT

[Lagos, JSSC Mar. 2019]

- Motivation
  - 1st order linear gain error often easy to calibrate (with digital or trimming)
  - Higher order gain error much harder to correct
- Idea
  - Feedback to "warp" V_{DZ} as function of V_{OUT}
  - Especially useful in low-gain tech. like 28nm





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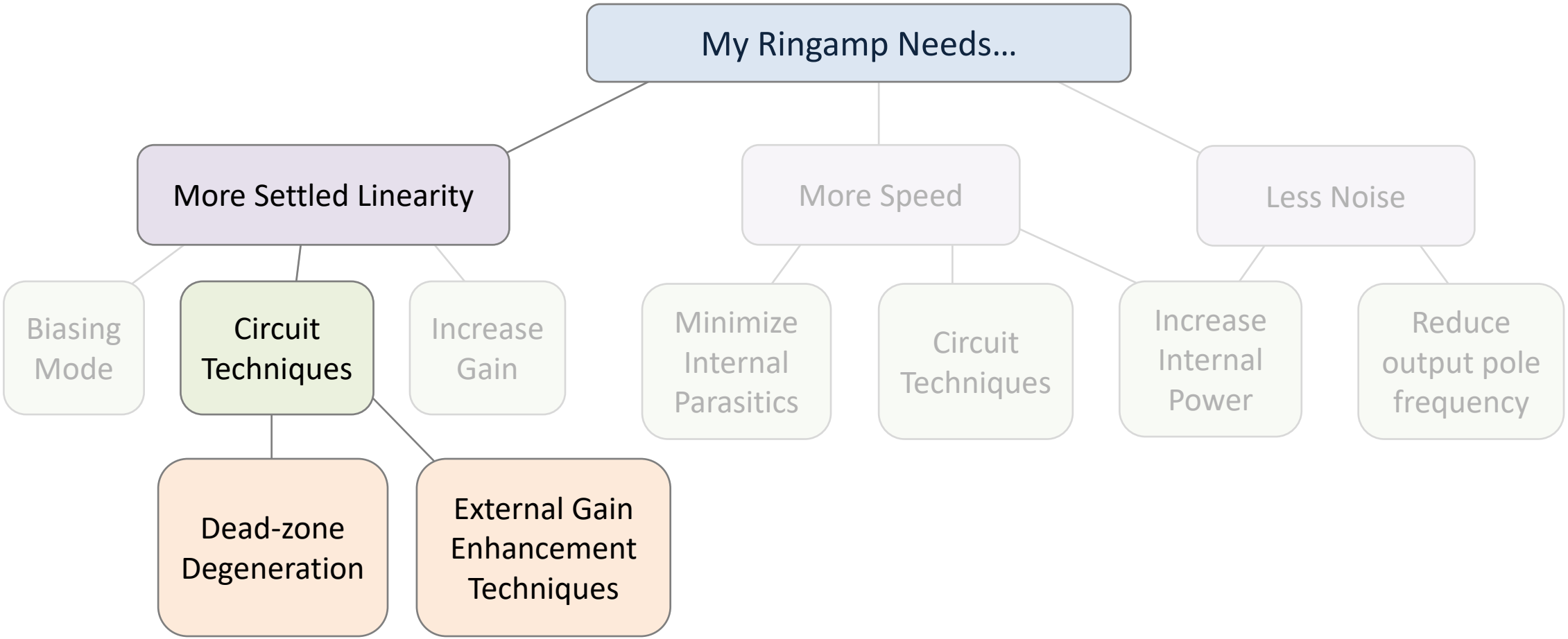
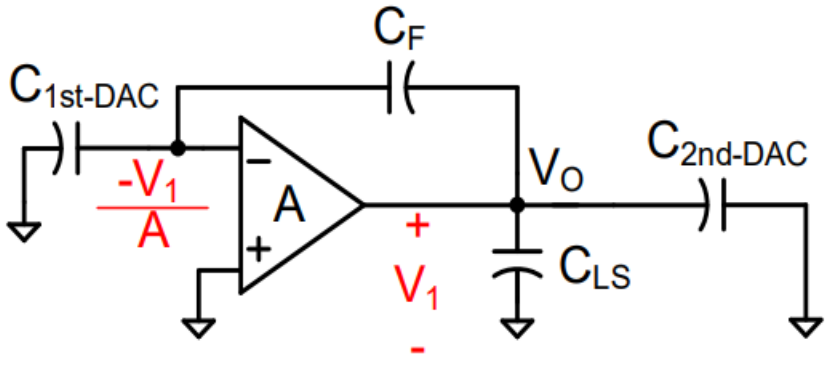


EXTERNAL GAIN ENHANCEMENT TECHNIQUES

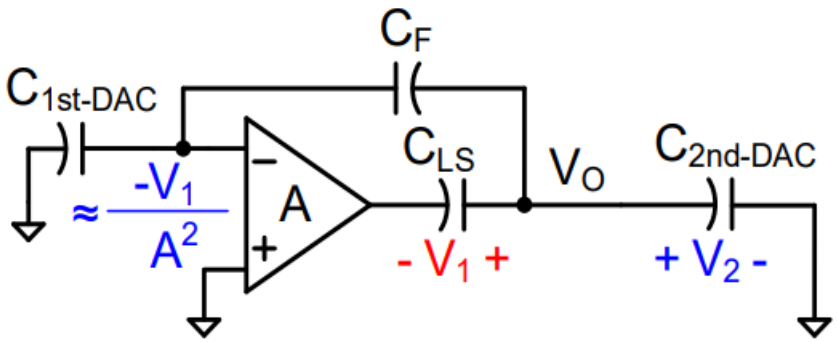
LINEARITY ENHANCEMENT

- Class-AB style ringamps compatible with many "classical" gain enhancement techniques
- Ringamps using Correlated Level Shifting (CLS) techniques:
  - Split-CLS [Hershberg, JSSC 2012]
  - A-CLS [T.C. Hung, JSSC 2019]
  - WA-CLS [T.C. Hung, JSSC 2020]

ϕ_{A1}: Before level shift

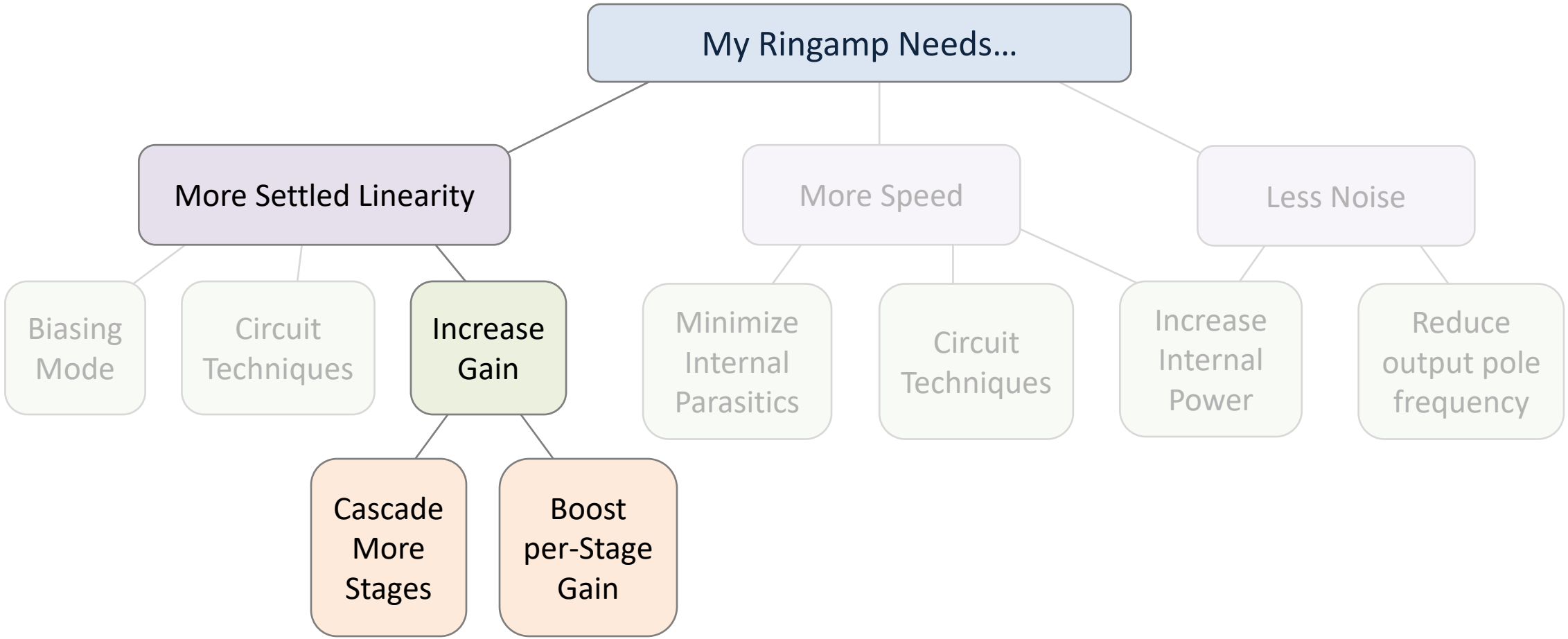


ϕ_{A2}: After level shift



[T.C. Hung, JSSC 2020]

PATHWAYS TO PERFORMANCE



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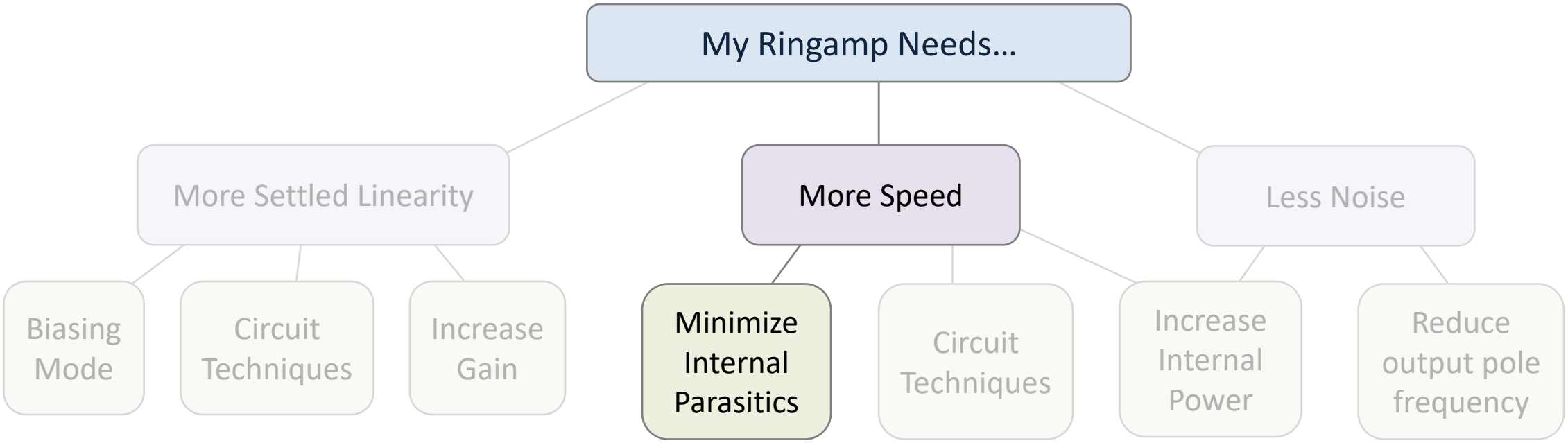
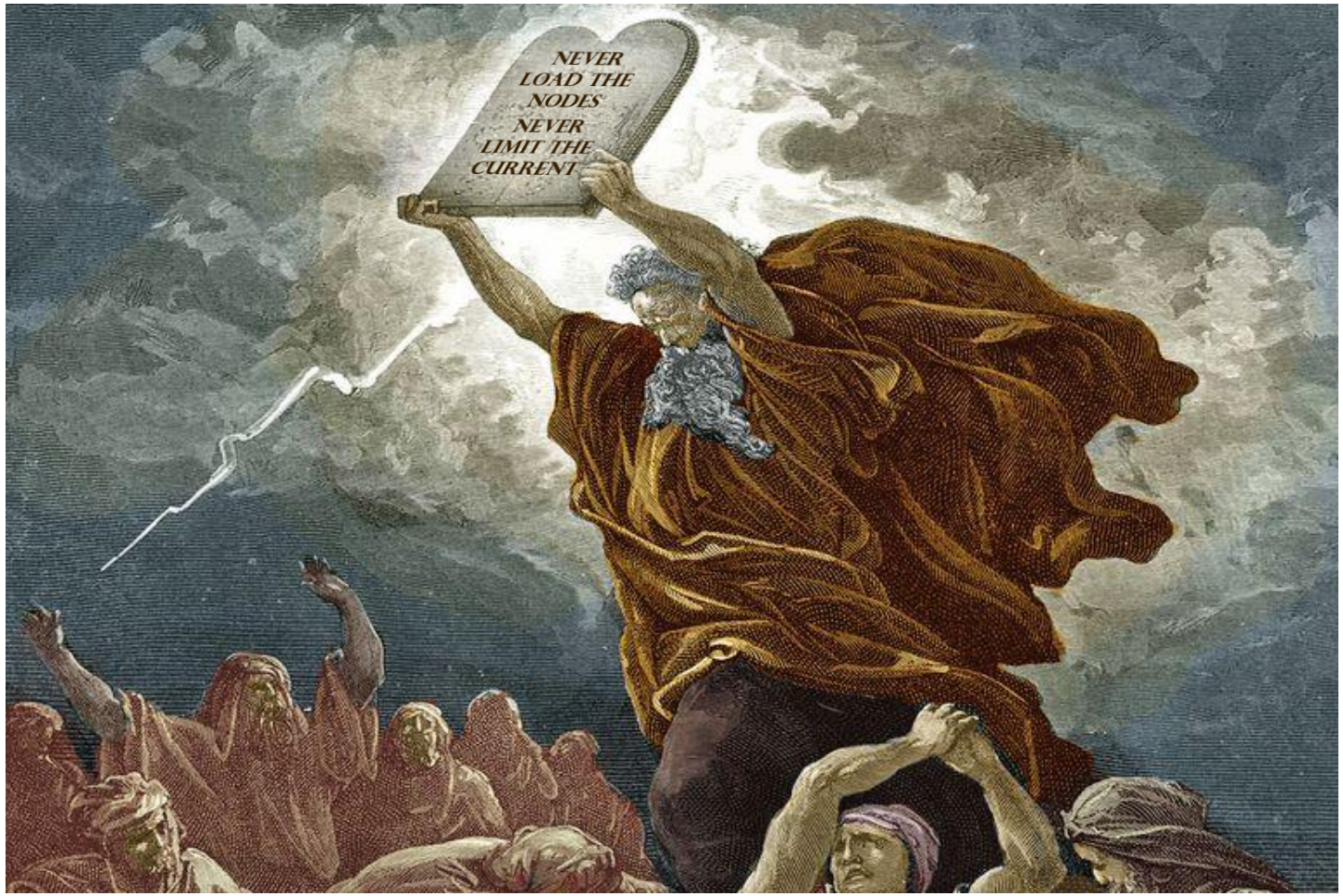


THE 2 COMMANDMENTS

OF HIGH SPEED RINGAMP DESIGN

1. Thou shalt never load the internal nodes

2. Thou shalt never limit the internal currents

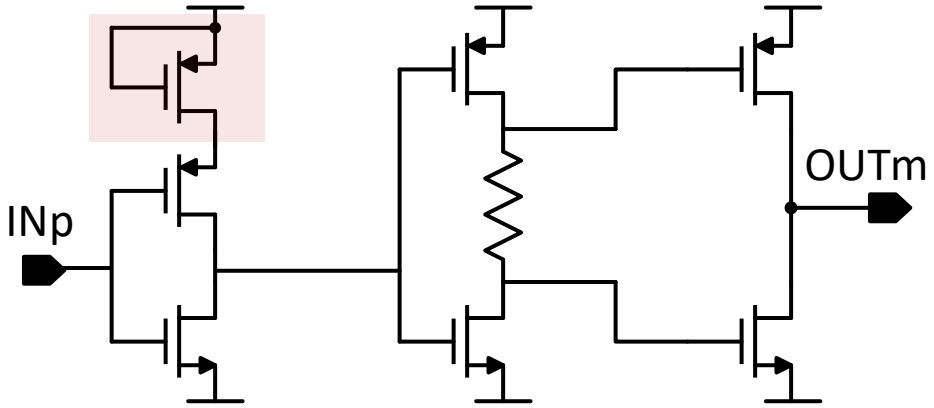


THE 2 COMMANDMENTS

OF HIGH SPEED RINGAMP DESIGN

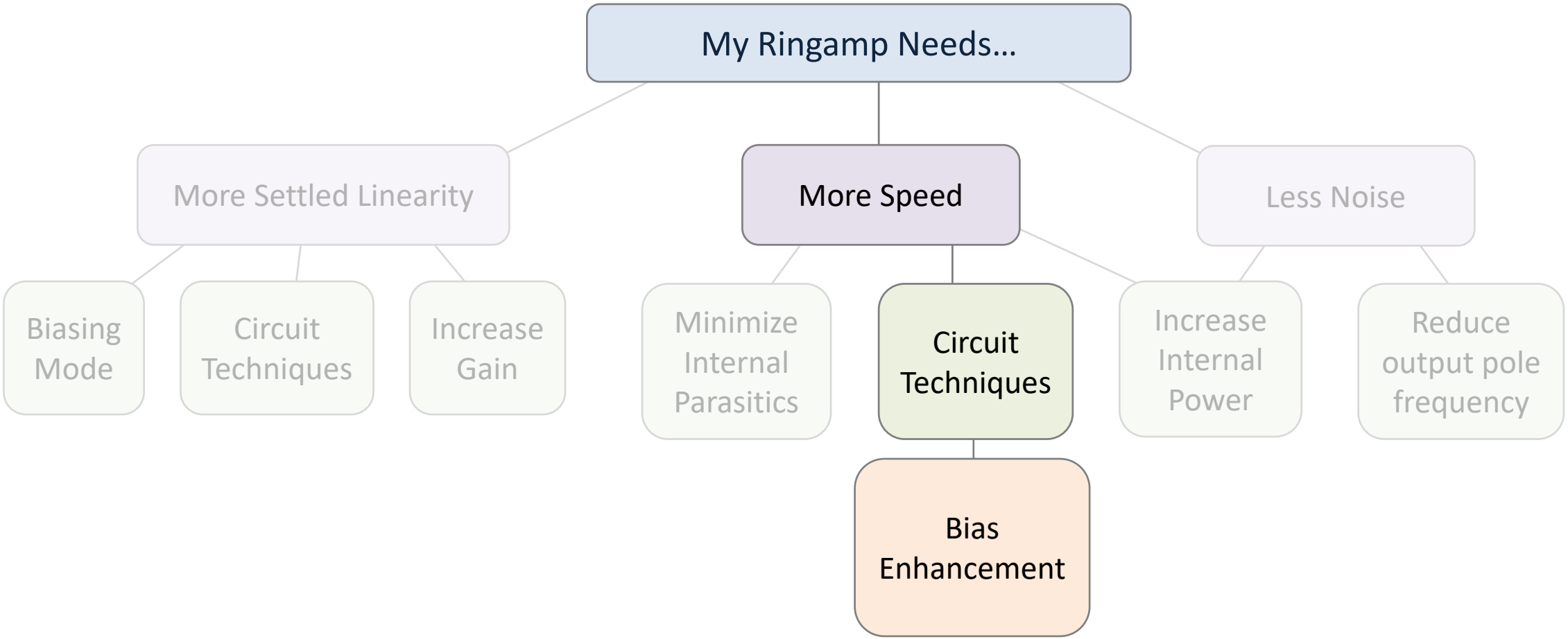
- But many choose to break the rules...
  - Trade speed for other benefits

Current limiter for peak g_m/I_D



[Lim, JSSC Oct. 2015]

PATHWAYS TO PERFORMANCE

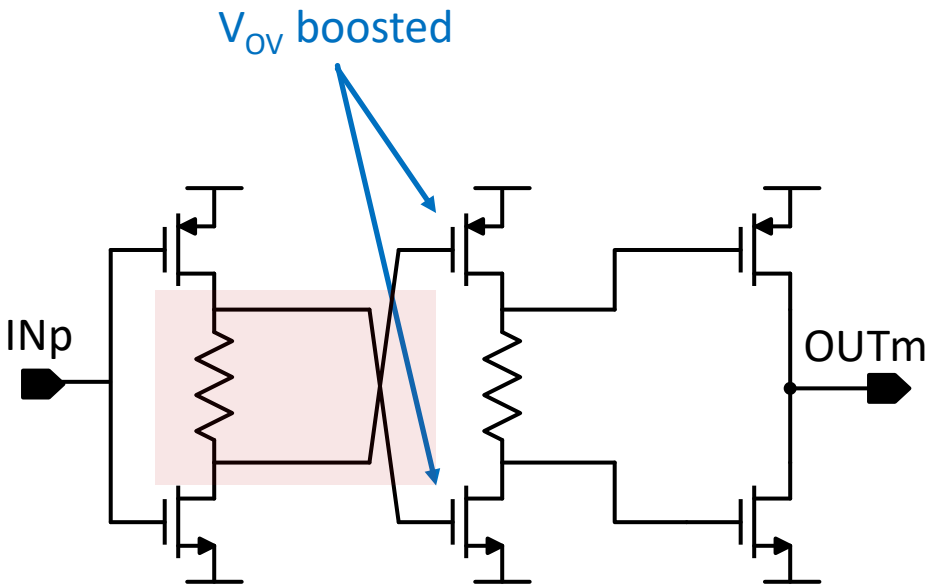


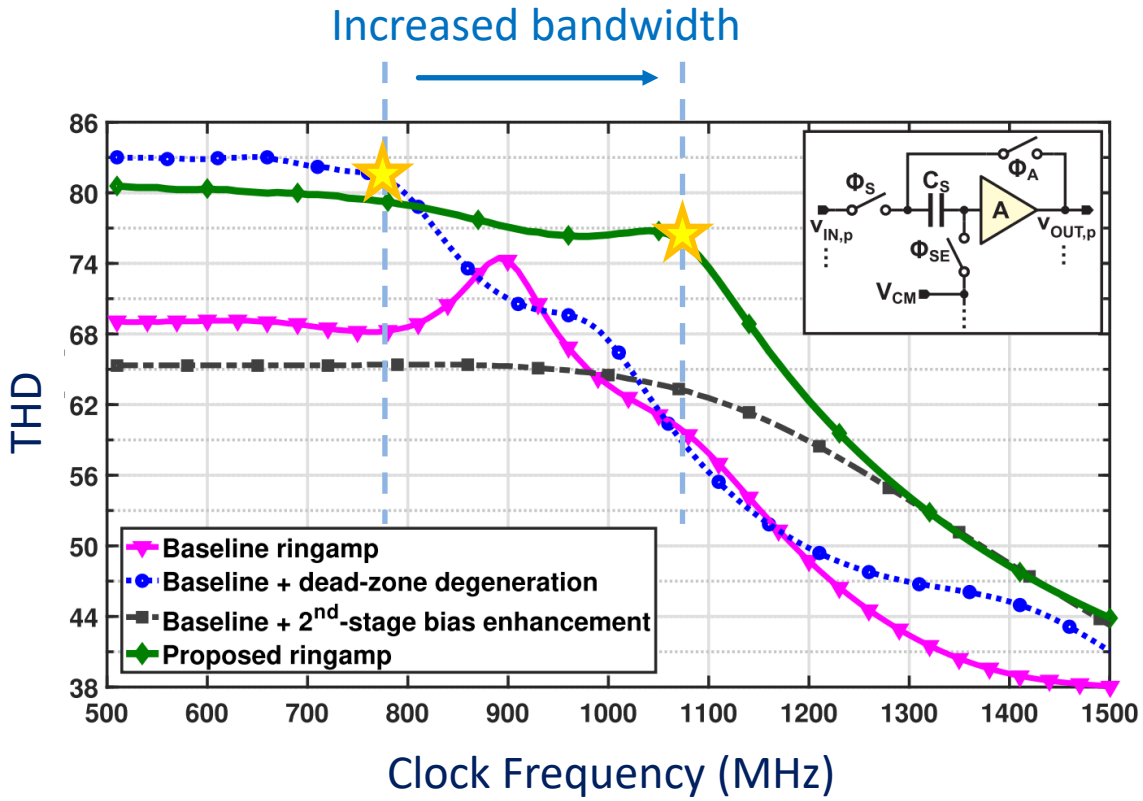
BIAS-ENHANCEMENT

SPEED ENHANCEMENT

- **Idea:** use additional signal splitting to boost V_{OV} and g_m of internal stage

[Chen, TCASII 2017]
[Lagos, JSSC Mar. 2019]





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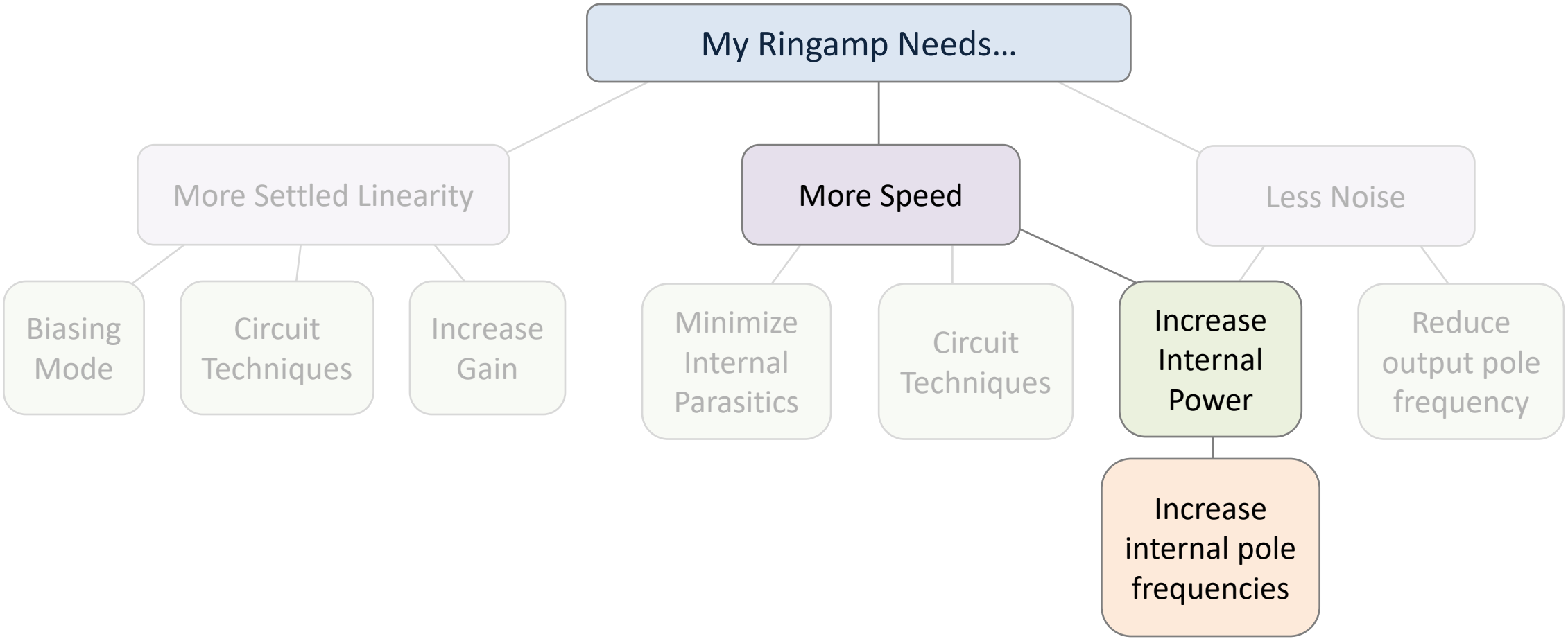

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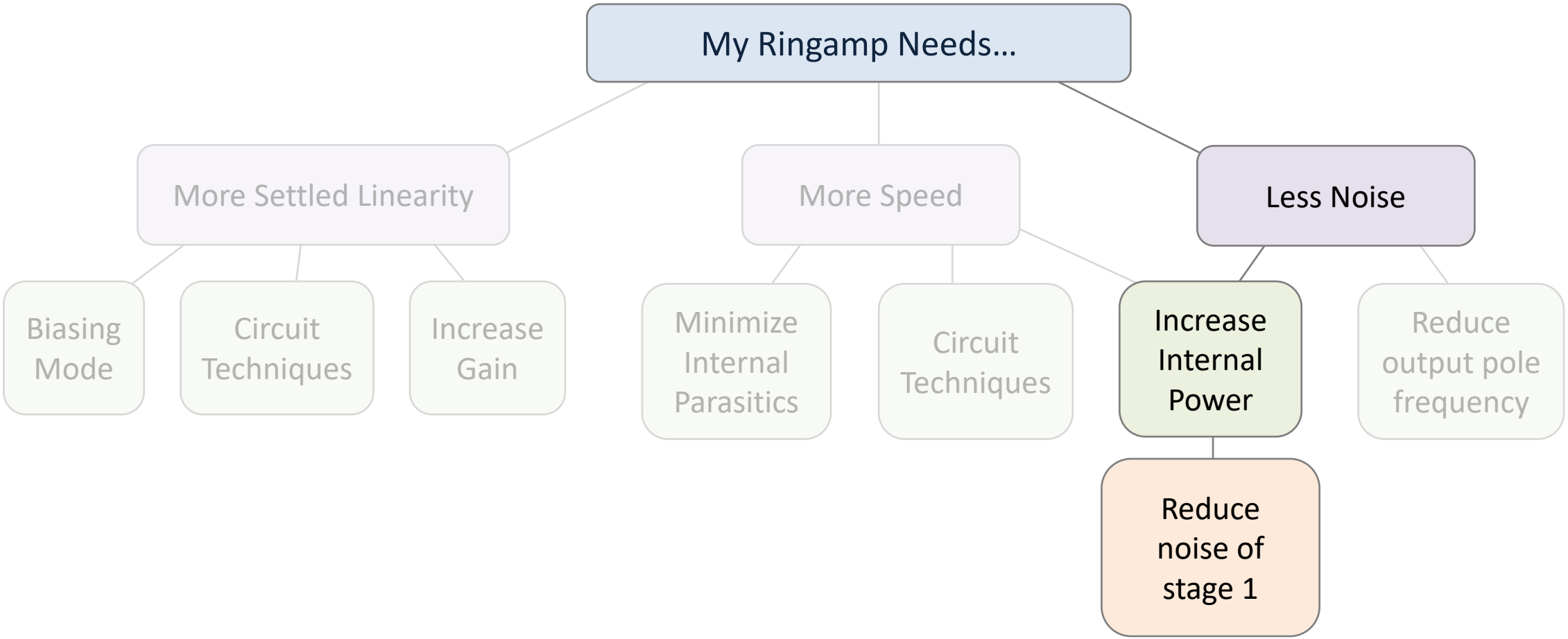

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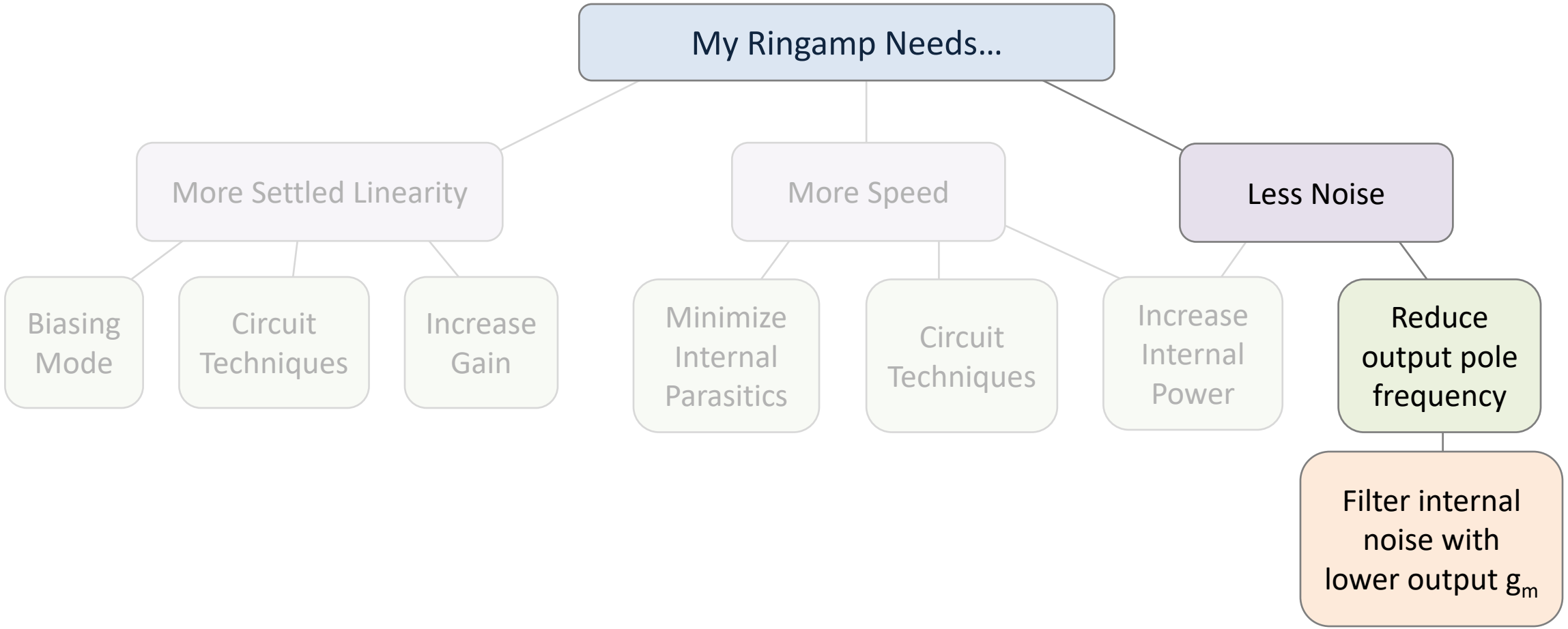
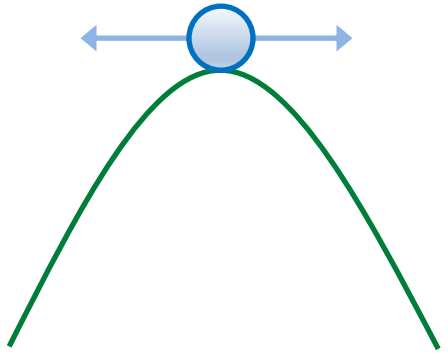


PVT CONSIDERATIONS

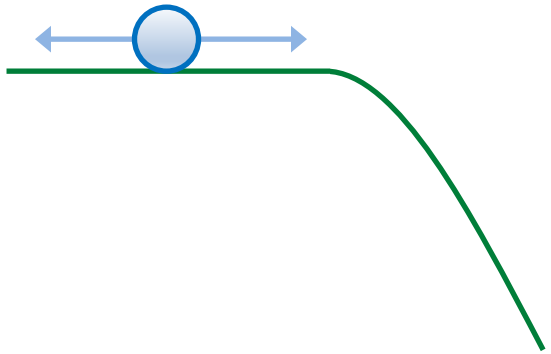
FEEDBACK MAKES LIFE EASIER

PVT CONSIDERATIONS

- Open-loop amplifier (e.g. Gm-C integrator)
  - *Like balancing a ball on a hill*
  - No feedback to suppress parameter variation
    - *E.g. open-loop residue gain*



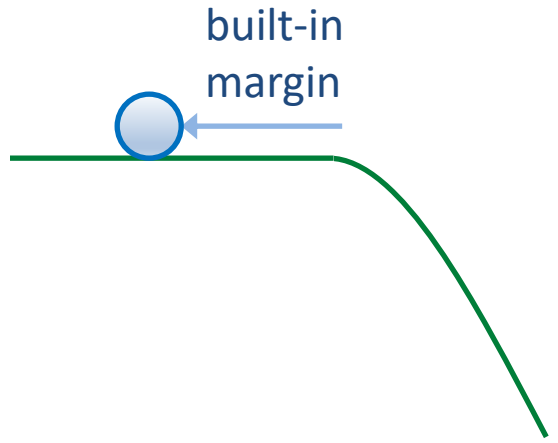
- Ring amplifier
  - *Like placing a ball safely away from the edge*
  - Feedback suppresses parameter variation
  - But only as good as the feedback itself
    - Loop gain, bandwidth, stability



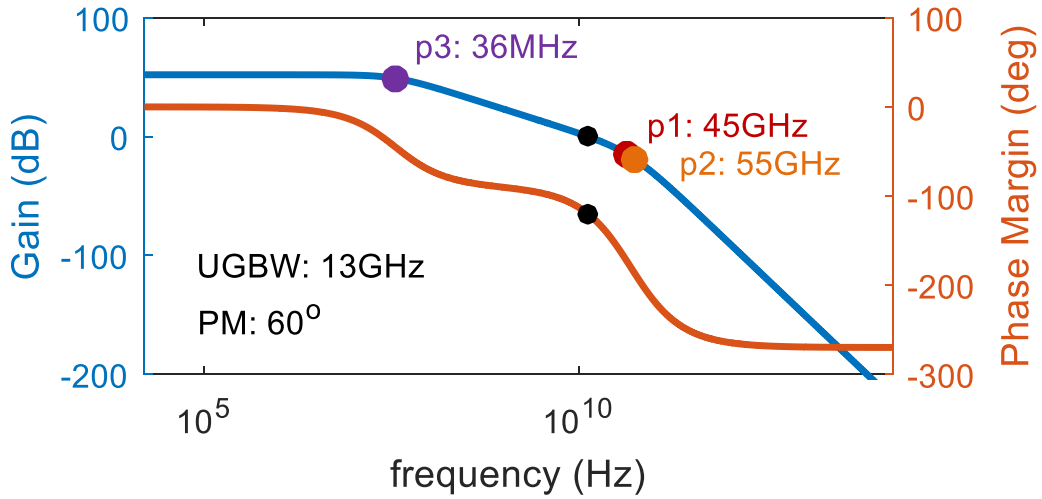
APPROACH 1: ROBUST-BY-DESIGN

PVT CONSIDERATIONS

- Calibration-free approach
  - Include extra margin to pass all corners
  - Sacrifice some efficiency / speed



- Options for increasing phase margin
  - Move internal poles higher
    - More power
  - Move external pole lower
    - Less speed



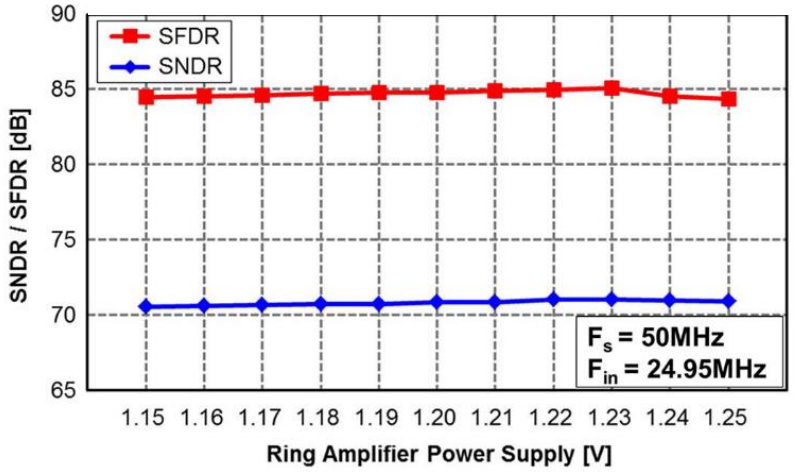
APPROACH 1: ROBUST-BY-DESIGN

PVT CONSIDERATIONS

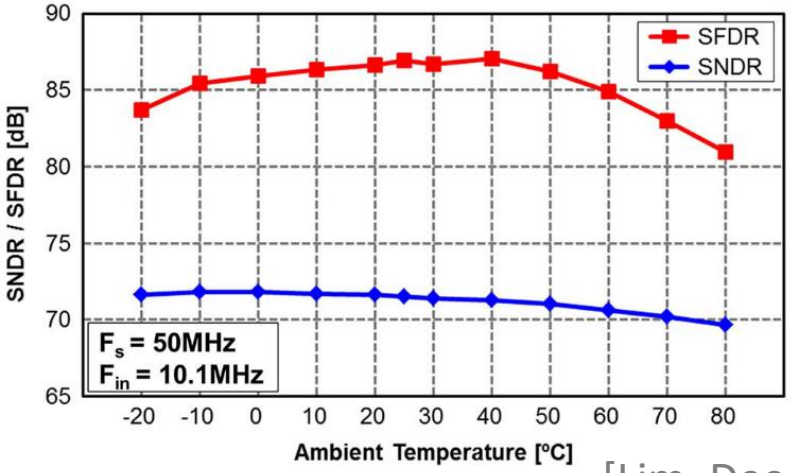
- Calibration-free approach
  - Include extra margin to pass all corners
  - Sacrifice some efficiency / speed

- Calibration-free ringamp ADCs
  - [Hung, ISSCC 2020]
    - 100MS/s, 71.7dB SNDR, 2.2fJ/c-step FoM_W
  - [Lim, JSSC Dec. 2015]
    - 50MS/s, 70.9dB SNDR, 6.9fJ/c-step FoM_W
  - [Lim, VLSI 2017]
    - 100MS/s, 73.2dB SNDR, 6.1fJ/c-step FoM_W

Power supply +/- 50mV



Temperature -20°C – 80°C



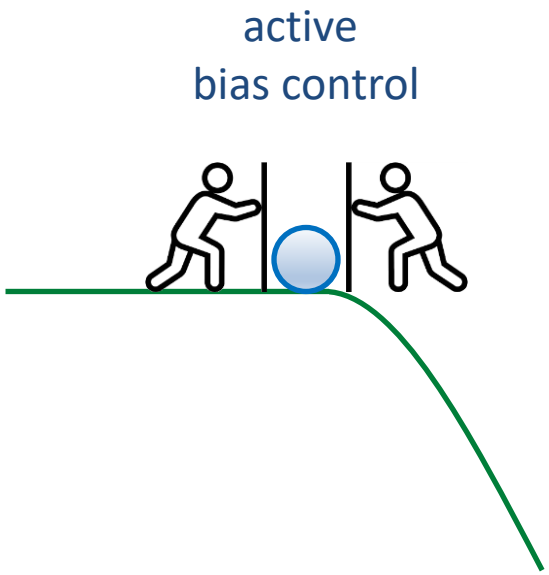
[Lim, Dec. JSSC 2015]

APPROACH 2: CALIBRATION

PVT CONSIDERATIONS

- Calibration-based approach
  - Use feedback to maintain optimal biasing
  - Top performance
  - More analog design freedom
  - More digital complexity ☹

- Calibration-based ringamp ADCs
  - [Hershberg 2019]
    - 3.2GS/s, 61.7dB SNDR, 19.3fJ/c-step FoM_W
  - More to come...



PRACTICAL DESIGN

TRANSIENT-BASED DESIGN & VALIDATION

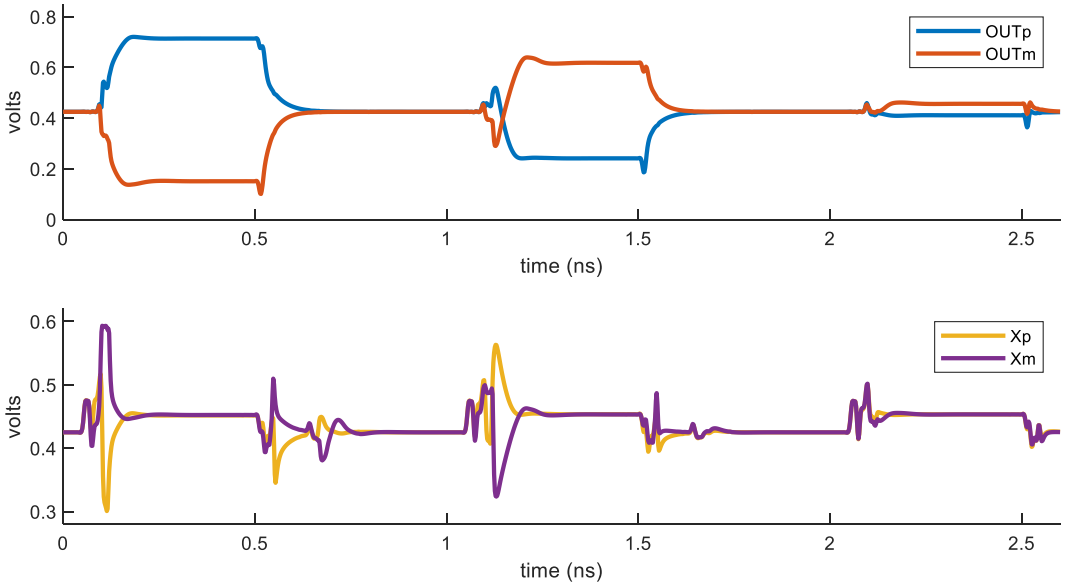
PRACTICAL DESIGN

- Transient-centric design is becoming mainstream
  - All “next-gen” amplifiers: ringamp, Gm-C, Gm-R, Charge-steering, Zero-crossing, etc.
- Modern compute power can handle it
  - Multi-core with APS

METHODS OF ANALYSIS

PRACTICAL DESIGN

- Transient waveform visual inspection
  - Amplifier input nodes particularly useful
- Transient (+noise) FFT of sampled output
  - Exercise full output swing, need enough FFT points
- AC, PAC, PSS, PNOISE where useful
  - But always confirm with transient!



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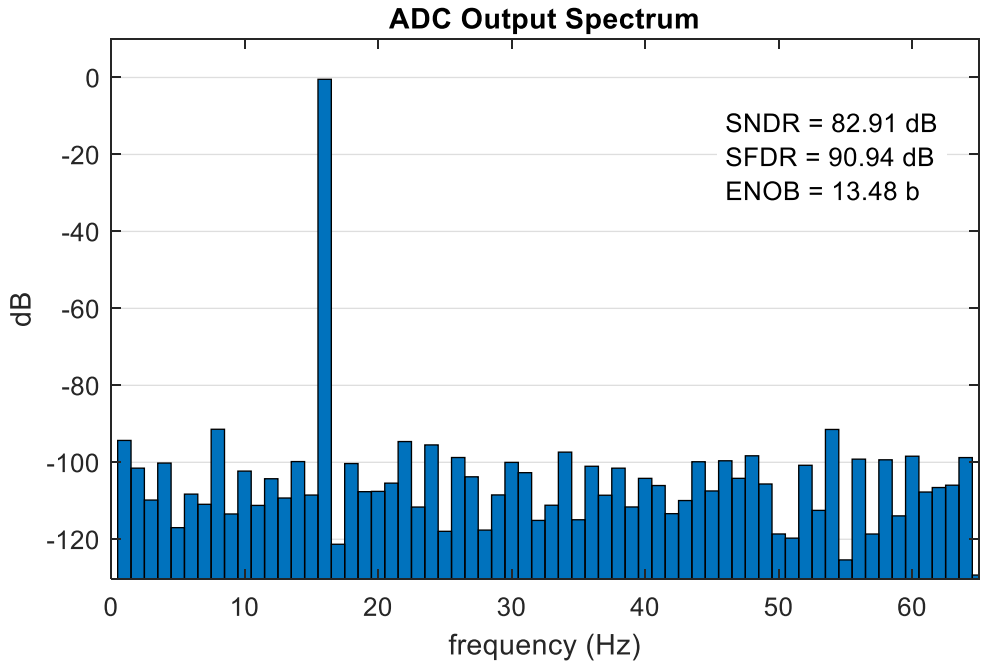


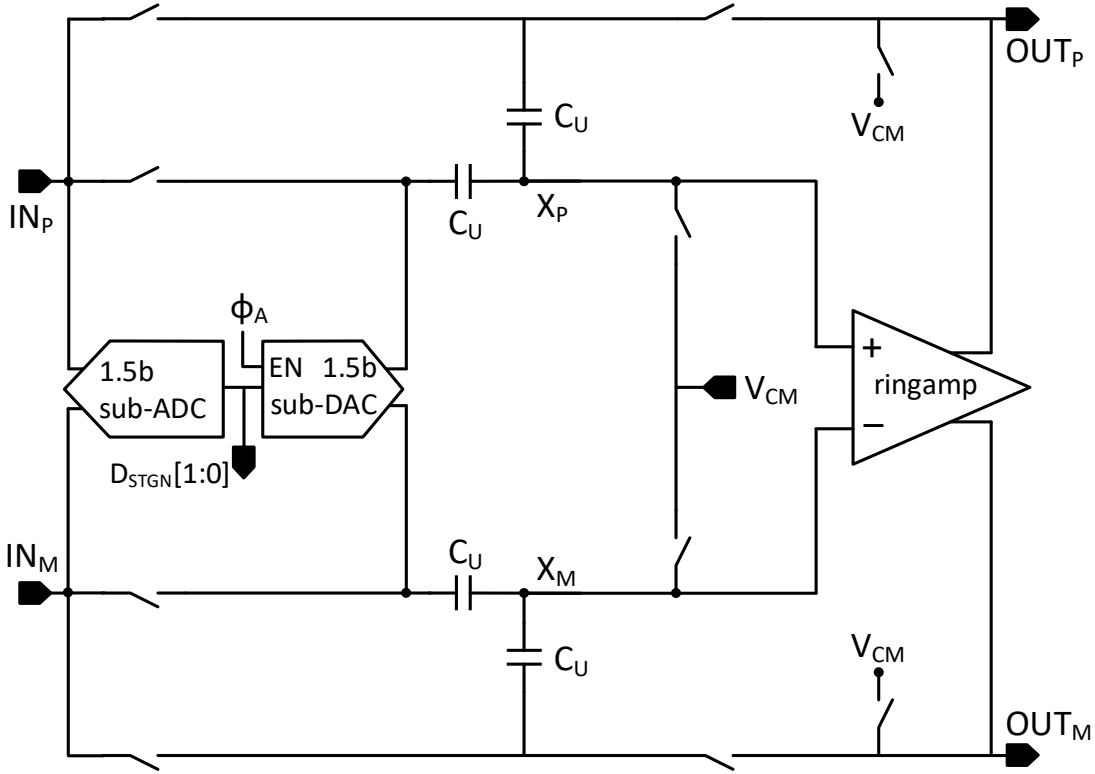
DESIGN PROCEDURE

16NM DESIGN EXAMPLE

- Build in-situ testbench
  - Real switches
  - Actual feedback factor
  - Real output loading
  - Real timing control scheme
  - Estimated parasitics
  - Any other non-idealities

example environment:

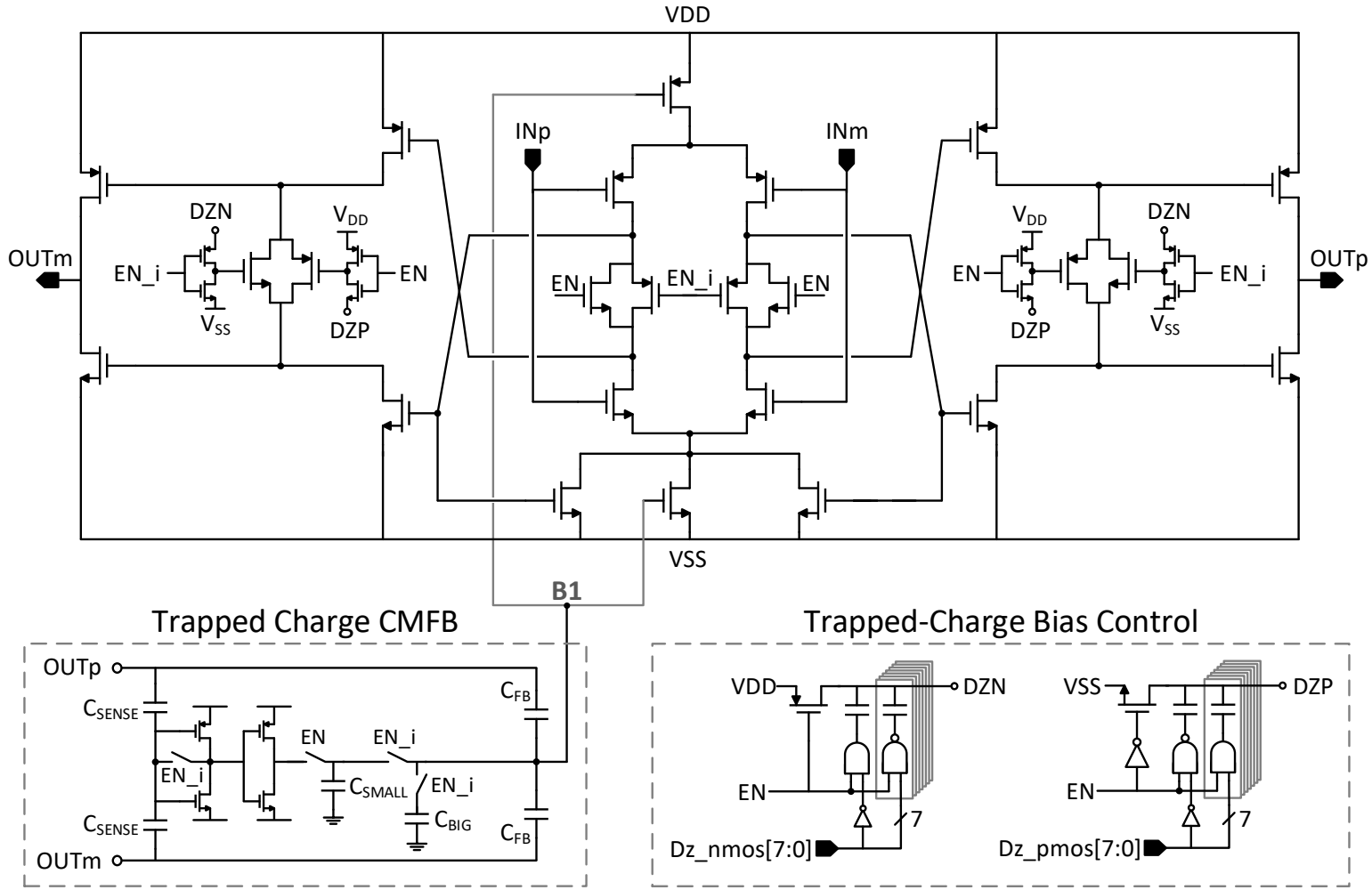
1.5b flip-around MDAC



DESIGN PROCEDURE

16NM DESIGN EXAMPLE

- Fully-differential
- CMOS-resistor
- Bias-enhanced
- Self-resetting
- Multi-path CMFB



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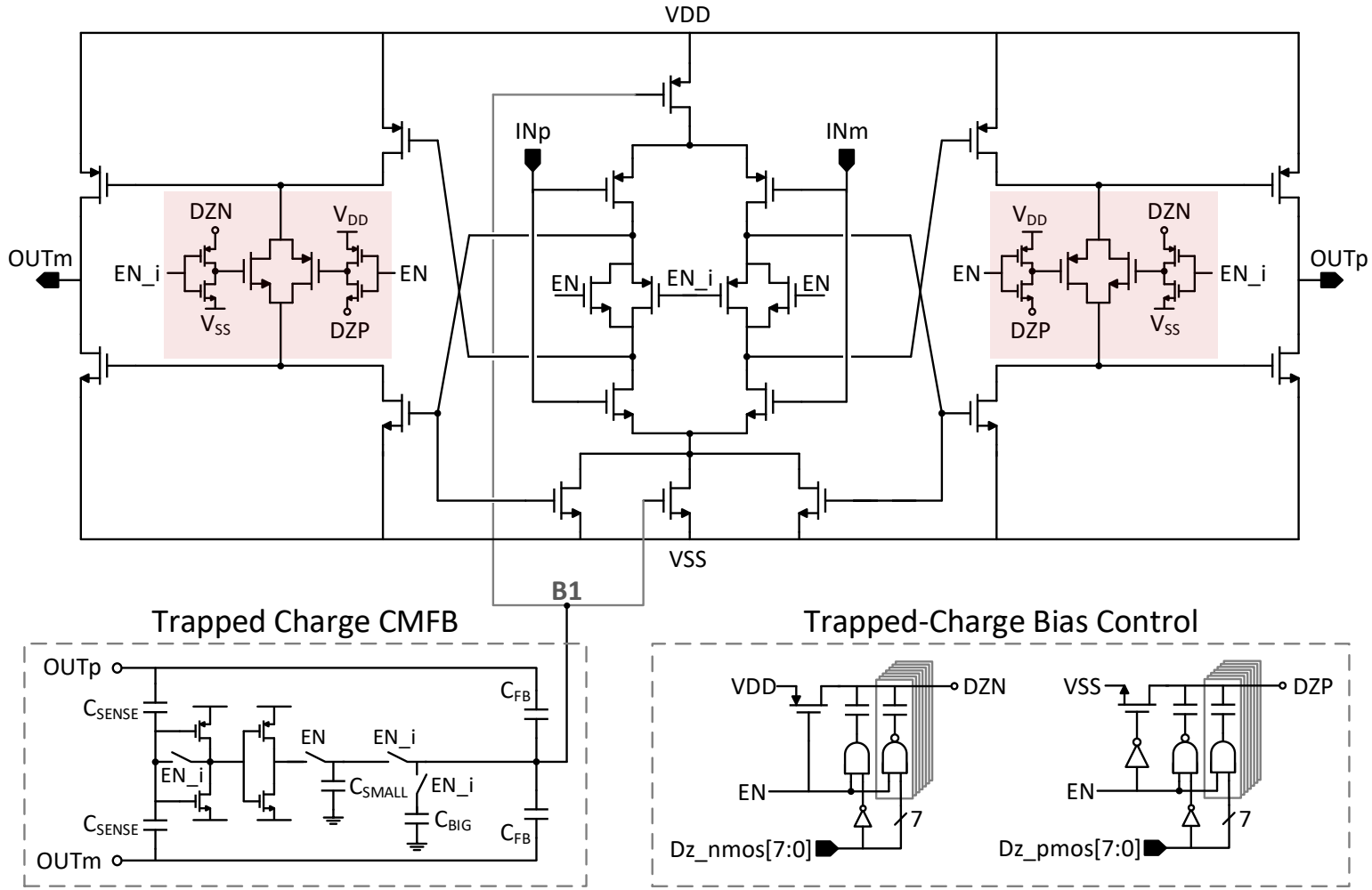

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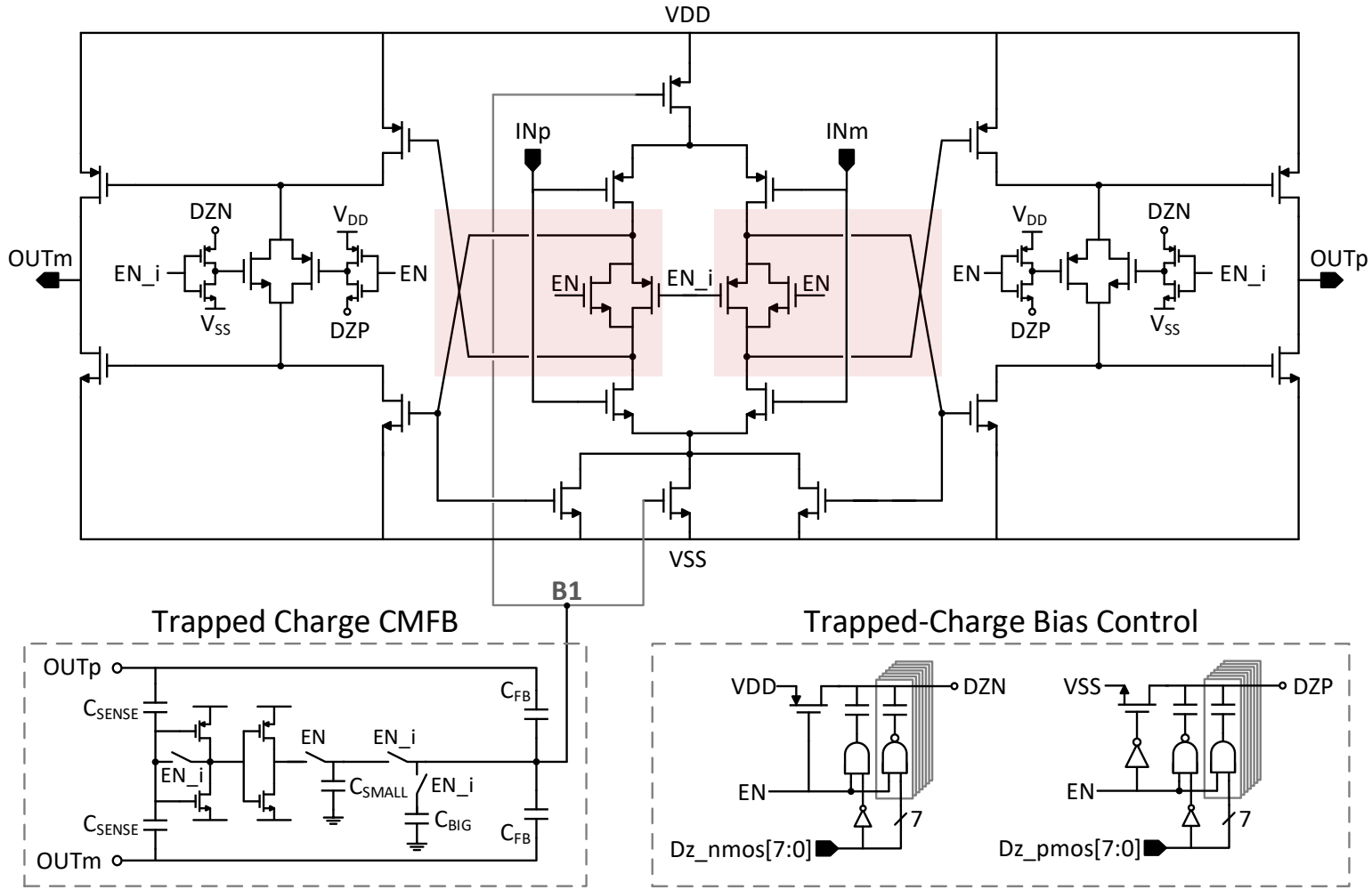

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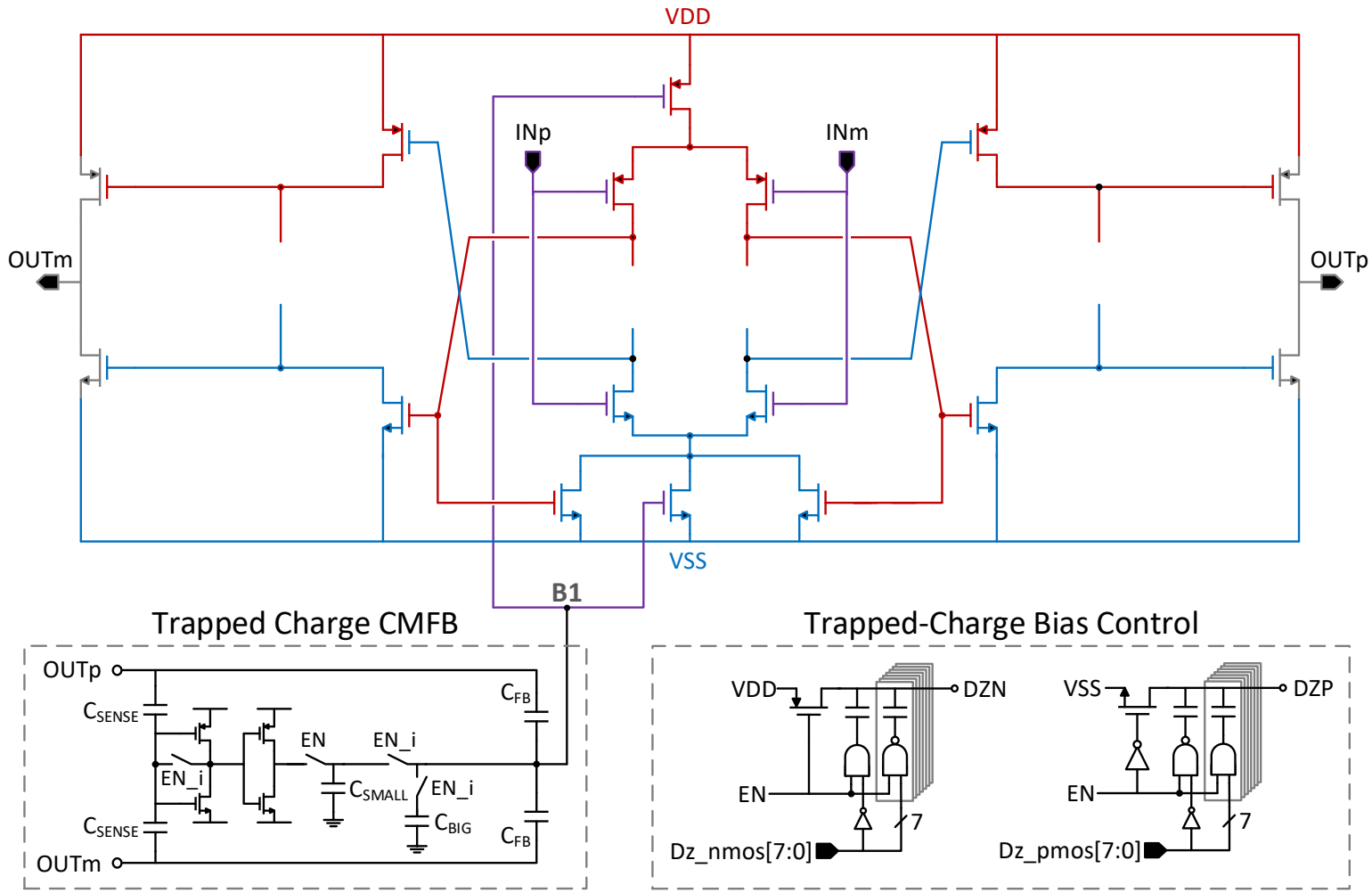

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16NM DESIGN EXAMPLE

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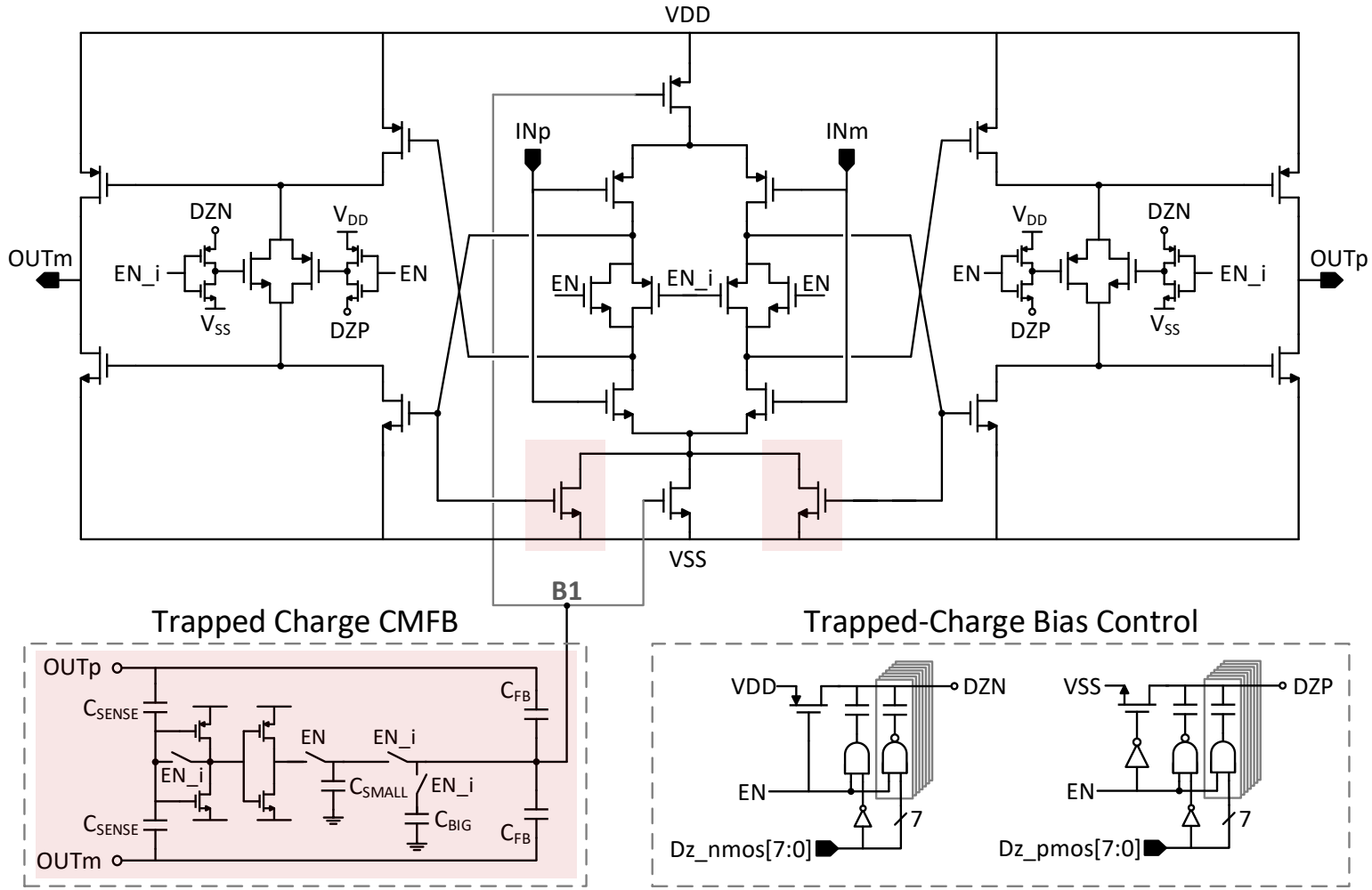
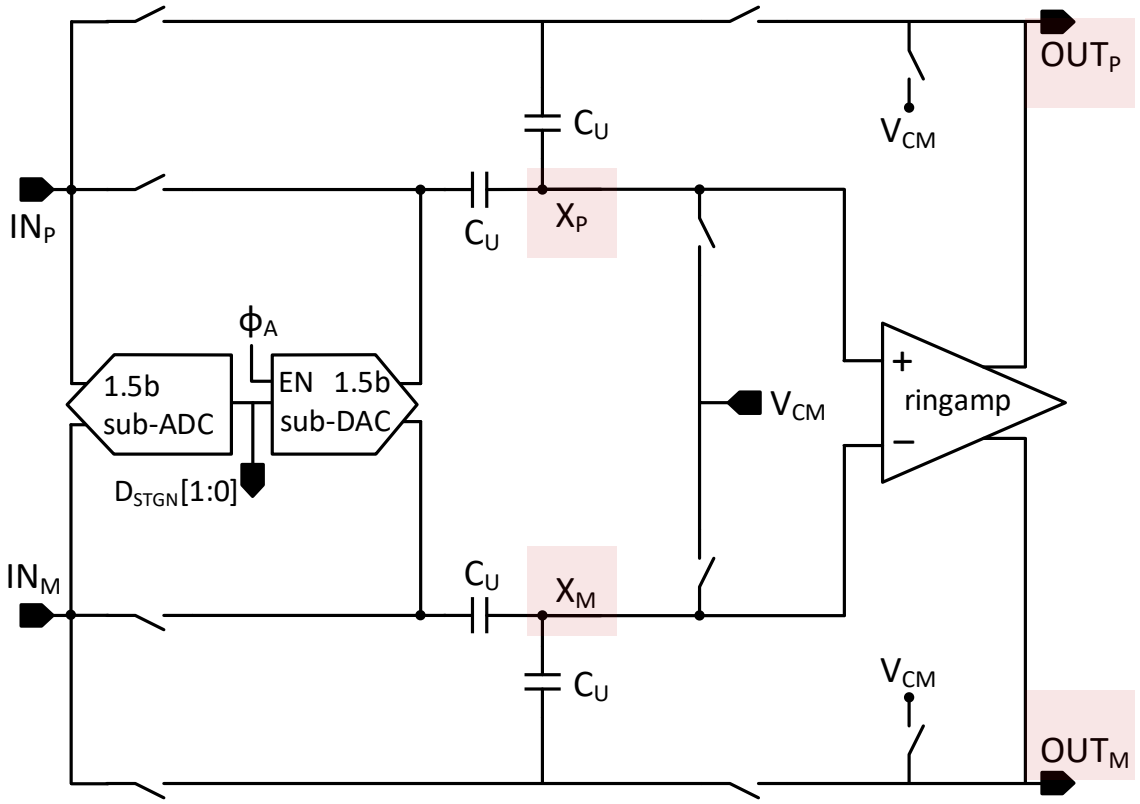
- Bias-enhanced
- Self-resetting
- Multi-path CMFB

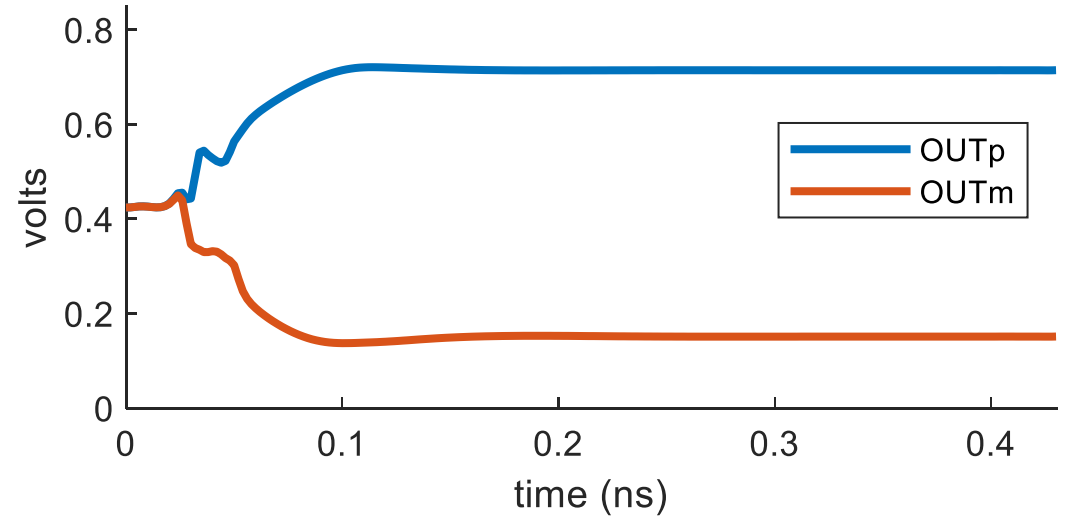


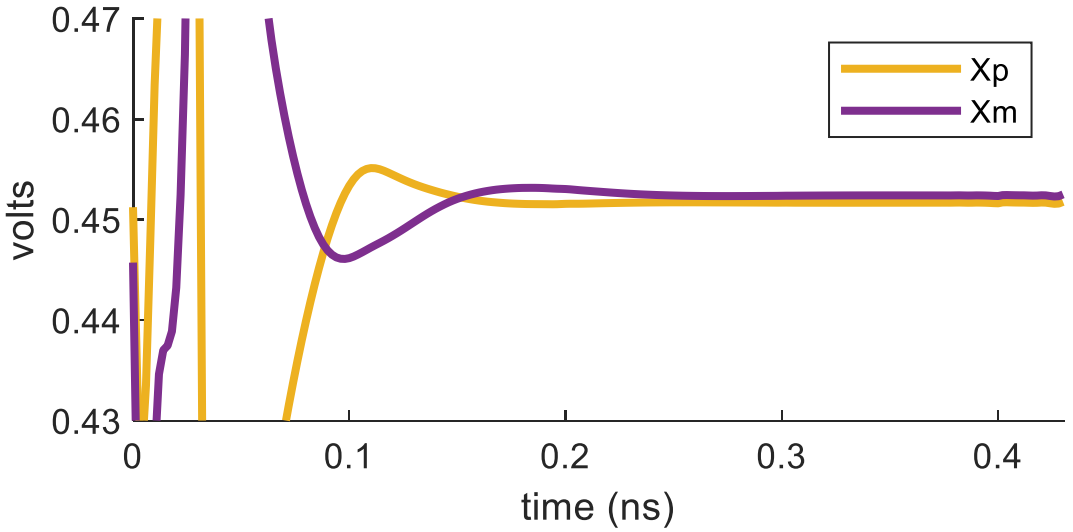
DESIGN PROCEDURE

16NM DESIGN EXAMPLE



Baseline (final design)



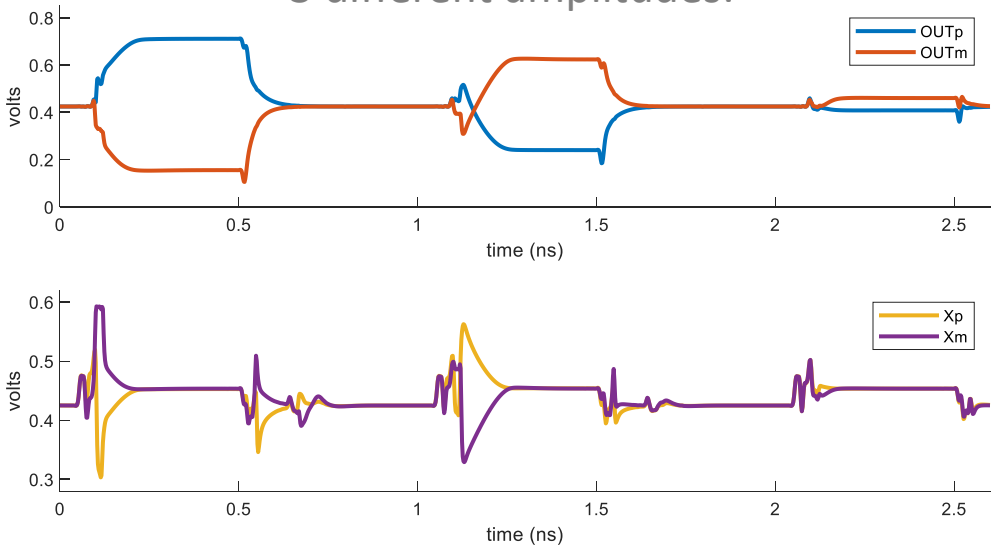


ADJUST DRIVE STRENGTH

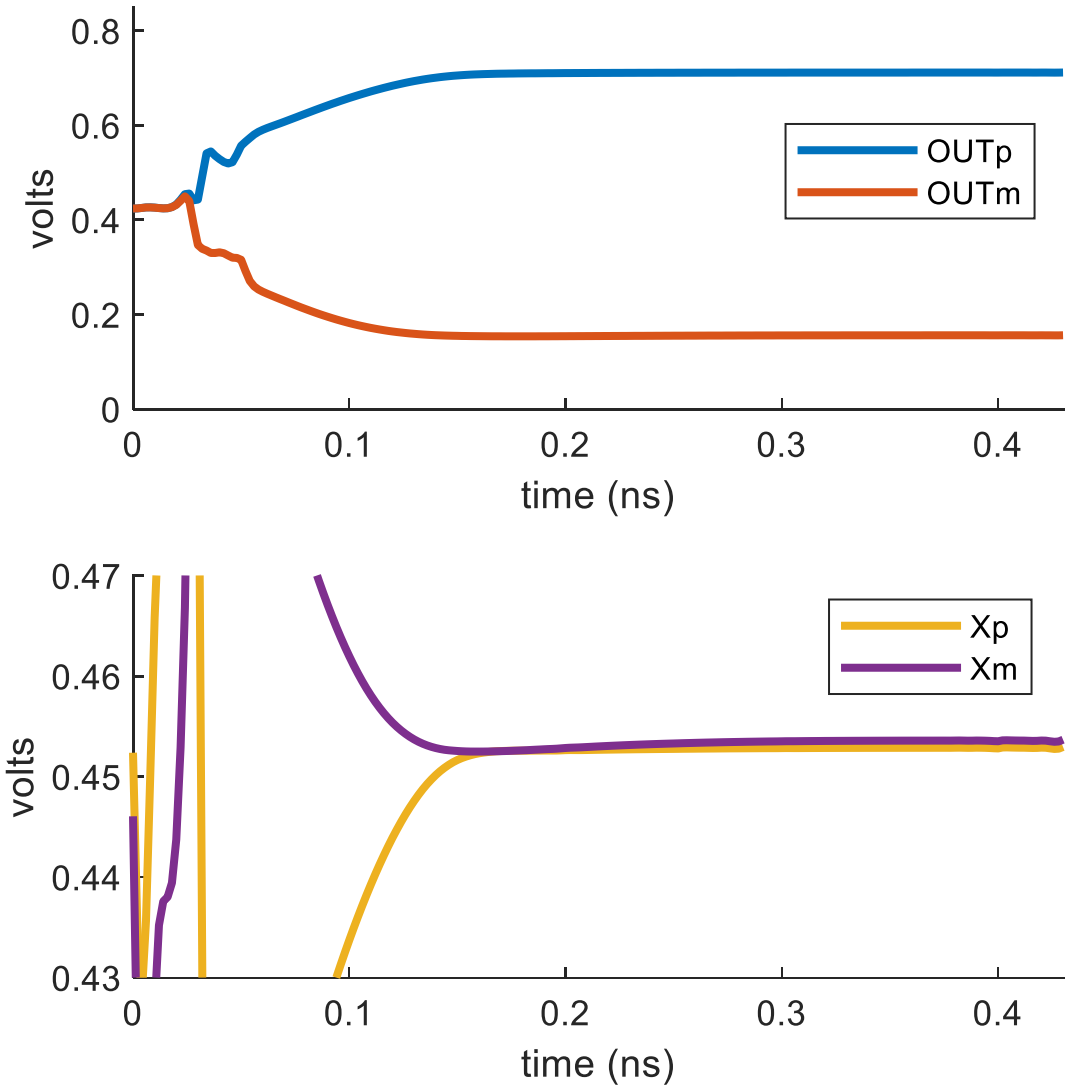
16NM DESIGN EXAMPLE

- Key parameter: output drive strength
  - Smaller: more stable, less internal loading
  - Larger: faster slew

3 different amplitudes:



½x Output Drive

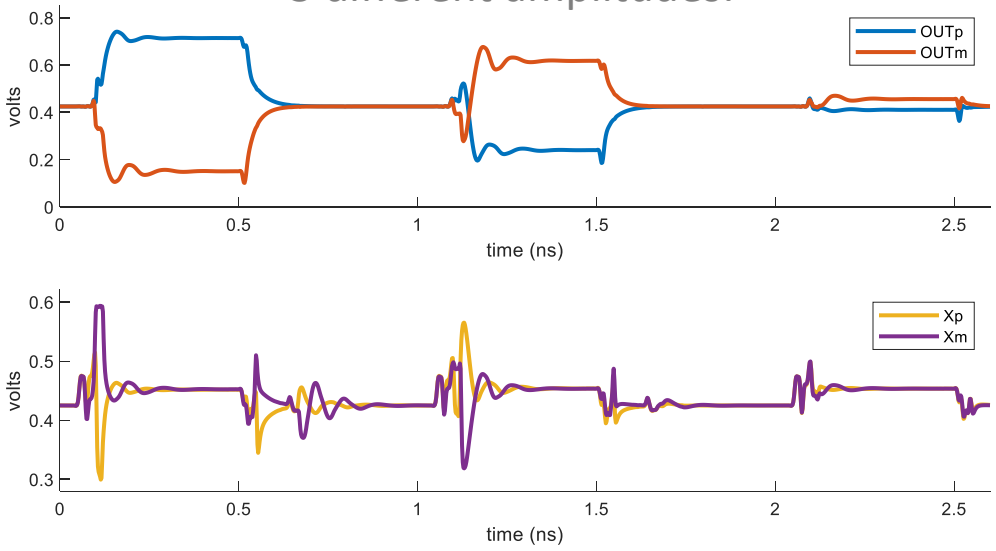


ADJUST DRIVE STRENGTH

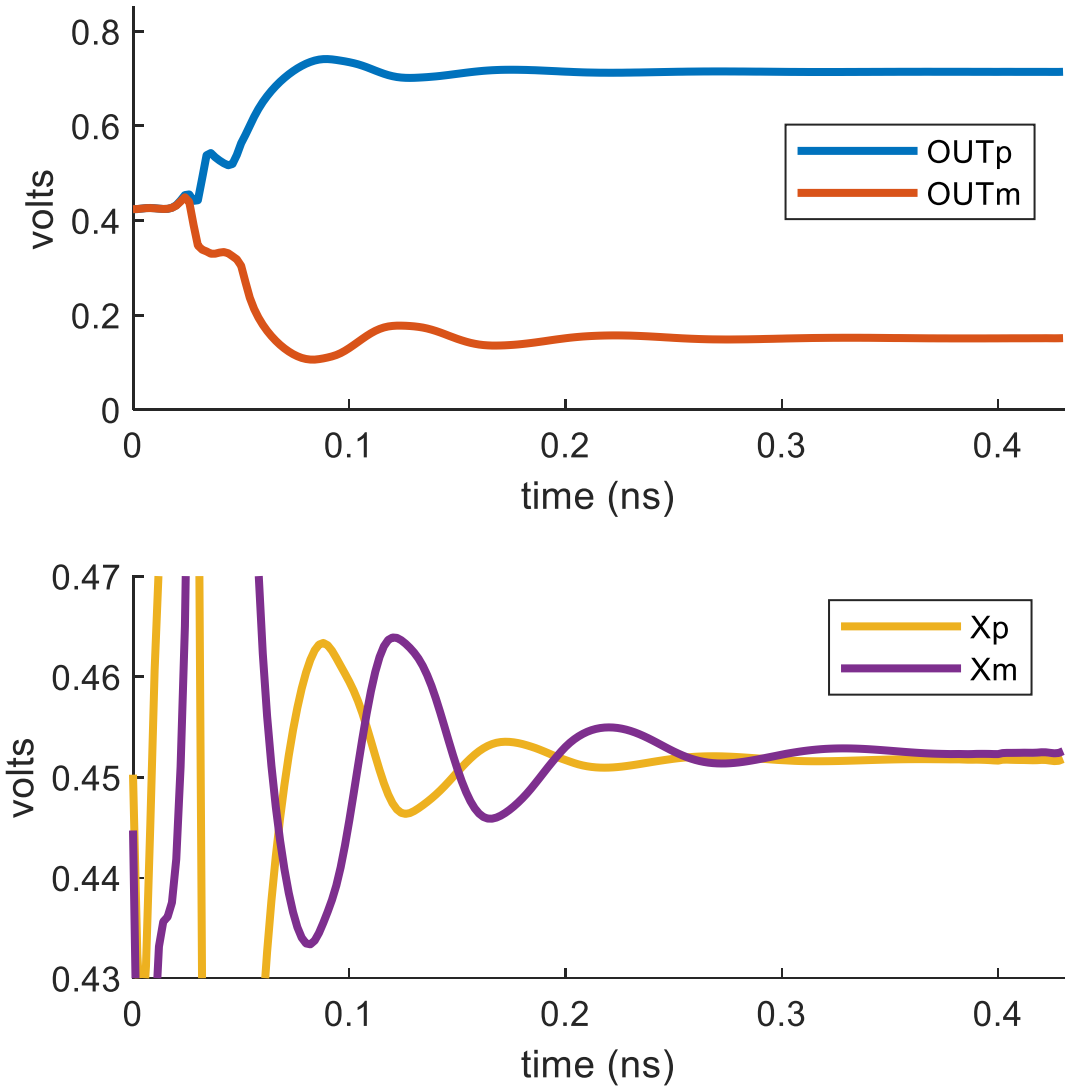
16NM DESIGN EXAMPLE

- Key parameter: output drive strength
  - Smaller: more stable, less internal loading
  - Larger: faster slew

3 different amplitudes:



2x Output Drive

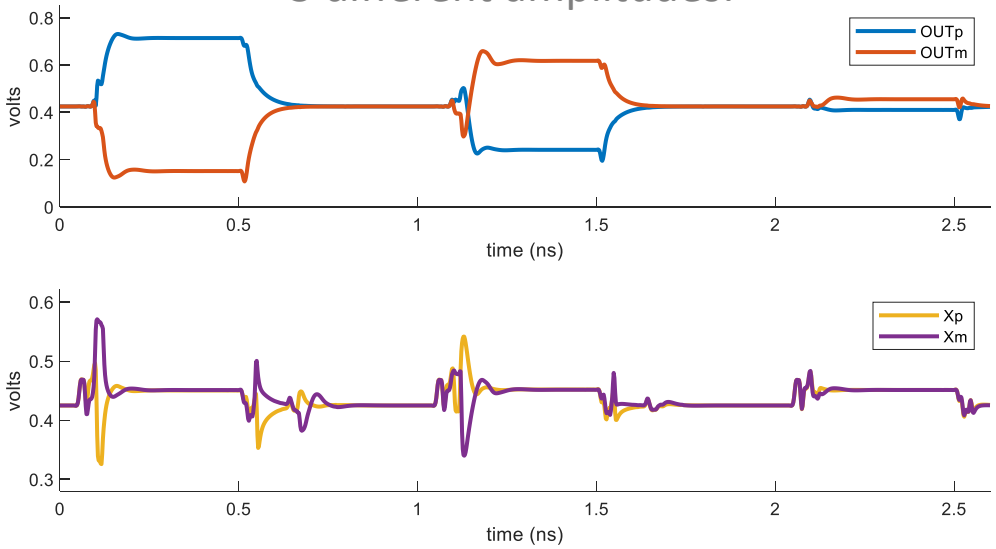


ADJUST DRIVE STRENGTH

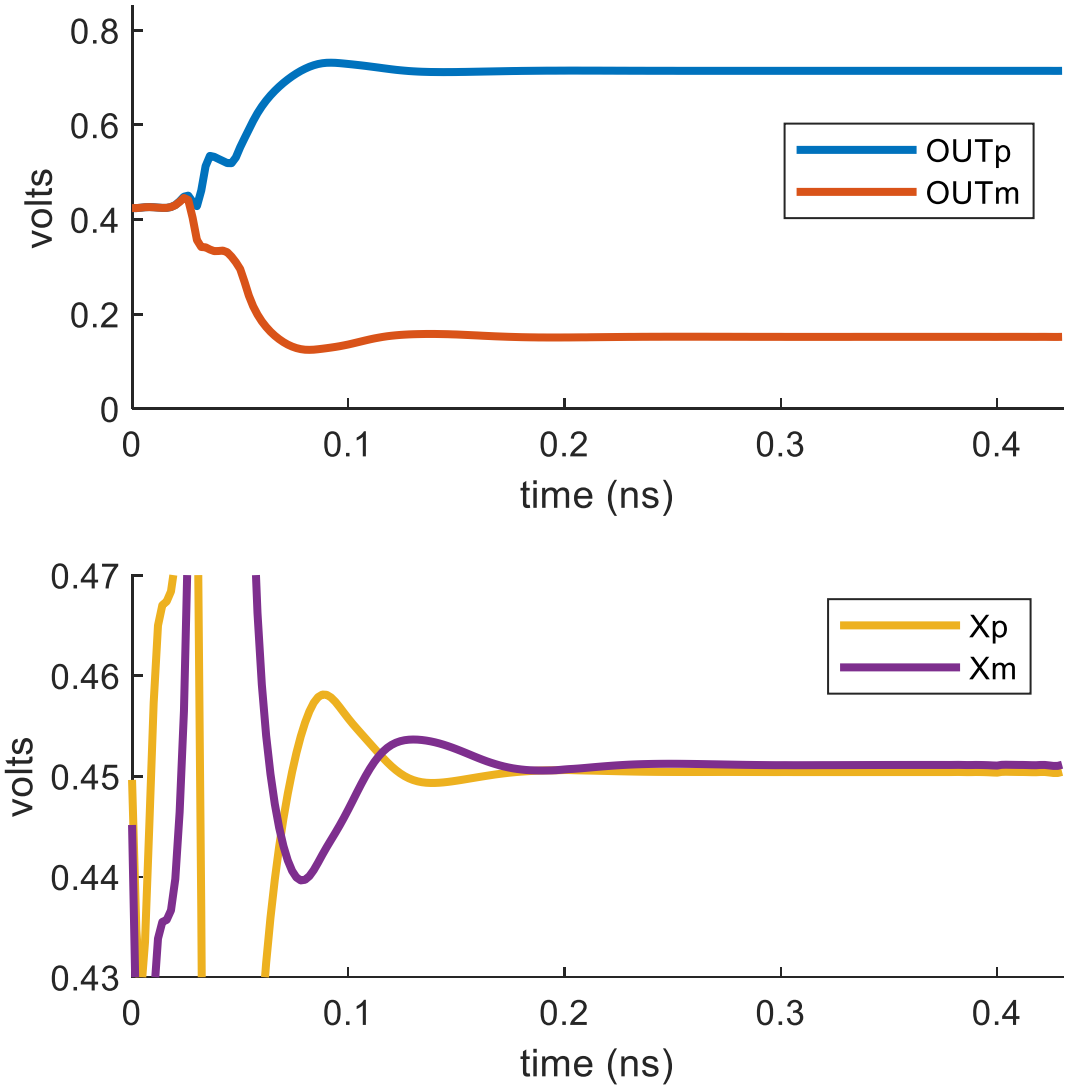
16NM DESIGN EXAMPLE

- Key parameter: internal stage sizes
  - Smaller: more efficient
  - Larger: faster

3 different amplitudes:



2x All Stages

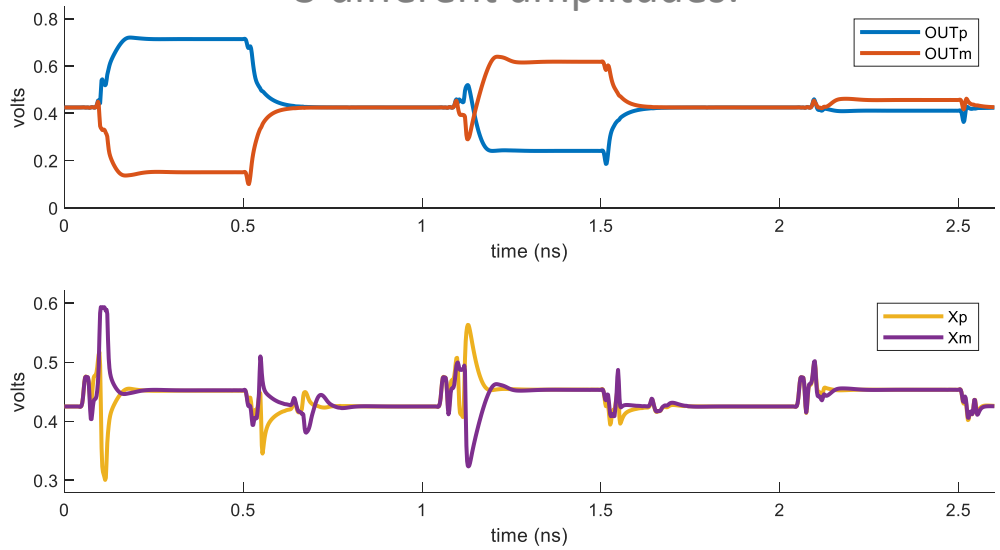


ADJUST DEADZONE

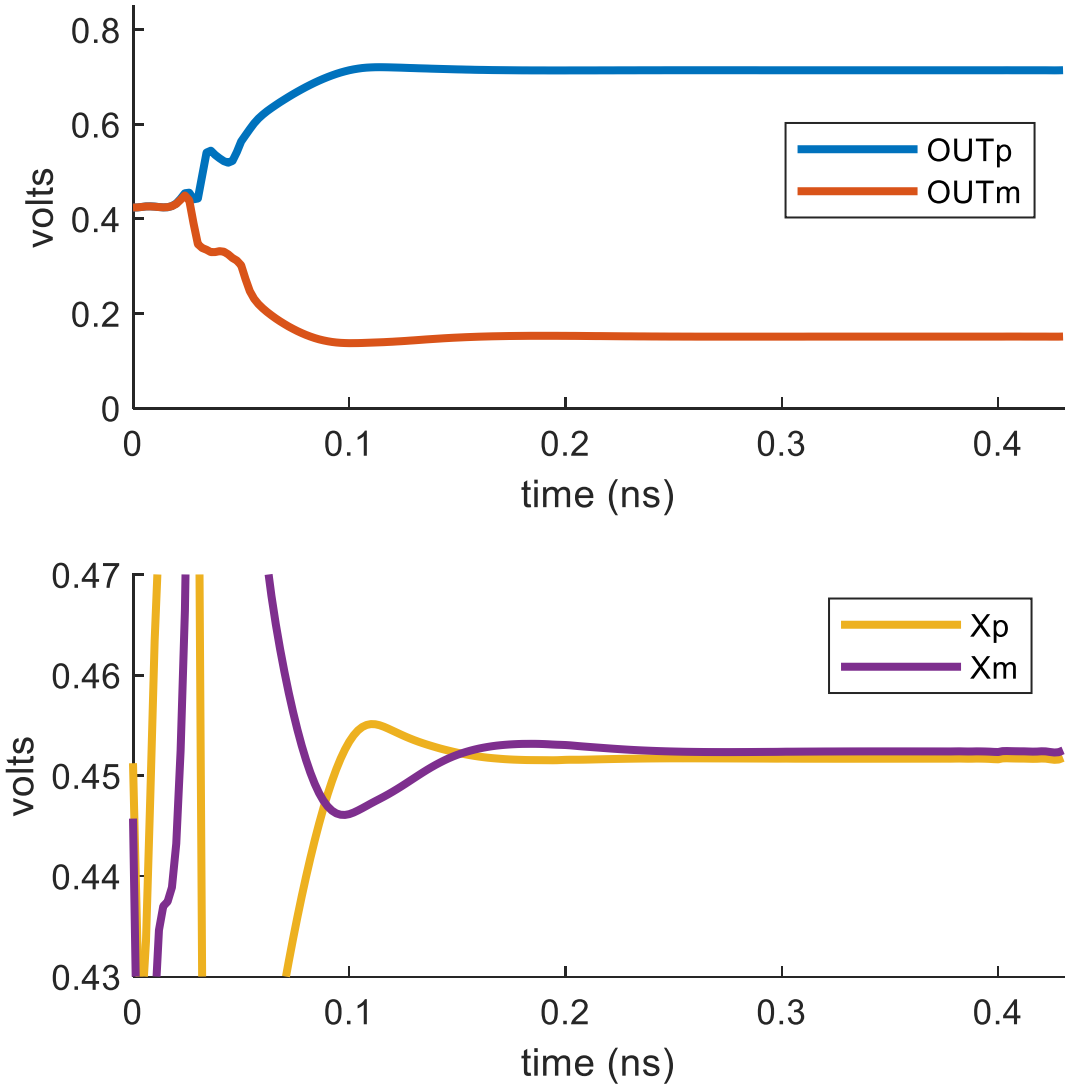
16NM DESIGN EXAMPLE

- Key parameter: dead-zone biasing
  - Smaller: faster settling
  - Larger: more stable

3 different amplitudes:



Optimal dead-zone

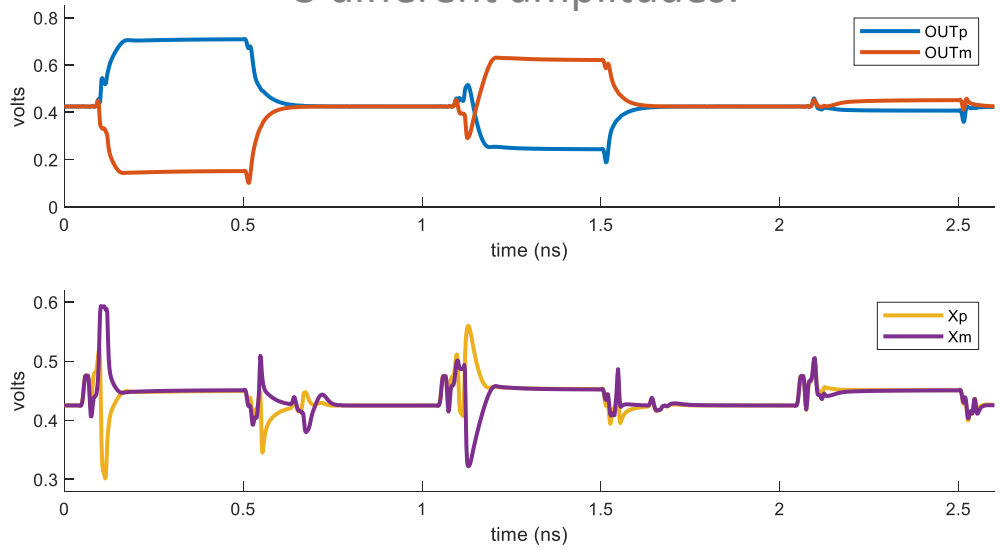


ADJUST DEADZONE

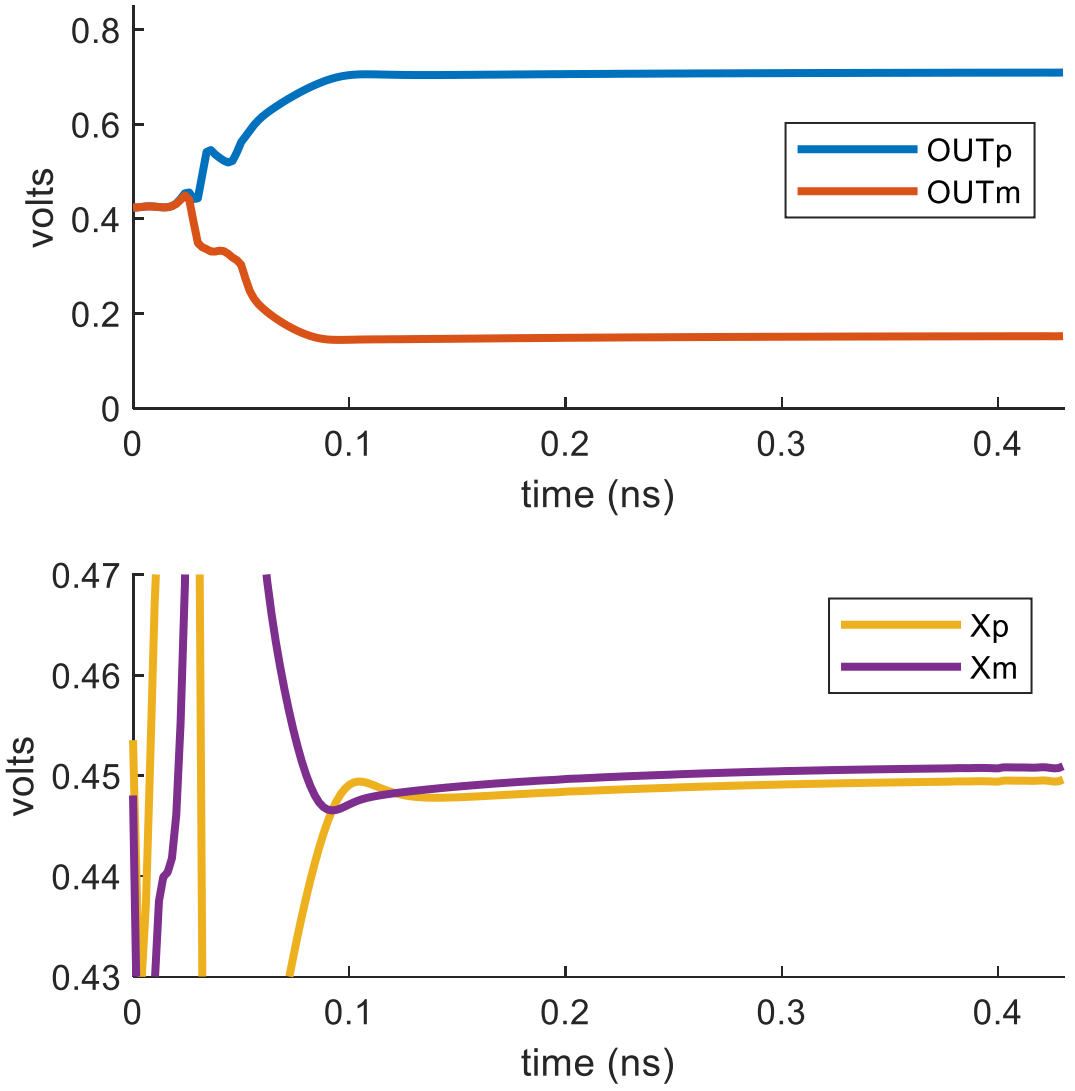
16NM DESIGN EXAMPLE

- Key parameter: dead-zone biasing
  - Smaller: faster settling
  - Larger: more stable

3 different amplitudes:



Dead-zone too large

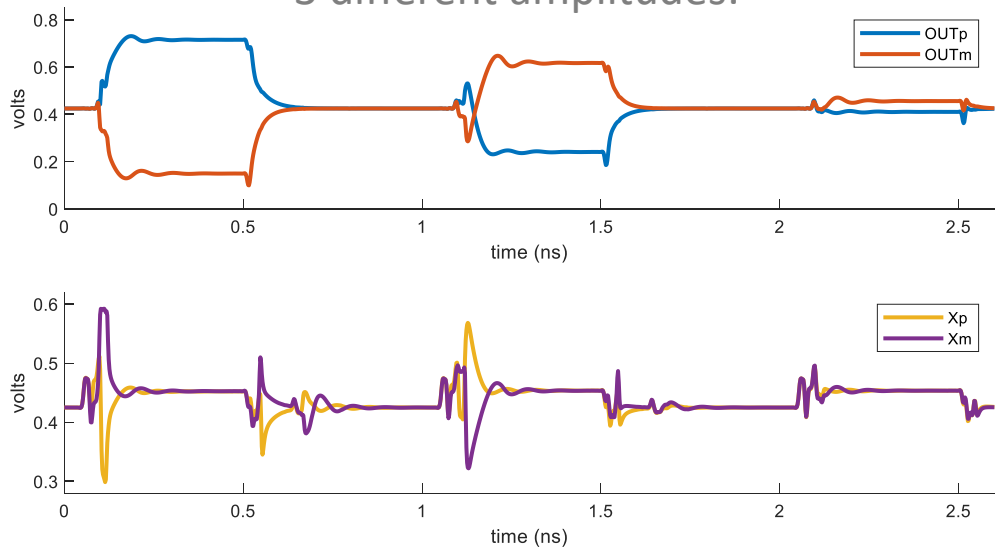


ADJUST DEADZONE

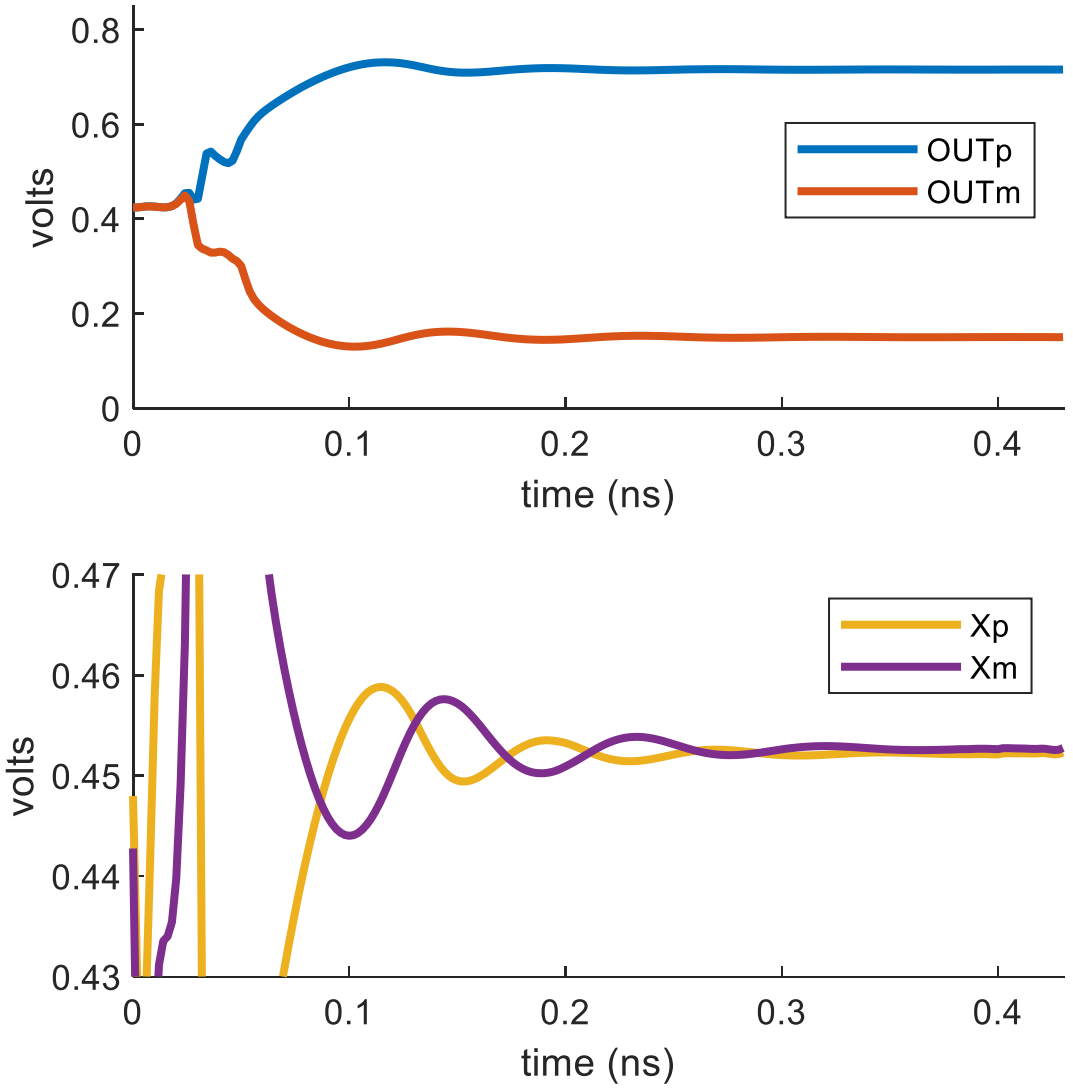
16NM DESIGN EXAMPLE

- Key parameter: dead-zone biasing
  - Smaller: faster settling
  - Larger: more stable

3 different amplitudes:



Dead-zone too small



EXAMPLE DESIGN PROCEDURE

PRACTICAL DESIGN

1. Build in-situ testbench with realistic timing & feedback conditions
2. Initialize ringamp with over-designed front stages (extra bandwidth)
3. Size output stage to balance worst-case slew rate / settling time (approx. 50/50)
4. Down-scale front stages for power efficiency (e.g. 4:2:1)
5. Iterate from #3 as necessary

Ultimately, the best design procedure depends on many factors, e.g. optimization priorities and application type. With practice will come intuition and insight. This is the art of analog design!

REVITALIZING THE ECOSYSTEM

REVITALIZING THE ECOSYSTEM

CONCLUSIONS

Ringamps remove the amplifier bottleneck...

more architectural freedom

amplifier-intensive techniques

new applications

...and diversity is increasing

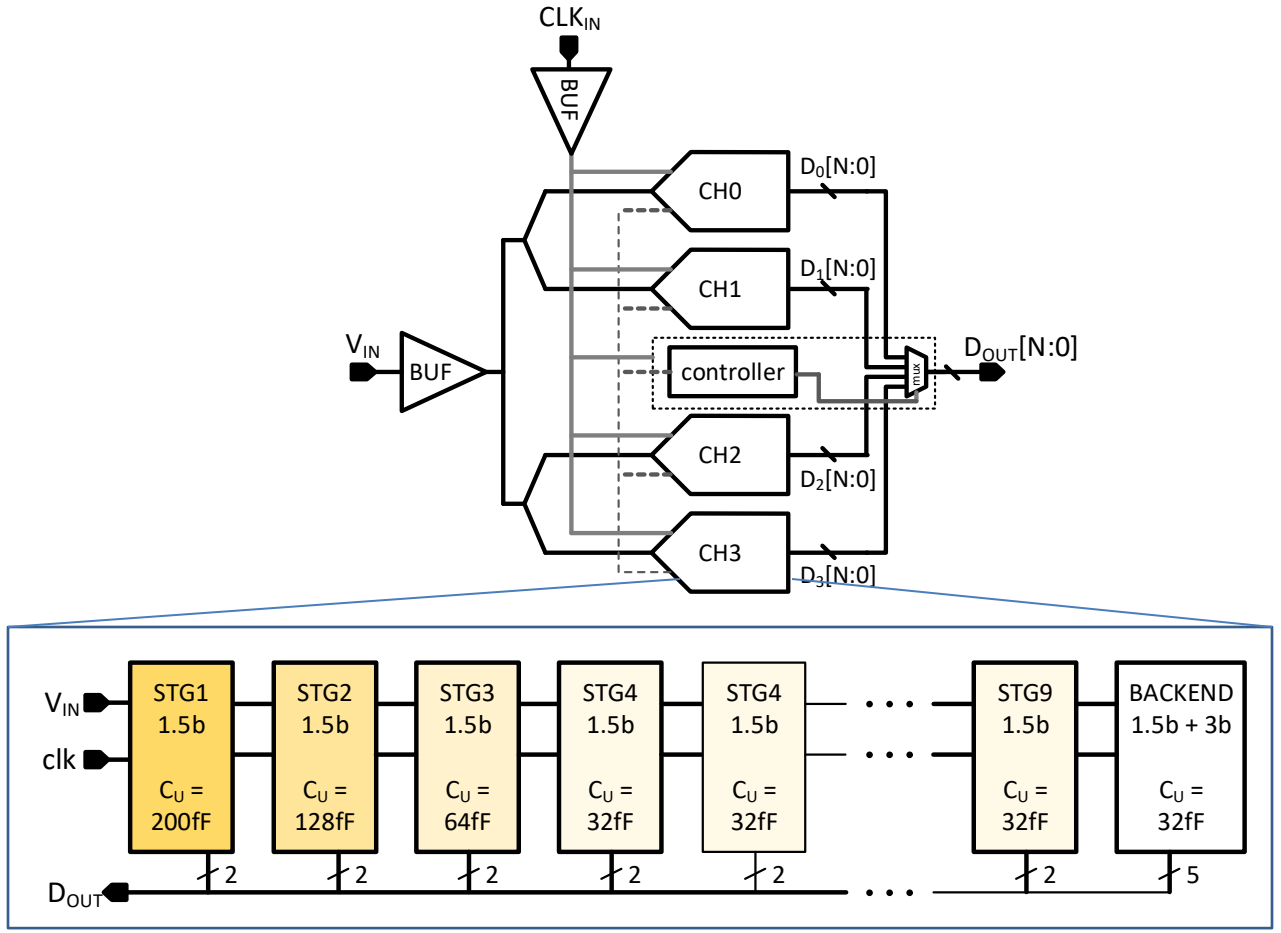
REVITALIZING THE ECOSYSTEM

CASE STUDY

[Hershberg, ISSCC 2019 (1)]

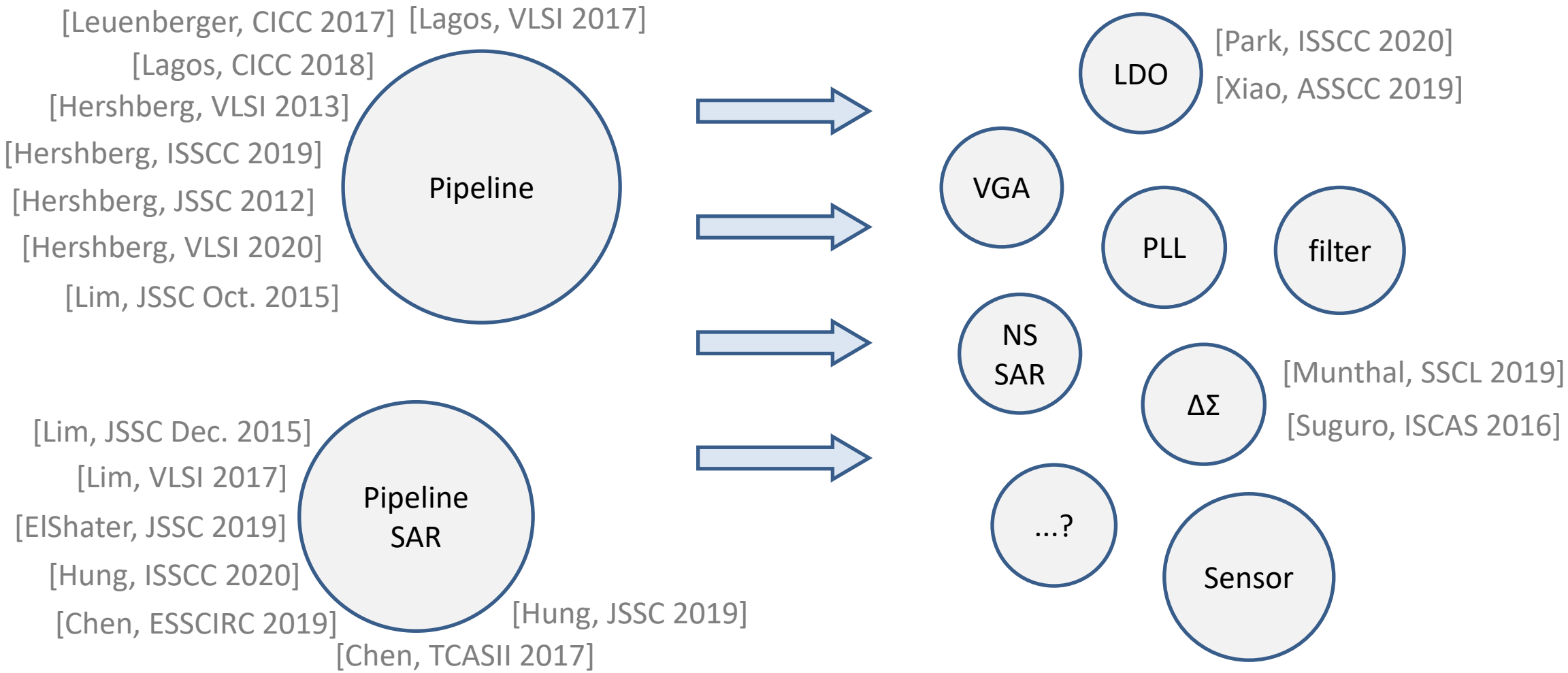
System	3.2 GS/s
Channel	800 MS/s
SNDR	63 dB
SFDR	80 dB
Power	61.3 mW
FoM_W	19 fJ/cs

- Order-of-magnitude improvement in direct-RF sampling ADC SoTA
- 36 ringamps in system
  - Very amplifier intensive



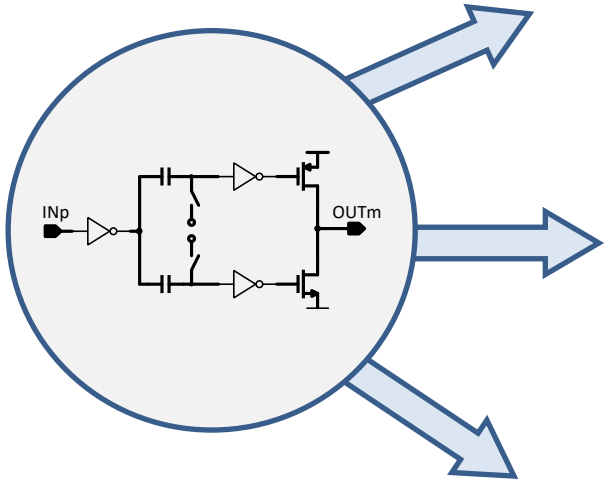
REVITALIZING THE ECOSYSTEM

RINGAMP DESIGNS WITH MEASURED SILICON



REVITALIZING THE ECOSYSTEM

RINGAMP TOPOLOGY DIVERSIFICATION



Rapid Reset
[T.C.Hung, ISSCC 2020]

Bias-Enhanced
[Chen, TCASII 2017]

Self-Resetting
[Lagos, JSSC Mar. 2019]

Self-Biased
[Lim, JSSC Oct. 2015]

Closed Loop
Dynamic Amplifier
[Tang, ISSCC 2020]

High Voltage
[ElShater, ISSCC 2019]

Power Management
[Park, ISSCC 2020]

Class B+AB
[Hershberg, VLSI 2013]

REVITALIZING THE ECOSYSTEM

CONCLUSIONS

But is it the scalable amplifier
you've been waiting for?

Depends!

Ringamps are an exciting new tool.

It *could* be the right one for your task.
Decide for yourself! ☺

THANK YOU FOR YOUR ATTENTION!