Ringamp: The Scalable Amplifier We’ve All Been Waiting For?

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Some ADC architectures have thrived and expanded.

SAR

VCO-based

CT $\Delta \Sigma$
Others have lost ground, forced into niche applications.

- Pipeline
- Folding Flash
- Algorithmic
- DT ΔΣ
- Sub-Ranging
The reason?

... a hidden bottleneck:

Residue Amplification
What did we lose in diversity?

How has this constrained our solutions?
REPLACING THE OPAMP

PROPOSED SOLUTIONS

Zero-crossing based

Gm-C style Dynamic Amplifier

Gm-R style Dynamic Amplifier

Charge-steering

Inverter based
THE “IDEAL AMPLIFIER” WISHLIST

- High bandwidth
- Fast slewing
- Performance scales like digital CMOS
- class-AB
- Fully dynamic (switchable)
- Speed
- Accuracy
- Efficiency
- Cost

No solution can tick all the circles yet...

- High linearity
- High gain
- Low noise
- Rail-to-rail output swing
- Small area
- Low design effort

Speed
Accuracy
Efficiency
Cost
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what else can we try?
RING OSCILLATOR
IN SWITCHED CAPACITOR FEEDBACK

Example MDAC Feedback Structure

$V_{CMX} = 0.6\text{V}$

$V_{IN}$

$\pm V_{REF}$

$V_{OUT}$

$C_{LOAD}$

$V_{CMO}$

RST
RING OSCILLATOR
IN SWITCHED CAPACITOR FEEDBACK

Example MDAC Feedback Structure

\[ V_{CMX} = 0.6 \text{V} \]

(ideal settled input value)

Volts

\[ V_{IN} \]

\[ V_{CMX} = 0.6 \text{V} \]

(time (ns))
RING OSCILLATOR
IN SWITCHED CAPACITOR FEEDBACK

😊 Large gain
😊 Rail to rail swing
😊 Maximal slewing efficiency
😊 Small, simple layout
😊 Inherent class-AB behavior
😊 Fully compatible with digital CMOS

Sounds great! Only one problem...

IT’S AN OSCILLATOR!
Any ring oscillator can be stabilized

It’s just a matter of putting the poles in the right place
RING AMPLIFIER

BASIC PRINCIPLES

- Make $p_1$ & $p_2$ as fast as technology will allow
  - $p_1$ & $p_2$ constrained by technology limits, not $kT/C_{LOAD}$ noise requirement
  - Scales well into nanoscale CMOS

- Stabilize with $p_3$
  - ring oscillator $\rightarrow$ ring amplifier
RING AMPLIFIER

BASIC PRINCIPLES

- But we can do even better
  - Dynamic biasing

Begin very fast but unstable:

![Gain vs Frequency Graph](image)

- **p1**: 45GHz
- **p2**: 55GHz
- **p3**: 1GHz

**UGBW**: 91GHz

**PM**: -32°
RING AMPLIFIER

BASIC PRINCIPLES

- But we can do even better
  - Dynamic biasing

Dynamically shift output pole:

Gain (dB) vs. frequency (Hz)

- p1: 45GHz
- p2: 55GHz
- p3: 1GHz

UGBW: 91GHz
PM: -32°
RING AMPLIFIER

BASIC PRINCIPLES

- But we can do even better
  - Dynamic biasing

Stable steady-state:

Gain (dB)

Phase Margin (deg)

UGBW: 13GHz
PM: 60°

p1: 45GHz
p2: 55GHz
p3: 36MHz
RING AMPLIFIER

BASIC PRINCIPLES

- AC analysis only explains steady-state
  - How do we get to steady state?
  - Do we ever get to steady state?

- Must also consider
  - DC
  - Transient

A “stable” ringamp with 73° phase margin:

[Lim, JSSC 2015]
DYNAMIC LARGE-SIGNAL STABILIZATION

- Split signal into two paths
- Shift DC level (of transient wave) differently in each path
DYNAMIC LARGE-SIGNAL STABILIZATION

\[ V_{\text{DEADZONE}} = 0 \text{mV} \]
DYNAMIC LARGE-SIGNAL STABILIZATION

\[ V_{\text{DEADZONE}} = 0 \text{mV} \]
DYNAMIC LARGE-SIGNAL STABILIZATION

\[ V_{\text{DEADZONE}} = 0 \text{mV} \]
DYNAMIC LARGE-SIGNAL STABILIZATION

$V_{DEADZONE} = 0\text{mV}$

Volts

time (ns)
DYNAMIC LARGE-SIGNAL STABILIZATION

$V_{\text{DEADZONE}} = 200\text{mV}$

![Waveform diagram showing oscillations with $V_{\text{DEADZONE}} = 200\text{mV}$]
DYNAMIC LARGE-SIGNAL STABILIZATION

$V_{\text{DEADZONE}} = 250\text{mV}$

- The graph shows the stabilization process over time.
- The $x$-axis represents time in nanoseconds (ns), ranging from 0 to 6 ns.
- The $y$-axis represents voltage (Volts), ranging from 0 to 1.2 Volts.
- The graph includes multiple curves indicating the stabilization behavior with a dead zone of $250\text{mV}$.
DYNAMIC LARGE-SIGNAL STABILIZATION

\[ V_{\text{DEADZONE}} = 300\text{mV} \]
V_{DEADZONE} = 350mV
DYNAMIC LARGE-SIGNAL STABILIZATION

$V_{\text{DEADZONE}} = 400\text{mV}$
DYNAMIC LARGE-SIGNAL STABILIZATION

THREE OPERATION PHASES

- Slewing
DYNAMIC LARGE-SIGNAL STABILIZATION

THREE OPERATION PHASES

- **Slewing**

![Circuit Diagram]

**Rail-to-rail inverters**

Max $V_{OV}$

Max $V_{OV}$

Very small transistors

Slewing Efficiency: Theoretical Maximum!

**Graph:**

- Time (ns)
- Voltage (Volts)

$V_{IN}$ - $V_{DZ1}$ + $V_{OUT}$

$C_2$, $C_3$, $C_L$

$M_{CP}$, $M_{CN}$

$RST$, $RST$, $RST$
DYNAMIC LARGE-SIGNAL STABILIZATION
THREE OPERATION PHASES

- **Slewing**

Acts like bi-directional switchable current source
DYNAMIC LARGE-SIGNAL STABILIZATION

THREE OPERATION PHASES

- Slewing
- Stabilization
DYNAMIC LARGE-SIGNAL STABILIZATION

STABILIZATION

\[ \begin{align*}
V_{\text{IN}} & \quad \rightarrow \quad V_A \\
V_{\text{IN}} & \quad \rightarrow \quad V_{\text{AP}} \\
V_{\text{IN}} & \quad \rightarrow \quad V_{\text{AN}} \\
V_{\text{IN}} & \quad \rightarrow \quad V_{\text{OUT}} \\
\end{align*} \]
DYNAMIC LARGE-SIGNAL STABILIZATION STABILIZATION

1. Reduced avg. overdrive voltage
2. Reduced output current
3. Reduced oscillation amplitude

Example here: operation on the edge of stability
DYNAMIC LARGE-SIGNAL STABILIZATION

STABILIZATION (IN NANOSCALE)

- Modern example in 16nm FinFET CMOS
  - Less intrinsic gain
  - Different dynamic biasing mechanism (resistor)
  - Class-AB biasing (outputs in weak-inversion at steady-state)

- But fundamental idea & behavior still the same
DYNAMIC LARGE-SIGNAL STABILIZATION

STABILIZATION (IN NANOSCALE)

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- But fundamental idea & behavior still the same

- $V_{OUT}$ affects stability!
  - $V_{DS}$ varies w.r.t. $V_{OUT}$
  - Thus, output pole location varies w.r.t. $V_{OUT}$
DYNAMIC LARGE-SIGNAL STABILIZATION

THREE OPERATION PHASES

- Slewing
- Stabilization
- Settling
DYNAMIC LARGE-SIGNAL STABILIZATION

SETTLING

- Weak-inversion steady-state

- Min $V_{OV}$
  - 😊 Low quiescent current
  - 😊 Noise filtering

- Min $V_{DSAT}$
  - 😊 Wide swing
  - 😊 High linearity

- Max $r_o$
  - 😊 High gain
  - 😊 High linearity
DYNAMIC LARGE-SIGNAL STABILIZATION

NOISE

- Noise at output filtered by steady-state $g_m$
  - Internal noise
  - Supply noise

- With smart design, noise at least as good as opamp
  - But much faster
  - But much more efficient
DYNAMIC LARGE-SIGNAL STABILIZATION

NOISE

- SNR and THD may have different bias optimums

- Noise
  - Best when over-damped
  - Lowest $g_m$ for most filtering

- Linearity
  - Best when critically-damped
  - Fastest settling
THE “IDEAL AMPLIFIER” WISHLIST

- High bandwidth
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- Performance scales like digital CMOS
- Class-AB
- Fully dynamic (switchable)
- High linearity
- High gain
- Low noise
- Rail-to-rail output swing
- Small area
- Low design effort

So ... how did we do?

Ring Amplifier (ringamp)
TOPOLOGY SELECTION
TOPOLOGY SELECTION

- Dead-zone embedding
- Signaling mode
- Number of stages
- CMFB
- Power Cycling
- Device
- Pseudo-differential
- Fully-differential
- Biasing Mode
- Location
- Device
- Auto-zero
- Other
- High-voltage
TOPOLOGY SELECTION

Basic Topology Selection

Dead-zone embedding

Location

Device

Pseudo-differential

Fully-differential

Signaling mode

Number of stages

CMFB

Power Cycling

Auto-zero

High-voltage

Other

Biasing Mode

Class B

Class AB

Class B+AB
BIASING MODE

TOPOLOGY SELECTION

- Class-B
  - Sub-threshold “dead-zone”
  - Surrounded by “weak-zone”

😊 Fastest, most stable
😊 Dead-zone distortion

DC Input Sweep

- DC Input Sweep
- Dead-zone distortion
- Weak-zones
BIASING MODE

TOPOLOGY SELECTION

- Class-AB
  - Only “weak zone”
  - Always conducting

😊 Highest accuracy
😢 Slower
BIASING MODE

TOPOLOGY SELECTION

- Class-B + AB
  - Class-B coarse charge
  - Class-AB fine settle

[Hershberg, VLSI 2013]
TOPOLOGY SELECTION

Basic Topology Selection

- Dead-zone embedding
- Signaling mode
- Number of stages
- CMFB
- Power Cycling
- Other

Location

- Directly before output stage
- Earlier stages

Device

- Pseudo-differential
- Fully-differential

Biasing Mode

- Auto-zero
- High-voltage
EMBEDDING LOCATION

TOPOLOGY SELECTION

- Directly before output stage
  - Precise control of output stage biasing

- Best for:
  - Class-AB operation
  - High accuracy & linearity
  - Low gain technologies
  - Nanoscale CMOS 👍

[Hershberg, VLSI 2013]

[Lim, JSSC Oct. 2015]
EMBEDDING LOCATION

TOPOLOGY SELECTION

- Before second-to-last stage
  - Decouples stability from large signal biasing of output stage

- Best for:
  - Class-B operation
  - High speed
  - Coarse charging

[Hershberg, JSSC 2012]
TOPOLOGY CHOICES

Basic Topology Selection

- Dead-zone embedding
  - Biasing Mode
  - Location
  - Device
    - Capacitor
    - Resistor
    - CMOS Resistor
  - Pseudo-differential
  - Fully-differential
- Signaling mode
- Number of stages
- CMFB
- Power Cycling
- Auto-zero
- High-voltage
- Other
CAPACITOR EMBEDDING
TOPOLOGY SELECTION

- Direct voltage-mode control
- Best for
  - Class-B biasing
  - High-voltage applications
- Limitations
  - If embedding in last stage, will reduce max slewing efficiency

[Hershberg, JSSC 2012]

[Hershberg, VLSI 2013]
RESISTOR EMBEDDING

TOPOLOGY SELECTION

- Dynamically creates offset during stabilization

- Best for
  - PVT robust design
  - Nanoscale CMOS
  - Slewing efficiency

- Limitations
  - Speed problems if large $V_{DZ}$ offset needs to be embedded

[Lim, JSSC Oct. 2015]
RESISTOR EMBEDDING

TOPOLOGY SELECTION

- Dynamically creates offset during stabilization
- Best for
  - PVT robust design
  - Nanoscale CMOS
  - Slewing efficiency
- Limitations
  - Speed problems if large $V_{DZ}$ offset needs to be embedded

[Equation]

$$I_{OUT} = V_{DD} - I_D - V_{DZ} - V_{OV}$$

[Line Diagram]

[Reference]

Lim, JSSC Oct. 2015
RESISTOR EMBEDDING

TOPOLOGY SELECTION

- Dynamically creates offset during stabilization
- Best for
  - PVT robust design
  - Nanoscale CMOS
  - Slewing efficiency
- Limitations
  - Speed problems if large $V_{DZ}$ offset needs to be embedded

\[ \Delta V_{DZ} = I_D \times R_B \]

Want a big $V$? Needs a big $R$ Creates slow stage 2 poles

$\omega_p = \frac{1}{RC}$

[Lim, JSSC Oct. 2015]
CMOS RESISTOR EMBEDDING

TOPOLOGY SELECTION

- Tunable on-state resistance
- Switchable (off-state)

- Best for
  - Power-cycling
  - Optimal biasing
  - Nanoscale CMOS

- Limitations
  - Less PVT robust than static resistor

[Diagram of CMOS topology with input (INp), output (OUTm), and enable (EN) signals.]

[Lagos, JSSC Feb. 2019]
OTHER EMBEDDINGS

TOPOLOGY SELECTION

- Current starved inverters

- Best for
  - Dynamic control
  - Analog PVT tracking schemes

- Limitations
  - Slower (lowers 2\textsuperscript{nd} stage output poles)

[Hershberg, PhD Thesis 2012]
[Leuenberger, CICC 2017]
OTHER EMBEDDINGS

TOPOLOGY SELECTION

- Threshold voltage of output stage

- Best for
  - Low supply voltages
  - High speed
  - Simplicity
  - Area

- Limitations
  - PVT variation
  - Not with high supply voltages

[Lim, JSSC Oct. 2015]
TOPOLOGY SELECTION

Basic Topology Selection

- Dead-zone embedding
- Signaling mode
- Number of stages
- CMFB
- Power Cycling
- Other

- Biasing Mode
- Location
- Device
- Pseudo-differential
- Fully-differential
- Auto-zero
- High-voltage
PSEUDO DIFFERENTIAL

TOPOLOGY SELECTION

- Can be purely inverter-based, most dynamic

- Best for
  - Speed

- Limitations
  - Large input offset must be canceled
  - Limited accuracy

![Pseudo Differential Topology Diagram]
FULLY DIFFERENTIAL

TOPOLOGY SELECTION

- Fully-differential
- Best for
  - General purpose
  - Highest accuracy
- Limitations
  - Moderate speed/power penalty
    (front stage becomes slower)
TOPOLOGY SELECTION

Basic Topology Selection

- Dead-zone embedding
- Signaling mode
- Number of stages
- CMFB
- Power Cycling
- Other

Biasing Mode
Location
Device
Pseudo-differential
Fully-differential
Auto-zero
High-voltage
THREE-STAGE TOPOLOGY SELECTION

- The “workhorse”
- Best for
  - Most applications
- Limitations
  - Might not give enough gain in some technologies to support calibration-free operation
  - CMFB can be a little tricky in fully-differential topologies

[Hershberg, ISSCC 2019]
FOUR-STAGE TOPOLOGY SELECTION

- When more gain is needed

- Best for
  - High precision
  - Calibration-free

- Limitations
  - CMFB and latch-up require careful consideration
  - A little less speed (extra internal pole)

[Lim, VLSI 2017]
TWO-STAGE TOPOLOGY SELECTION

- Special purpose

- Best for
  - Non-inverting feedback loop (e.g. CMFB)
  - Low precision applications

- Limitations
  - Low gain

[Lagos, JSSC Feb. 2019]
ONE STAGE?

TOPOLOGY SELECTION

- “Inverter based amplifier”

- Best for
  - Specialty applications

- Limitations
  - Low gain
  - Low gain-bandwidth
  - Low slew rate / slew efficiency
  - No gain before output stage (no large-signal effects)

- A multi-stage ringamp is generally faster and more efficient.
TOPOLOGY SELECTION

CMFB

- Approach varies depending on topology
  - Pseudo-differential
  - Fully-differential
  - Level of CM rejection needed
## TOPOLOGY SELECTION

### CMFB

- Approach varies depending on topology
  - Pseudo-differential
  - Fully-differential
  - Level of CM rejection needed

- Passive CMFB
  - Simple
  - Often good enough

[Hershberg, JSSC 2012]
TOPOLOGY SELECTION

CMFB

- Approach varies depending on topology
  - Pseudo-differential
  - Fully-differential
  - Level of CM rejection needed

- Passive CMFB
  - Simple
  - Often good enough

- Active CMFB
  - Add gain
  - Higher accuracy
  - Larger rejection range

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[Image of circuit diagram with INm, OUTp, INp, OUTm, VCM, and 2-stage ringamp] [Lagos, JSSC Feb. 2019]
TOPOLOGY SELECTION

CMFB

- Fully differential
  - Often requires global and local loops
- 3 paths
  - DC bias
  - Fast global feedback
  - Fast local feedback

[Hershberg, ISSCC 2019]
TOPOLOGY SELECTION

CMFB

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  - Often requires global and local loops

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  - DC bias
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[Hershberg, ISSCC 2019]
TOPOLOGY SELECTION

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  - DC bias
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[Hershberg, ISSCC 2019]
TOPOLOGY SELECTION

POWER CYCLING

- Only operate when needed
  - Save power

- Best solution very architecture dependent
TOPOLOGY SELECTION

POWER CYCLING

- Only operate when needed
  - Save power

- Best solution is very architecture dependent

- A naive solution: power gate + output switch
  - Extra switch in feedback path 😞
  - Undefined internal reset state 😞
  - Signal dependent charge kickback 😞
  - Clock must drive all switches on EN line 😞
  - Headroom reduced by power gating switches 😞
TOPOLOGY SELECTION

POWER CYCLING

- Only operate when needed
  - Save power

- Best solution is very architecture dependent

- **A better solution**: full-reset, self-disconnect
  - Extra parasitics from pullup/pulldown switches 😞
  - Clock must drive all switches on EN line 🙁
  - Headroom reduced by power gating switches 😞
TOPOLOGY SELECTION

POWER CYCLING

- Only operate when needed
  - Save power

- Best solution is very architecture dependent

- A better solution: full-reset, self-disconnect
  - Extra parasitics from pullup/pulldown switches 😞
  - Clock must drive all switches on EN line 😞
  - Headroom reduced by power gating switches 😞
TOPOLOGY SELECTION

POWER CYCLING

▪ **A very elegant solution:** self-resetting

▪ Requires
  ▪ Bias-enhancement (we’ll get to this later)
  ▪ CMOS resistors

▪ Best of all worlds
  ▪ No power-gating switches
  ▪ No pull-up or pull-down switches
  ▪ Small switches (CMOS resistors) minimize clock loading

[Lagos, JSSC Mar. 2019]
TOPOLOGY SELECTION

POWER CYCLING

- A very elegant solution: self-resetting

- Requires
  - Bias-enhancement (we’ll get to this later)
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  - Small switches (CMOS resistors) minimize clock loading

[Lagos, JSSC Mar. 2019]


TOPOLOGY SELECTION

AUTO-ZERO

▪ Not for free
  ▪ Extra complexity
  ▪ Sometimes extra power

▪ Some applications / topologies require it
  ▪ Pseudo-differential ringamps
  ▪ Zero-offset applications

▪ Most applications / topologies can avoid it
  ▪ Offset tolerant and “good enough” use cases
  ▪ System level methods
TOPOLOGY SELECTION
AUTO-ZERO

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  - System level methods

“Good enough” partial cancellation:
1. Inverter trip-point offset
   (tech. dependent $V_{TH}$ mismatch)
2. Stage 1 random offset
   (largest source of random offset)
TOPOLOGY SELECTION

AUTO-ZERO

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  - Sometimes extra power

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\[ \beta = 1 \]
\[ C_{LOAD} = C_L + C_{AZ} \]

Be careful with \( C_{AZ} \) sizing:
- Stability
- Noise

[Lim, Oct. 2015]
TOPOLOGY SELECTION

AUTO-ZERO

- Not for free
  - Extra complexity
  - Sometimes extra power

- Some applications / topologies require it
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\[ \beta = \frac{C_S}{C_{FB}} \]

\[ C_{LOAD} = C_L + C_{FB//C_S} \]

[Lim, Oct. 2015]
## AUTO-ZERO

- **Not for free**
  - Extra complexity
  - Sometimes extra power

- **Some applications / topologies require it**
  - Pseudo-differential ringamps
  - Zero-offset applications

- **Most applications / topologies can avoid it**
  - Offset tolerant and “good enough” use cases
  - System level methods

**Differential topologies:**
- No inverter trip-point offset 😊
- Only random mismatch offset
**TOPOLOGY SELECTION**

**AUTO-ZERO**

- Not for free
  - Extra complexity
  - Sometimes extra power

- Some applications / topologies require it
  - Pseudo-differential ringamps
  - Zero-offset applications

- Most applications / topologies can avoid it
  - Offset tolerant and “good enough” use cases
  - System level methods

*Example: Pipelined SAR stage*

Can often find simple methods to cancel ringamp offset somewhere else in the system
TOPOLOGY SELECTION

Basic Topology Selection

- Dead-zone embedding
- Signaling mode
- Number of stages
- CMFB
- Power Cycling
- Other
- Biasing Mode
- Location
- Device
- Pseudo-differential
- Fully-differential
- Auto-zero
- High-voltage
TOPOLOGY SELECTION

HIGH-VOLTAGE

- Capacitor embedding is best
  - Can store large $\Delta V$ needed to generate dead-zone
  - Can level shift between different VDDs
  - Can couple in multiple output paths (coarse/fine)

[ElShater, JSSC 2019]
PATHWAYS TO PERFORMANCE
PATHWAYS TO PERFORMANCE

My Ringamp Needs...

More Settled Linearity
- Biasing Mode
- Circuit Techniques
- Increase Gain

More Speed
- Minimize Internal Parasitics
- Circuit Techniques

Less Noise
- Increase Internal Power
- Reduce output pole frequency
PATHWAYS TO PERFORMANCE

My Ringamp Needs...

More Settled Linearity
- Biasing Mode
  - class-AB biasing (weak-zone only)
- Circuit Techniques
- Increase Gain

More Speed
- Minimize Internal Parasitics
- Circuit Techniques

Less Noise
- Increase Internal Power
- Reduce output pole frequency
PATHWAYS TO PERFORMANCE

My Ringamp Needs...

More Settled Linearity
- Circuit Techniques
  - Biased Mode
  - Increase Gain
  - Dead-zone Degeneration
  - External Gain Enhancement Techniques

More Speed
- Minimize Internal Parasitics
- External Gain Techniques

Less Noise
- Increase Internal Power
- Reduce output pole frequency

Increase
- Circuit Techniques
- Minimize Internal Parasitics
- Increase Internal Power
DEAD-ZONE DEGENERATION
LINEARITY ENHANCEMENT

■ Motivation
  ▪ 1st order linear gain error often easy to calibrate (with digital or trimming)
  ▪ Higher order gain error much harder to correct

■ Idea
  ▪ Feedback to “warp” $V_{DZ}$ as function of $V_{OUT}$
  ▪ Especially useful in low-gain tech. like 28nm

[Lagos, JSSC Mar. 2019]
PATHWAYS TO PERFORMANCE

My Ringamp Needs...

More Settled Linearity
- Biasing Mode
- Dead-zone Degeneration
- Circuit Techniques
- Increase Gain
- External Gain Enhancement Techniques

More Speed
- Minimize Internal Parasitics
- Increase Internal Power
- Circuit Techniques

Less Noise
- Reduce output pole frequency
EXTERNAL GAIN ENHANCEMENT TECHNIQUES

LINEARITY ENHANCEMENT

- Class-AB style ringamps compatible with many “classical” gain enhancement techniques

- Ringamps using Correlated Level Shifting (CLS) techniques:
  - Split-CLS [Hershberg, JSSC 2012]
  - A-CLS [T.C. Hung, JSSC 2019]
  - WA-CLS [T.C. Hung, JSSC 2020]
PATHWAYS TO PERFORMANCE

My Ringamp Needs...

More Settled Linearity
- Increase Gain
  - Cascade More Stages
  - Boost per-Stage Gain

More Speed
- Minimize Internal Parasitics

Less Noise
- Increase Internal Power
- Reduce output pole frequency

Biasing Mode
Circuit Techniques
Circuit Techniques
PATHWAYS TO PERFORMANCE

My Ringamp Needs...

- More Settled Linearity
  - Biasing Mode
  - Circuit Techniques
  - Increase Gain

- More Speed
  - Minimize Internal Parasitics

- Less Noise
  - Circuit Techniques
  - Increase Internal Power
  - Reduce output pole frequency
THE 2 COMMANDMENTS
OF HIGH SPEED RINGAMP DESIGN

1. Thou shalt never load the internal nodes

2. Thou shalt never limit the internal currents
THE 2 COMMANDMENTS
OF HIGH SPEED RINGAMP DESIGN

- But many choose to break the rules...
  - Trade speed for other benefits

Current limiter for peak $g_m/I_D$

[Lim, JSSC Oct. 2015]
PATHWAYS TO PERFORMANCE

My Ringamp Needs...

More Settled Linearity

More Speed

Circuit Techniques

Minimize Internal Parasitics

Bias Enhancement

Biasing Mode

Circuit Techniques

Increase Gain

Increase Internal Power

Reduce output pole frequency

Less Noise
BIAS-ENHANCEMENT

SPEED ENHANCEMENT

- **Idea:** use additional signal splitting to boost $V_{OV}$ and $g_m$ of internal stage

[Chen, TCASII 2017]
[Chen, TCASII 2017]
[Chen, TCASII 2017]
[Chen, TCASII 2017]

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[Chen, TCASII 2017]
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Increased bandwidth

Clock Frequency (MHz)

THD

Baseline ringamp
Baseline + dead-zone degeneration
Baseline + 2nd-stage bias enhancement
Proposed ringamp

$V_{OV}$ boosted

INp
OUTm
PATHWAYS TO PERFORMANCE

My Ringamp Needs...

- More Settled Linearity
  - Biasing Mode
  - Circuit Techniques
  - Increase Gain
- More Speed
  - Minimize Internal Parasitics
  - Circuit Techniques
- Less Noise
  - Increase Internal Power
  - Reduce output pole frequency
  - Increase internal pole frequencies
PATHWAYS TO PERFORMANCE

My Ringamp Needs...

- More Settled Linearity
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  - Circuit Techniques
  - Increase Gain

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  - Circuit Techniques

- Less Noise
  - Increase Internal Power
  - Reduce output pole frequency
  - Reduce noise of stage 1
PATHWAYS TO PERFORMANCE

My Ringamp Needs...

- More Settled Linearity
  - Biasing Mode
  - Circuit Techniques
  - Increase Gain

- More Speed
  - Minimize Internal Parasitics
  - Circuit Techniques
  - Increase Internal Power

- Less Noise
  - Reduce output pole frequency
  - Filter internal noise with lower output $g_m$
PVT CONSIDERATIONS
FEEDBACK MAKES LIFE EASIER

PVT CONSIDERATIONS

- **Open-loop amplifier** (e.g. Gm-C integrator)
  - *Like balancing a ball on a hill*
  - No feedback to suppress parameter variation
    - *E.g. open-loop residue gain*

- **Ring amplifier**
  - *Like placing a ball safely away from the edge*
  - Feedback suppresses parameter variation
  - But only as good as the feedback itself
    - Loop gain, bandwidth, stability
APPROACH 1: ROBUST-BY-DESIGN

PVT CONSIDERATIONS

- Calibration-free approach
  - Include extra margin to pass all corners
  - Sacrifice some efficiency / speed

- Options for increasing phase margin
  - Move internal poles higher
    - More power
  - Move external pole lower
    - Less speed
APPROACH 1: ROBUST-BY-DESIGN

PVT CONSIDERATIONS

- Calibration-free approach
  - Include extra margin to pass all corners
  - Sacrifice some efficiency / speed

- Calibration-free ringamp ADCs
  - [Hung, ISSCC 2020]
    - 100MS/s, 71.7dB SNDR, 2.2fJ/c-step FoM_{W}
  - [Lim, JSSC Dec. 2015]
    - 50MS/s, 70.9dB SNDR, 6.9fJ/c-step FoM_{W}
  - [Lim, VLSI 2017]
    - 100MS/s, 73.2dB SNDR, 6.1fJ/c-step FoM_{W}

![Power supply +/- 50mV](image)

![Temperature -20°C – 80°C](image)

[Lim, Dec. JSSC 2015]
APPROACH 2: CALIBRATION

PVT CONSIDERATIONS

- Calibration-based approach
  - Use feedback to maintain optimal biasing
  - Top performance
  - More analog design freedom
  - More digital complexity 😊

- Calibration-based ringamp ADCs
  - [Hershberg 2019]
    • 3.2GS/s, 61.7dB SNDR, 19.3fJ/c-step FoM \_w
  - More to come...
PRACTICAL DESIGN
TRANSIENT-BASED DESIGN & VALIDATION
PRACTICAL DESIGN

▪ Transient-centric design is becoming mainstream
  ▪ All “next-gen” amplifiers: ringamp, Gm-C, Gm-R, Charge-steering, Zero-crossing, etc.

▪ Modern compute power can handle it
  ▪ Multi-core with APS
METHODS OF ANALYSIS

PRACTICAL DESIGN

- Transient waveform visual inspection
  - Amplifier input nodes particularly useful

- Transient (+noise) FFT of sampled output
  - Exercise full output swing, need enough FFT points

- AC, PAC, PSS, PNOISE where useful
  - But always confirm with transient!
METHODS OF ANALYSIS
PRACTICAL DESIGN

- Transient waveform visual inspection
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  - But always confirm with transient!
DESIGN PROCEDURE

16NM DESIGN EXAMPLE

- Build in-situ testbench
  - Real switches
  - Actual feedback factor
  - Real output loading
  - Real timing control scheme
  - Estimated parasitics
  - Any other non-idealities

example environment:
1.5b flip-around MDAC
16NM DESIGN EXAMPLE

- Fully-differential
- CMOS-resistor
- Bias-enhanced
- Self-resetting
- Multi-path CMFB
DESIGN PROCEDURE

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DESIGN PROCEDURE
16NM DESIGN EXAMPLE

Baseline (final design)
Key parameter: output drive strength

- Smaller: more stable, less internal loading
- Larger: faster slew

3 different amplitudes:
ADJUST DRIVE STRENGTH

16NM DESIGN EXAMPLE

- Key parameter: output drive strength
  - Smaller: more stable, less internal loading
  - Larger: faster slew

3 different amplitudes:
ADJUST DRIVE STRENGTH
16NM DESIGN EXAMPLE

- Key parameter: internal stage sizes
  - Smaller: more efficient
  - Larger: faster
ADJUST DEADZONE
16NM DESIGN EXAMPLE

- Key parameter: dead-zone biasing
  - Smaller: faster settling
  - Larger: more stable

Optimal dead-zone

3 different amplitudes:
**ADJUST DEADZONE**

**16NM DESIGN EXAMPLE**

- Key parameter: dead-zone biasing
  - Smaller: faster settling
  - Larger: more stable

---

![Graph showing different amplitudes](image-url)

3 different amplitudes:

- [Graph 1](image-url)
- [Graph 2](image-url)

---

*Dead-zone too large*
ADJUST DEADZONE

16NM DESIGN EXAMPLE

- Key parameter: dead-zone biasing
  - Smaller: faster settling
  - Larger: more stable

Dead-zone too small

3 different amplitudes:
EXAMPLE DESIGN PROCEDURE
PRACTICAL DESIGN

1. Build in-situ testbench with realistic timing & feedback conditions

2. Initialize ringamp with over-designed front stages (extra bandwidth)

3. Size output stage to balance worst-case slew rate / settling time (approx. 50/50)

4. Down-scale front stages for power efficiency (e.g. 4:2:1)

5. Iterate from #3 as necessary

Ultimately, the best design procedure depends on many factors, e.g. optimization priorities and application type. With practice will come intuition and insight. This is the art of analog design!
REVITALIZING THE ECOSYSTEM
REVITALIZING THE ECOSYSTEM

CONCLUSIONS

Ringamps remove the amplifier bottleneck...

more architectural freedom

amplifier-intensive techniques

new applications

...and diversity is increasing
REVITALIZING THE ECOSYSTEM

CASE STUDY

[Hershberg, ISSCC 2019 (1)]

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>System</td>
<td>3.2 GS/s</td>
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<tr>
<td>Channel</td>
<td>800 MS/s</td>
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<tr>
<td>SNDR</td>
<td>63 dB</td>
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<tr>
<td>SFDR</td>
<td>80 dB</td>
</tr>
<tr>
<td>Power</td>
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<tr>
<td>FoM&lt;sub&gt;W&lt;/sub&gt;</td>
<td>19 fJ/cs</td>
</tr>
</tbody>
</table>

- Order-of-magnitude improvement in direct-RF sampling ADC SoTA
- 36 ringamps in system
  - Very amplifier intensive

![Diagram](image-url)
REVITALIZING THE ECOSYSTEM
RINGAMP DESIGNS WITH MEASURED SILICON
REVITALIZING THE ECOSYSTEM
RINGAMP TOPOLOGY DIVERSIFICATION

Bias-Enhanced
[Chen, TCASII 2017]

Self-Biased
[Lim, JSSC Oct. 2015]

Self-Resetting
[Lagos, JSSC Mar. 2019]

Closed Loop Dynamic Amplifier
[Tang, ISSCC 2020]

High Voltage
[ElShater, ISSCC 2019]

Power Management
[Park, ISSCC 2020]

Rapid Reset
[T.C.Hung, ISSCC 2020]

Class B+AB
[Hershberg, VLSI 2013]
But is it the scalable amplifier you’ve been waiting for?

Depends!

Ringamps are an exciting new tool.

It could be the right one for your task.
Decide for yourself! 😊
THANK YOU FOR YOUR ATTENTION!