High Performance ADCs for 5G

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5G NR FR2:
ADC REQUIREMENTS

5G NR FR2: 3GPP specs

- 5G Bandwidth Specs
  - Channel: 50MHz, 100MHz, 200MHz, 400MHz
  - Max. Aggregation: 800MHz
  - Widest Band: 3.25GHz (24.25GHz – 27.50GHz)
  - Agg. 28GHz Bands: 5.25GHz (24.25GHz – 29.50GHz)

- ...and need >1.5x more bandwidth to relax anti-alias filter.

- 5G Modulation Specs
  - QPSK, 16 QAM, 64 QAM, 256 QAM
  - Future: 1024 QAM

[3GPP, 2019]

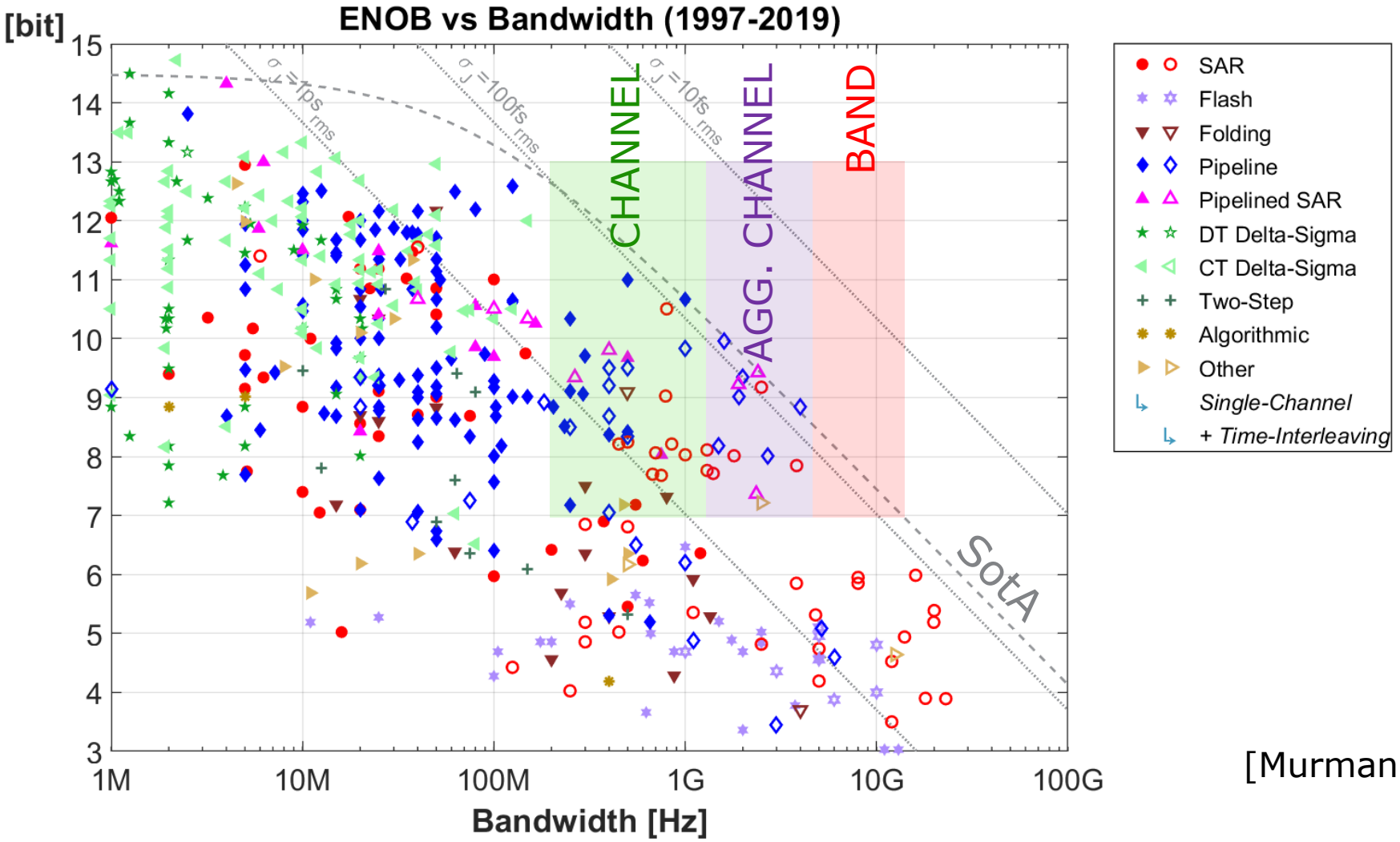
5G NR FR2: ADC specs

- Translation into ADC specs depends heavily on system-level choices
  - Receiver chain SNR budget
  - % of standard supported

- Let's see what we can do across the large range of likely 5G ADC specs:
  - Resolution: 7 – 13 bits
  - Speed: 400 MS/s – 12 GS/s
  - Linearity: 65 dB – 85 dB SFDR

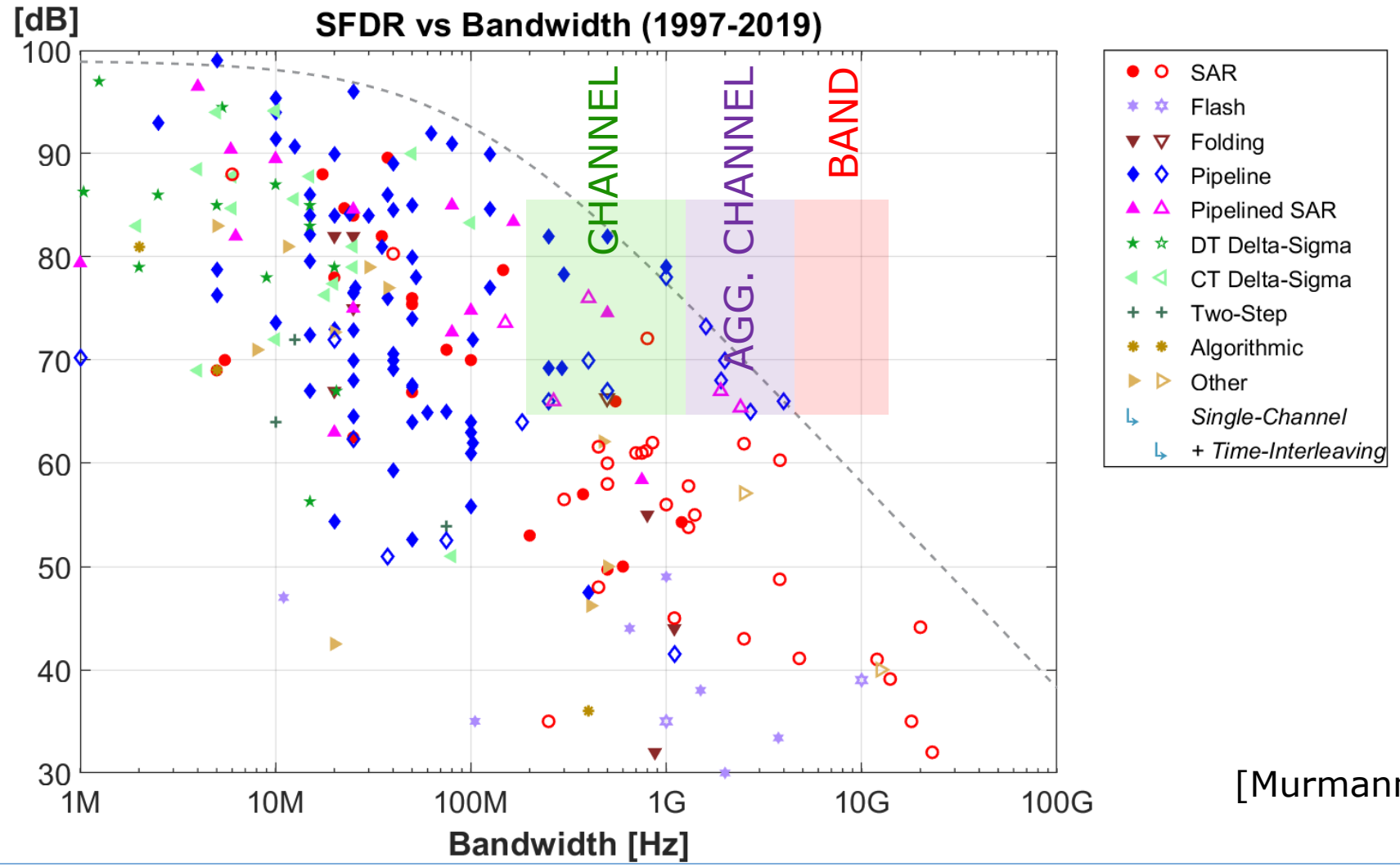
  (needs to cover Mobile-Terminal, Base-Station, etc...)

5G NR FR2: ADC SoTA



[Murmann, 2019]

Linearity SoTA



[Murmann, 2019]

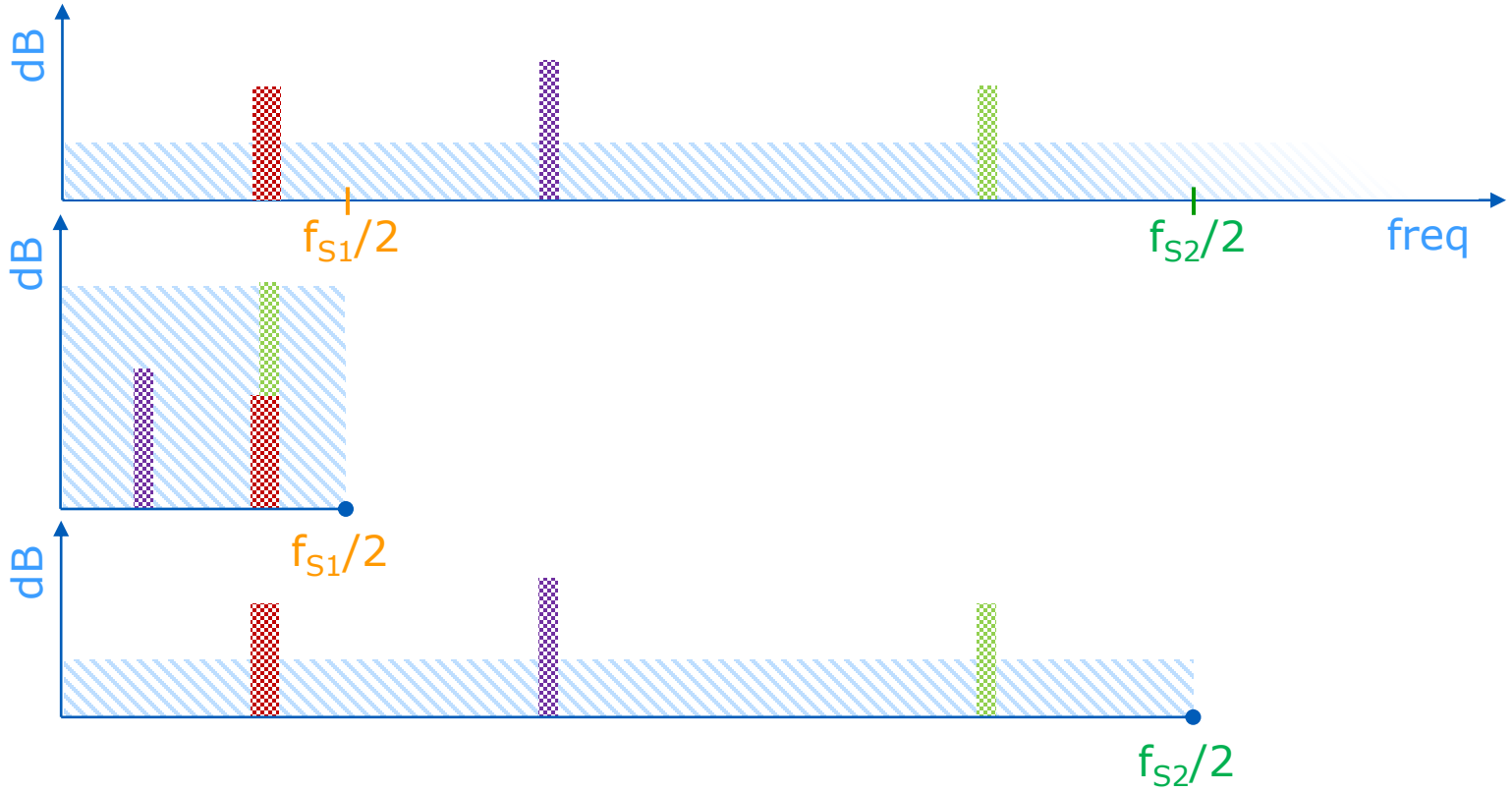
Linearity considerations

- SFDR/THD specs can be harder than SNR specs!
  - Noise power gets spread across large bandwidth
  - Distortion power remains concentrated at specific frequencies

Continuous-time input spectrum:

Low speed ADC after sampling:

High speed ADC after sampling:



More considerations

- Beamforming requires many ADCs
  - Power efficiency
  - Area efficiency

An industrial solution today:

500mW 4GS/s ADC in 0.5mm²
x 128 element digital beam-forming
= 64 Watts
= 64 mm² ☹

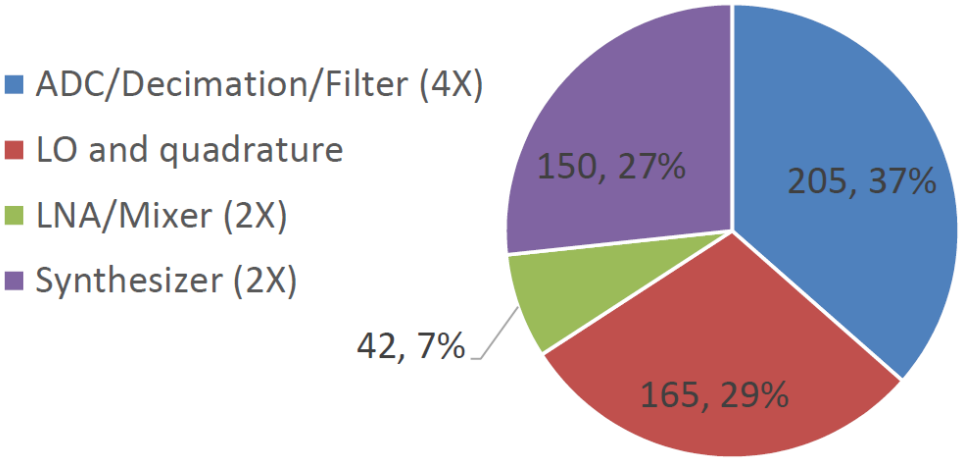
- Reconfigurability
  - Large variation in required performance depending on mode (e.g. 50MHz vs. 800MHz BW)

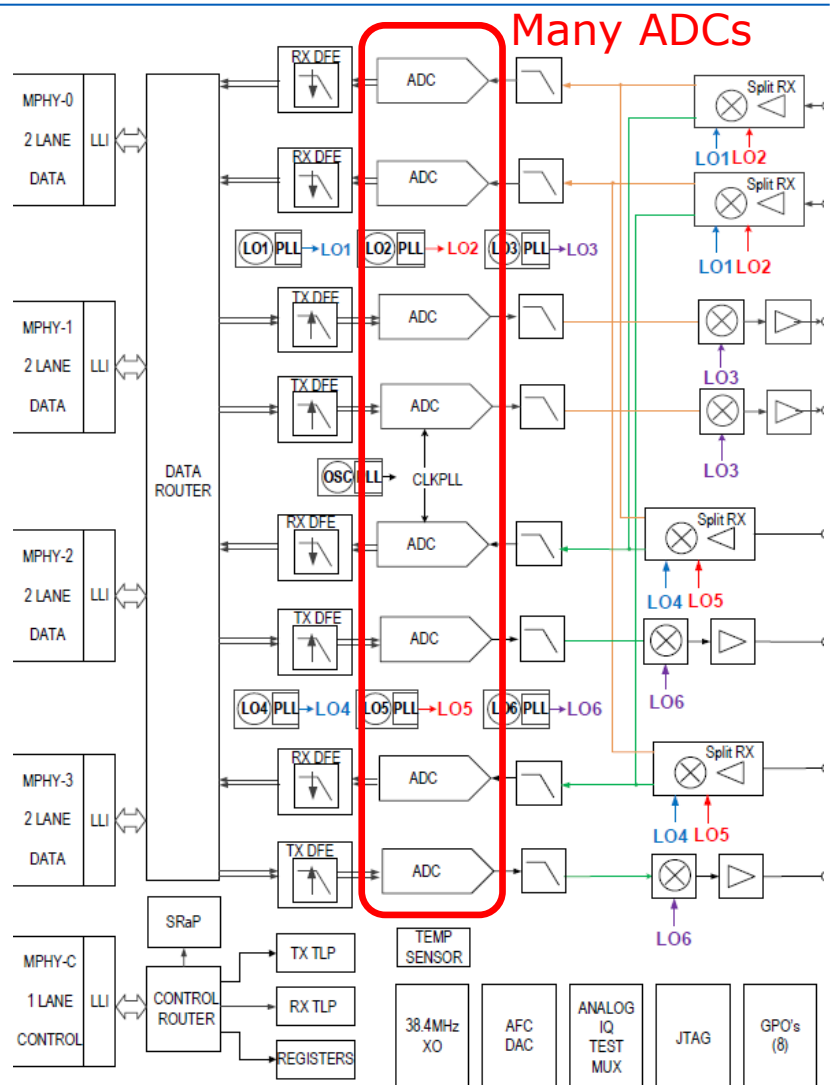
Industry SoTA

	Vaz ISSCC 2017	Devarajan ISSCC 2017	Straayer ISSCC 2016	Wu ISSCC 2016	Ali VLSI 2016
Architecture	Pipe-SAR	Pipeline	Pipeline	Pipeline	Pipeline
Sampling rate [Gsps]	4	10	4	4	5
Technology [nm]	16	28	65	16	28
ENOB Nyquist [bit]	9.2	8.8	8.9	9.0	9.3
SFDR Nyquist [dB]	67.0	64	64.0	68.0	70
Power [mW]	513	2900	2214	300	2300
FoM_{Walden} [fJ/c.step]	214	631	1130	145	709
$FoM_{Schreier}$ [dB]	153	147	145	154	148
Area [mm²]	1.04	20.2	11.0	0.34	14.4

Case Study: MIMO Transceiver

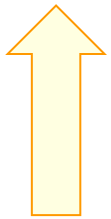
- [Jann ISSCC 2019]
  - First fully-integrated 5G TRX
- Modest ADC specs
  - 400 MS/s
  - 7.7 ENOB
  - ...but ADC is *still* biggest slice of RX power!





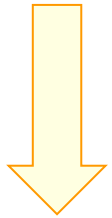
Conclusions: 5G NR FR2 requirements

- High speed (400MS/s - 12GS/s)
- Medium resolution (7 - 13b)
- High linearity (65dB - 85dB)



Industry SoTA can meet these specs... ☺

- Low power
- Low area



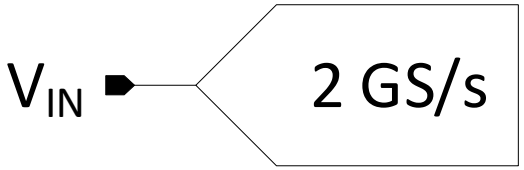
...but not necessarily with acceptable power / area. ☹

GETTING TO GIGA-SAMPLE SPEEDS

Giga-samples: how do we get there?

- Two possible strategies:

1. Fast single-channel
   - 😐 Practical technology speed limits
   - ☹ Many clocking overheads don't scale w/ clock
   - ☹ Limited architecture choices

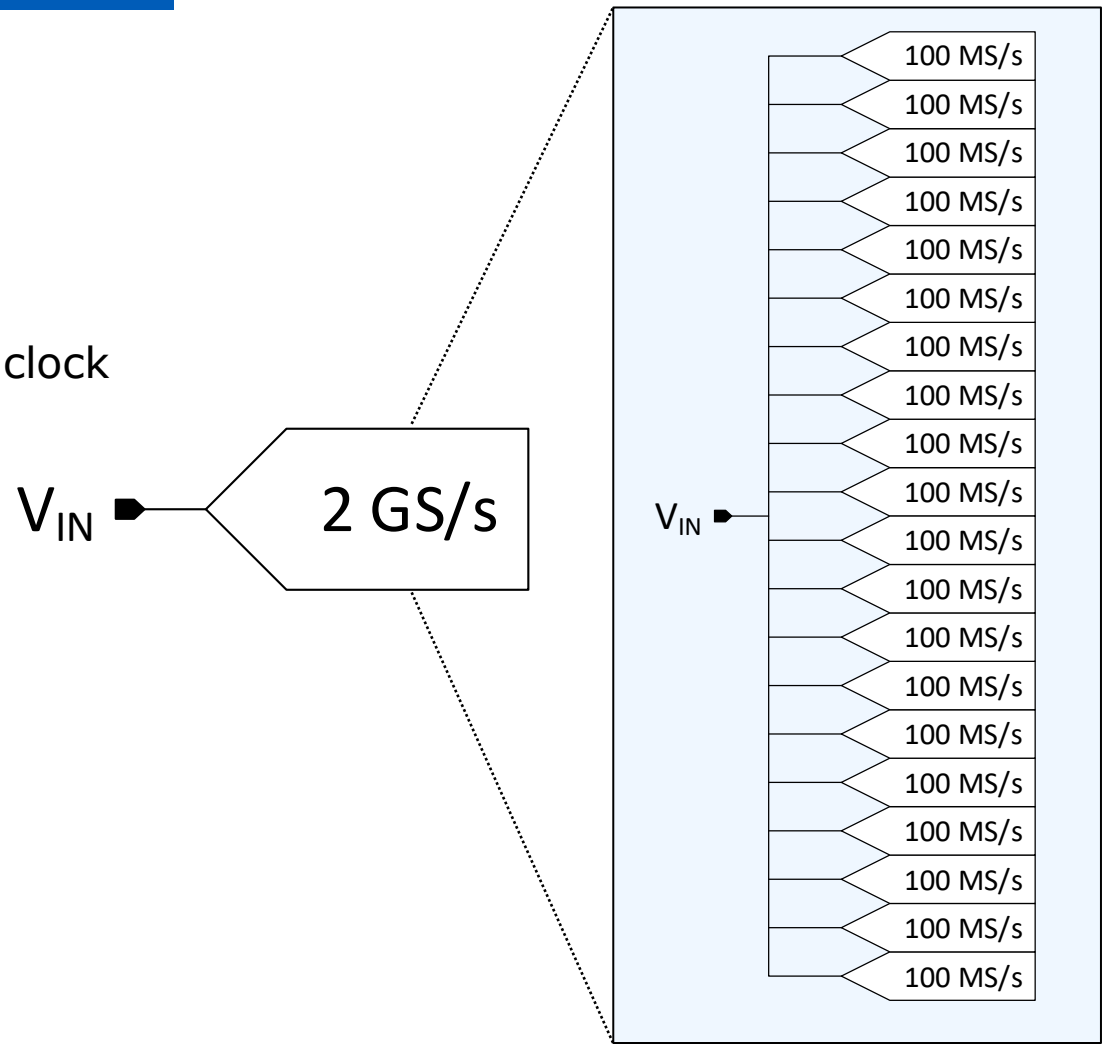


Giga-samples: how do we get there?

- Two possible strategies:

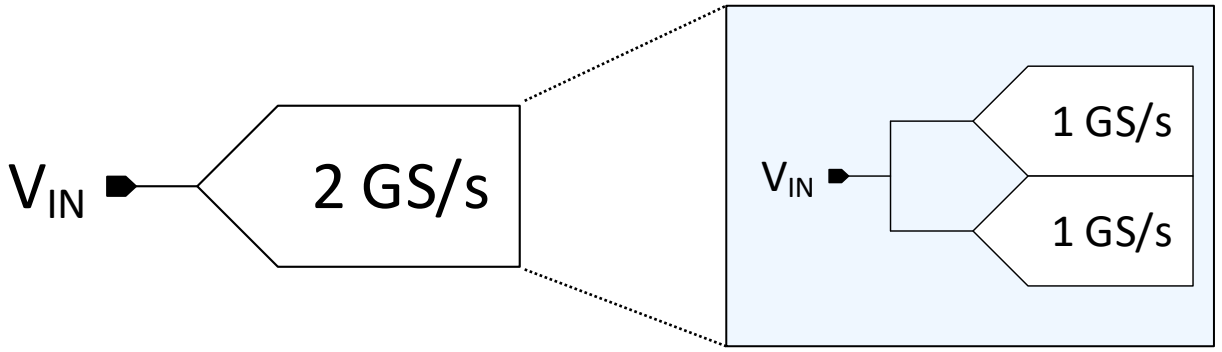
1. Fast single-channel
   - 😐 Practical technology speed limits
   - ☹ Many clocking overheads don't scale w/ clock
   - ☹ Limited architecture choices

2. Interleave several slower channels
   - ☹ Interleave errors (spurs)
     - 😐 Easy to correct: Offset, Gain
     - ☹ Hard to correct: Skew, Bandwidth
   - ☹ Larger input load to drive
   - ☹ Larger area



Giga-samples: how do we get there?

- Combine both strategies
  - First: maximize channel speed
  - Then: interleave as necessary



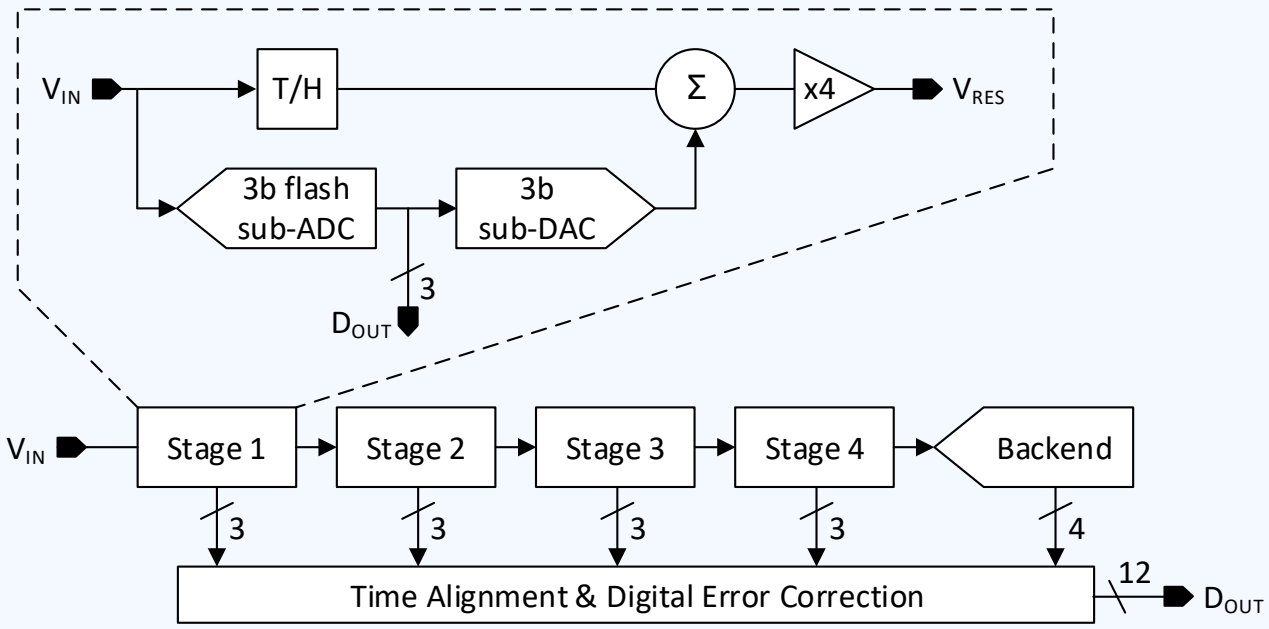
Core mission statement:

Maximize per-channel speed!

Pipelining

- Pipelining
  - Appears in all medium/high resolution giga-sample ADCs
  - Break task into smaller pieces
  - Pass incomplete result along for more processing
- Minimize # of operations in critical timing path
  - Sample
  - Quantize
  - Amplify

Example 3b/stage Pipelined ADC

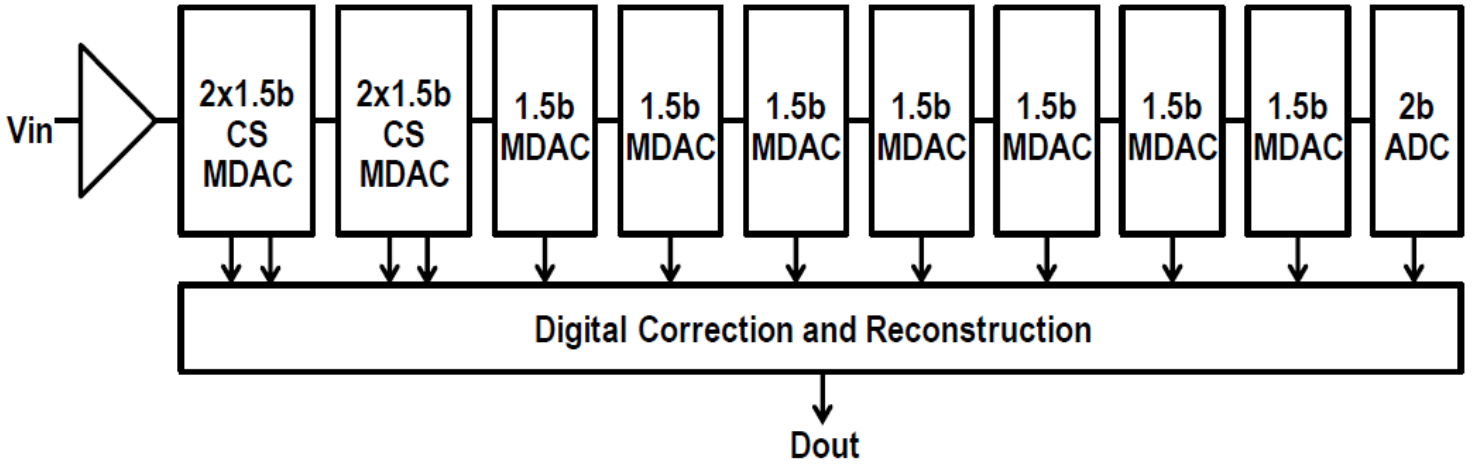


- 2b/stage of quantization
- 1b/stage of redundancy (error correction)

Case study: Deep Pipeline

[Wu, ISSCC 2016]

System	4 GS/s
Channel	1 GS/s
SNDR	56 dB
SFDR	68 dB
Power	300 mW
FoM_W	146 fJ/cs

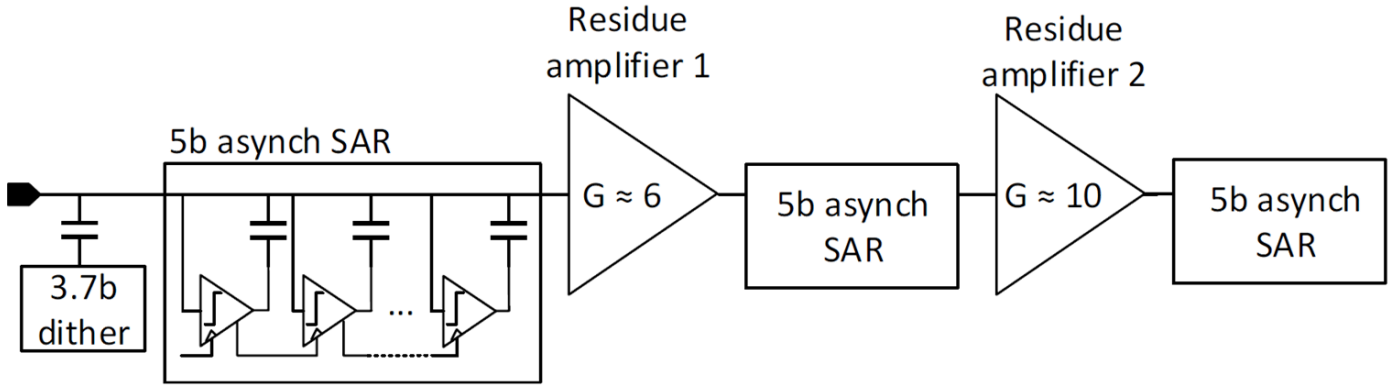


- 1.5b/stage Flash ADC Quantizer
  - ☺ Fast! Minimum set of actions per stage
  - ☹ Many stages / residue amplifiers

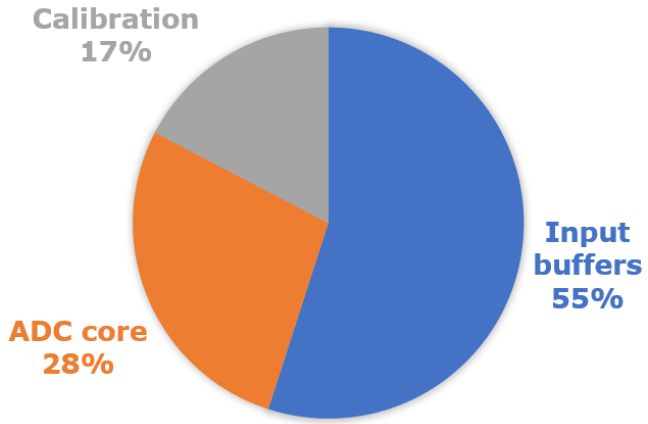
Case study: Pipelined SAR

[Vaz, ISSCC 2017]

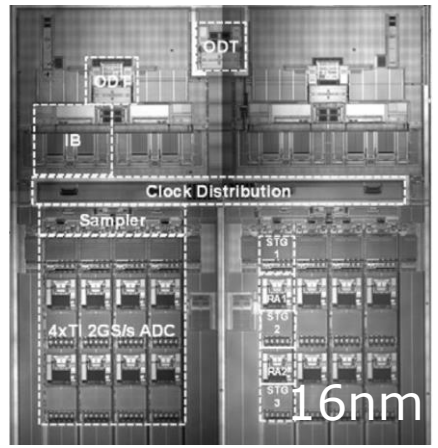
System	4 GS/s
Channel	500 MS/s
SNDR	57 dB
SFDR	67 dB
Power	513 mW
FoM_W	214 fJ/cs



- SAR as a sub-ADC
  - ☺ Fewer stages / amplifiers
  - ☺ Power efficient sub-ADC
  - ☹ Slower channel speed



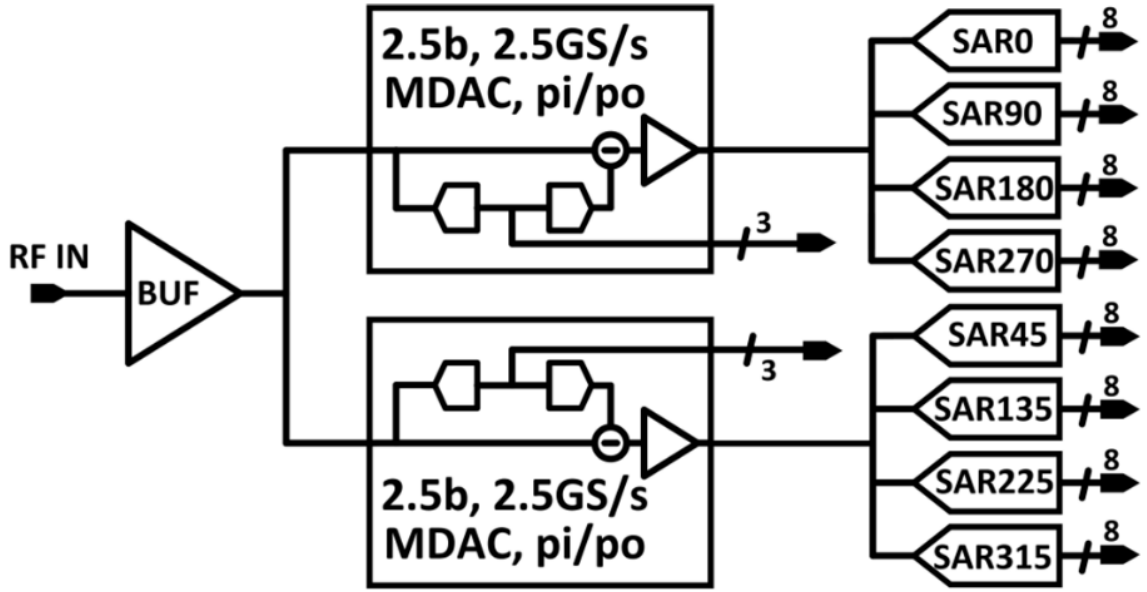
Area = 1mm²



Case study: Hybrid Pipeline

[Brandolini, JSSC 2015]

System	5 GS/s
Channel	2.5 GS/s
SNDR	52 dB
SFDR	58 dB
Power	150 mW
FoM_W	96 fJ/cs

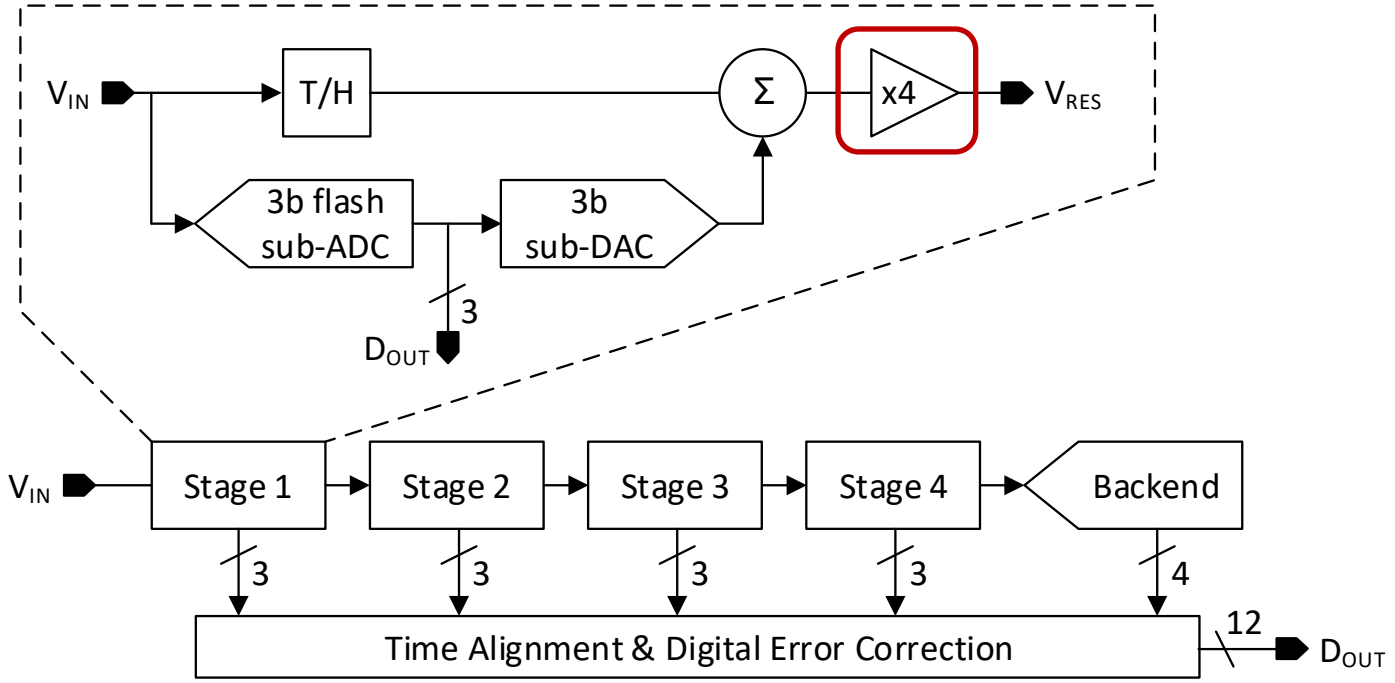


- Fast frontend, slower backend
  - ☺ Fast frontend minimizes interleave factor
  - ☺ Interleaved SARs improve backend efficiency
  - 😐 Frontend amplifiers still power-hungry

AMPLIFICATION: THE HIDDEN BOTTLENECK

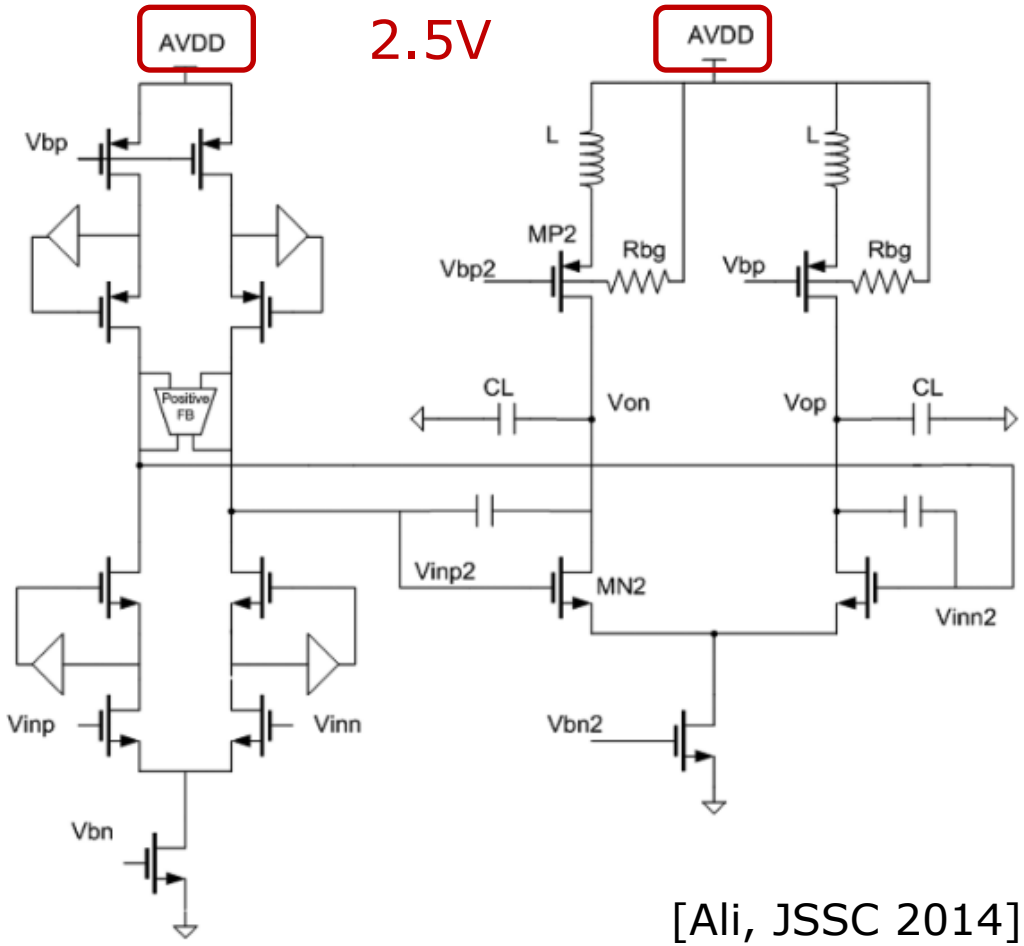
Amplification

- Pipelining requires passing along analog residues
- To go high speed, you need good amplifiers!



Case study: Industry Gigasample ADCs

- Class-A opamps in nanoscale CMOS
  - ☹ Not enough voltage headroom
  - ☹ Poor efficiency / technology scaling
- Requires a special high-voltage supply
  - ☹ Eliminates *all hope* of high efficiency
- But lacking better options, this is still what many in industry use...



[Ali, JSSC 2014]

Case study: Industry Gigasample ADCs

[Wu, VLSI 2013]

Fs	5.4 GS/s
SNDR	52 dB
Power	500 mW

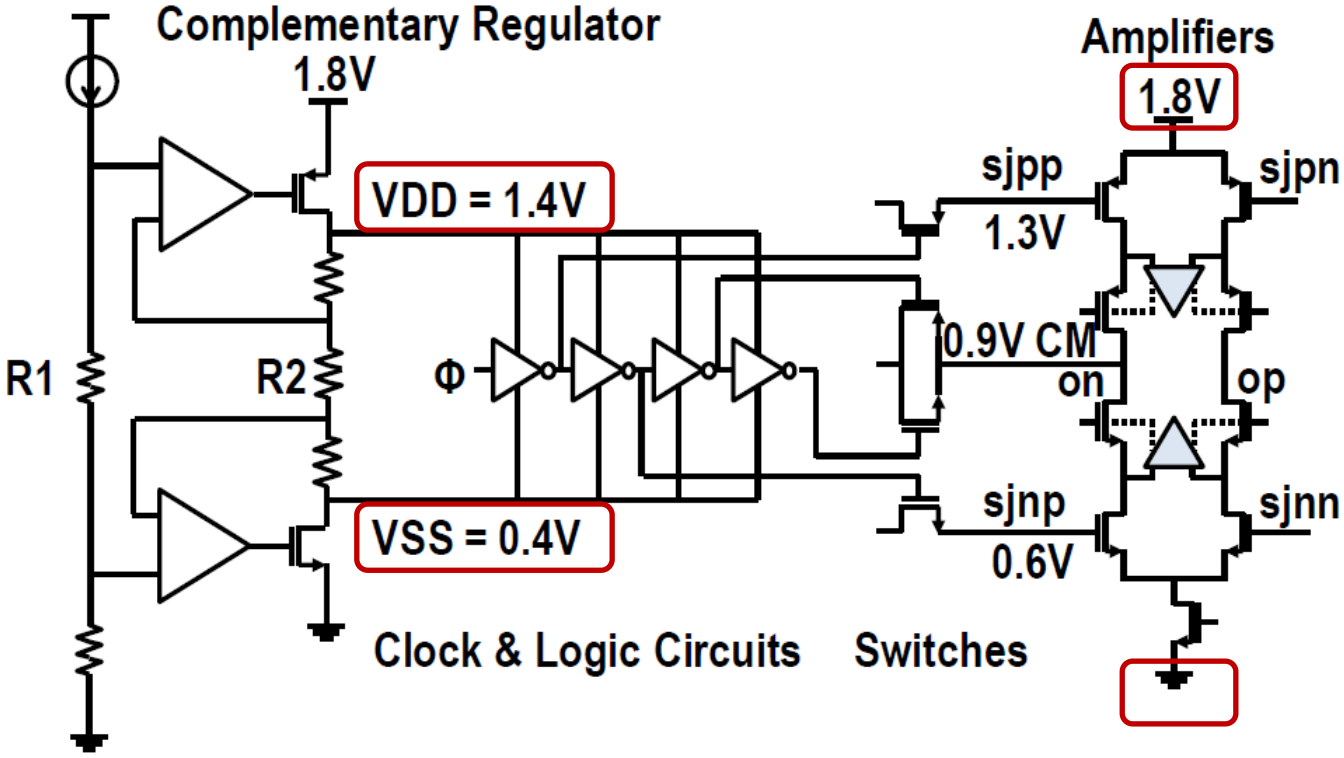
[Wu, ISSCC 2016]

Fs	4 GS/s
SNDR	56 dB
Power	300 mW

[Brandolini, JSSC 2015]

Fs	5 GS/s
SNDR	52 dB
Power	150 mW

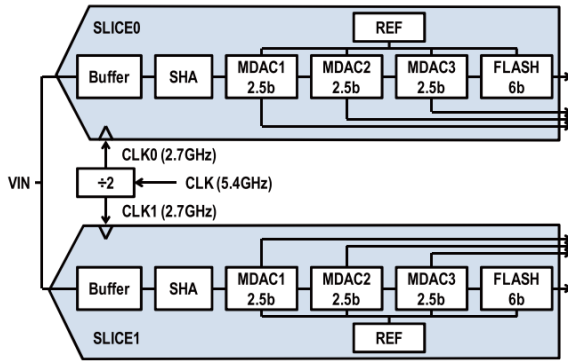
- All 3 ADCs use the same residue amplifier on 1.8V
- Core circuits on 1.4V/0.4V



Case study: Industry Gigasample ADCs

[Wu, VLSI 2013]

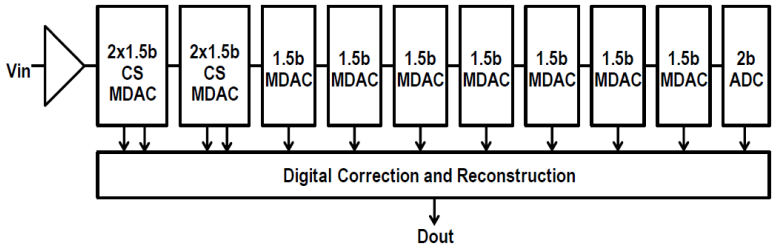
Fs	5.4 GS/s
SNDR	52 dB
Power	500 mW



8 high-performance amps

[Wu, ISSCC 2016]

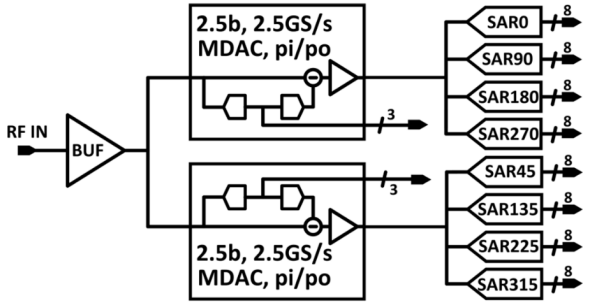
Fs	4 GS/s
SNDR	56 dB
Power	300 mW



2 high-performance amps
14 low-performance amps

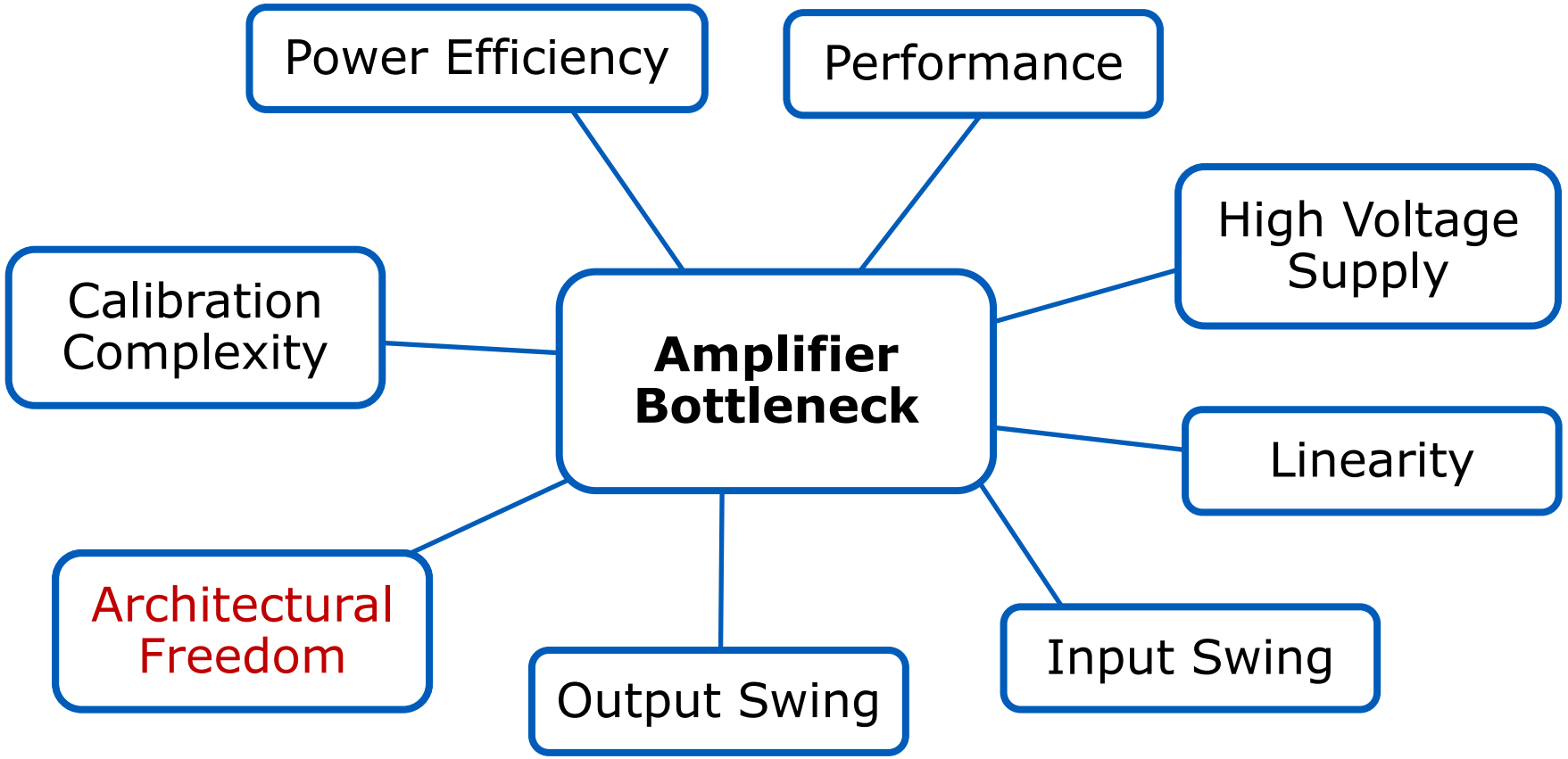
[Brandolini, JSSC 2015]

Fs	5 GS/s
SNDR	52 dB
Power	150 mW



2 high-performance amps

Amplification: The Hidden Bottleneck



Conclusions: Amplifier Bottleneck

- Class-A opamps will *never* be good in scaled CMOS
  - Severely constrains ADC design freedoms
  - 2010's were the era of the (amplifier-less) SAR ADC

- A new approach is needed!

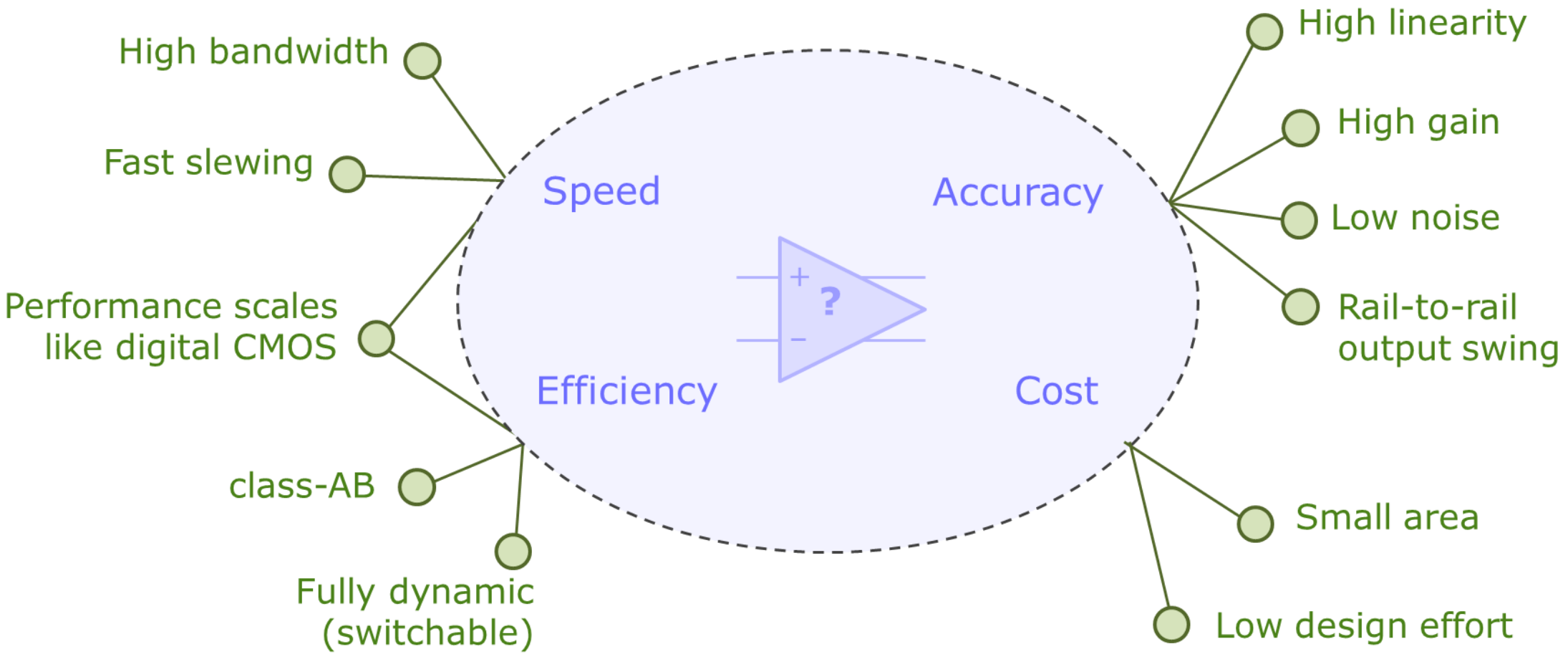
EMERGING AMPLIFICATION SOLUTIONS

Emerging Amplification Solutions

- Open loop
  - ★ Gm-C integrator
  - ★ Gm-R amplifier
  - Charge-pump based
- Feedback
  - ★ Ring amplifier
  - Zero-crossing based circuit
  - Charge-steering amplifier
  - Digital amplifier

★ Found in state-of-the-art Gigasample ADCs

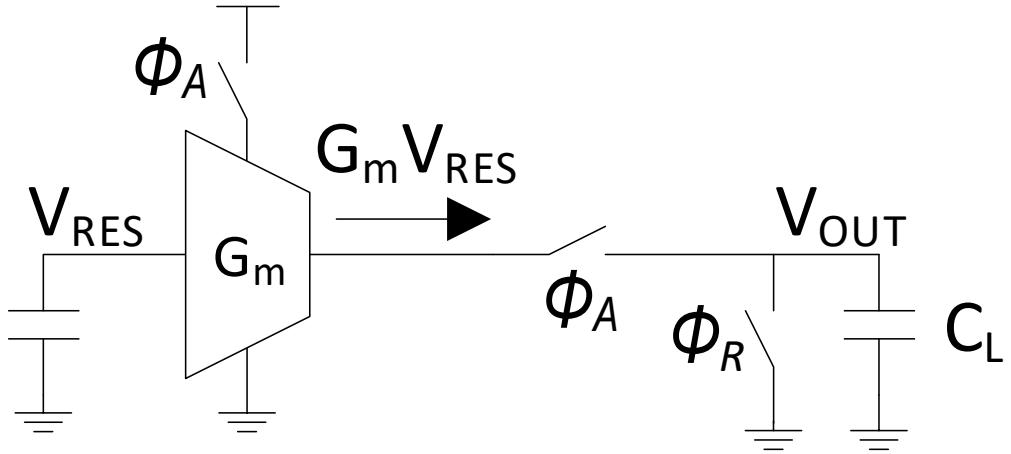
Amplifier Wishlist



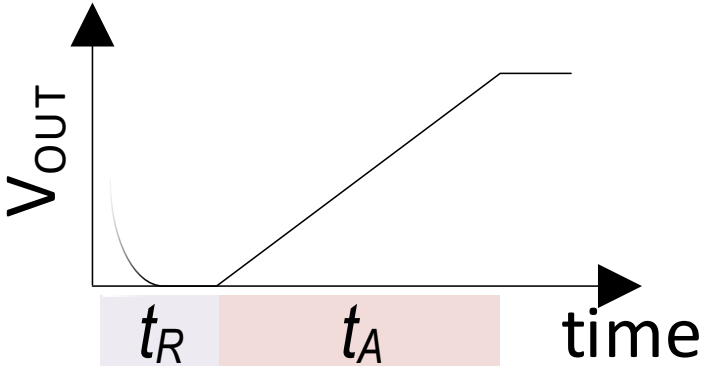
Gm-C integrator

- Basic idea: Integrate current $G_m V_{RES}$ onto load capacitor

  - ☺ Fast (open-loop)
  - ☺ Fully dynamic (switchable)
  - ☺ Inherent filtering (sinc)
  - ☺ Good efficiency
  - ☹ Poor linearity
  - ☹ Small input swing
  - ☹ Small output swing
  - ☹ Sensitive to jitter
  - ☹ Sensitive to PVT



$$A_V = \frac{G_m \cdot t_a}{C_L}$$

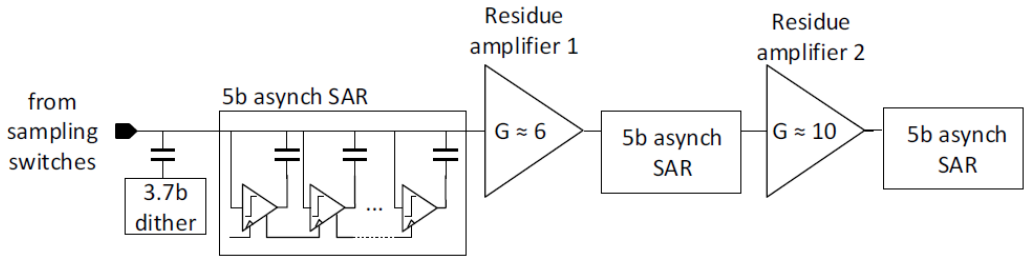


Case Study: Gm-C Integrator

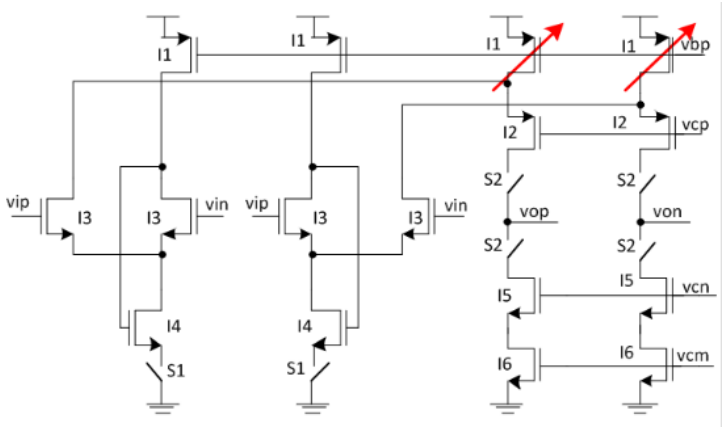
[Vaz, ISSCC 2017]

System	4 GS/s
Channel	500 MS/s
SNDR	57 dB
SFDR	67 dB
Power	513 mW
FoM_W	214 fJ/cs

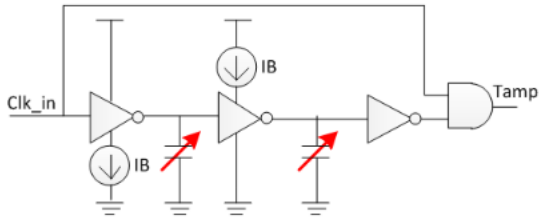
Channel:



Gm-C:



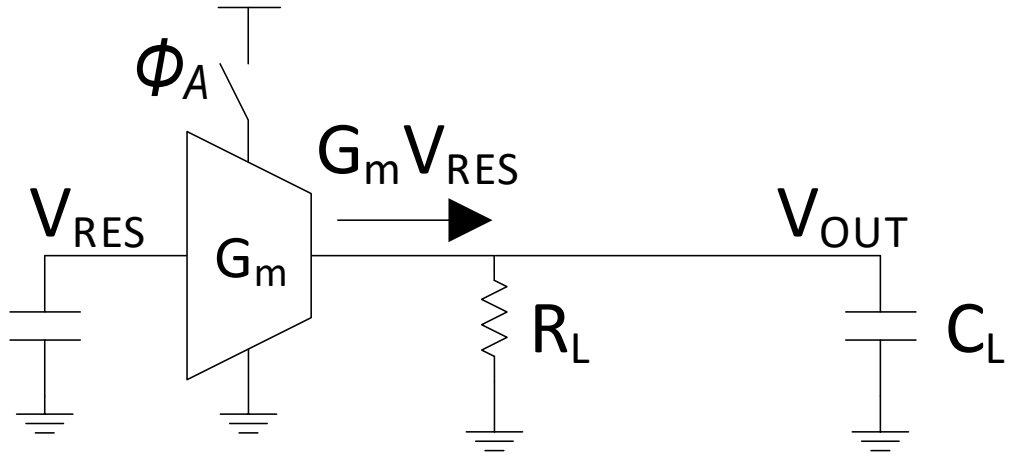
Tunable integration time:



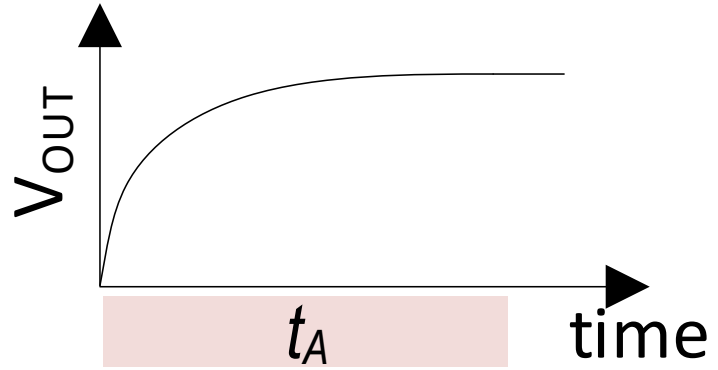
Gm-R amplifier

- Basic idea: RC settle voltage $G_m V_{RES} R_L$ across load capacitor

  - ☺ Even faster! (no pre-clearing)
  - ☺ Fully dynamic (switchable)
  - ☺ Good efficiency
  - 😐 Moderate PVT sensitivity
  - ☹ Poor linearity
  - ☹ Small input swing
  - ☹ Small output swing



$$A_V = G_m \cdot R_L$$

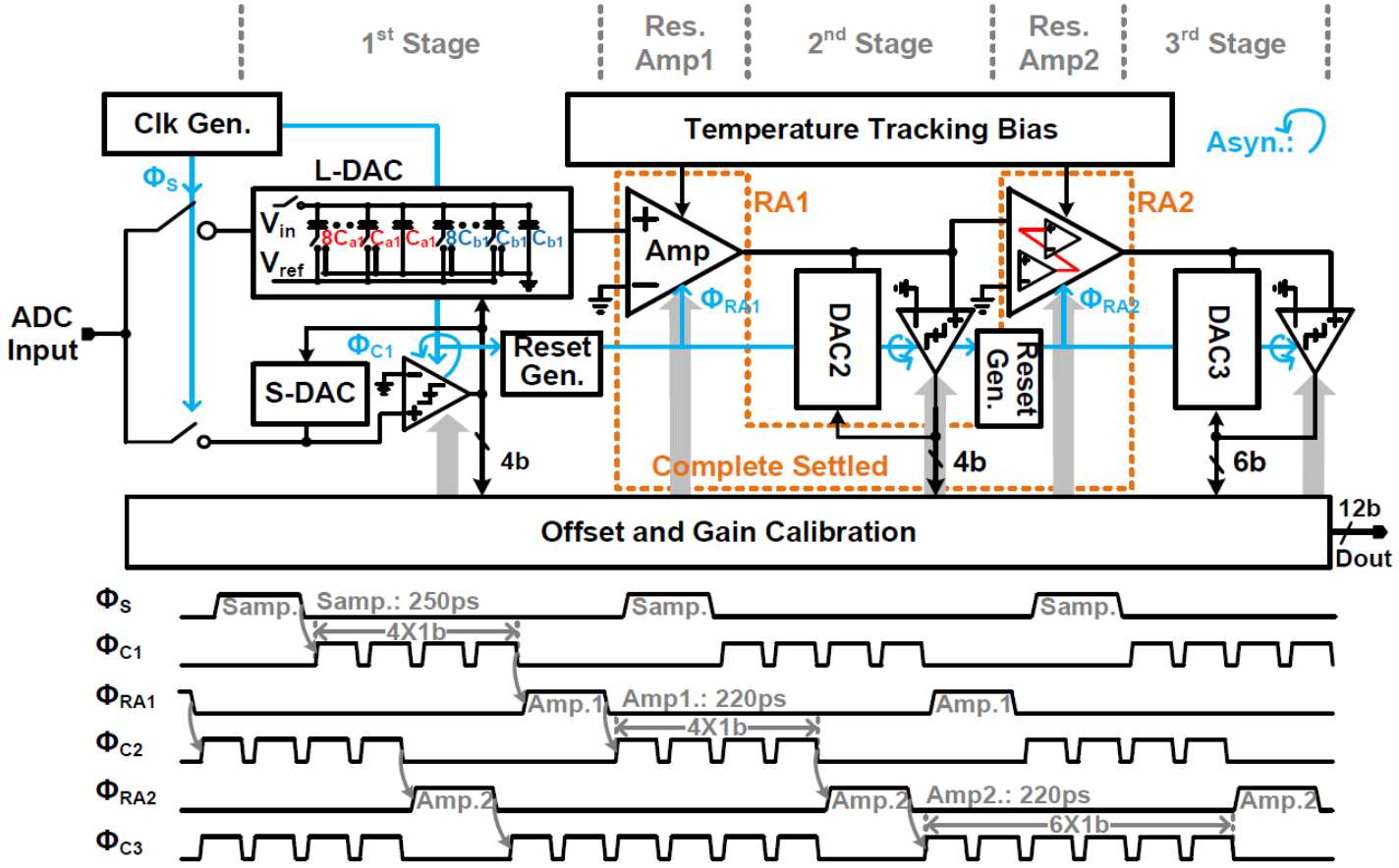


Case study: Gm-R Amplifier

[Jiang, ISSCC 2019]

System	1 GS/s
Channel	1 GS/s
SNDR	60 dB
SFDR	75 dB
Power	8 mW
FoM_W	9 fJ/cs

- Current SoTA for single-channel gigasample ADCs

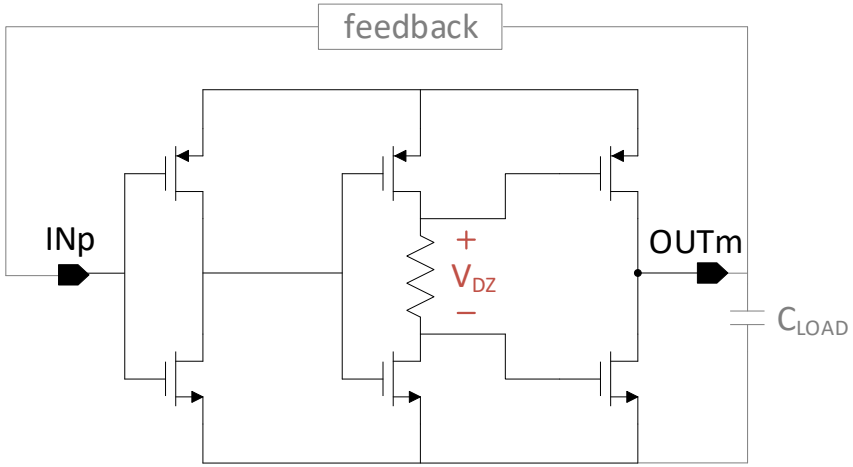


Ring Amplifier

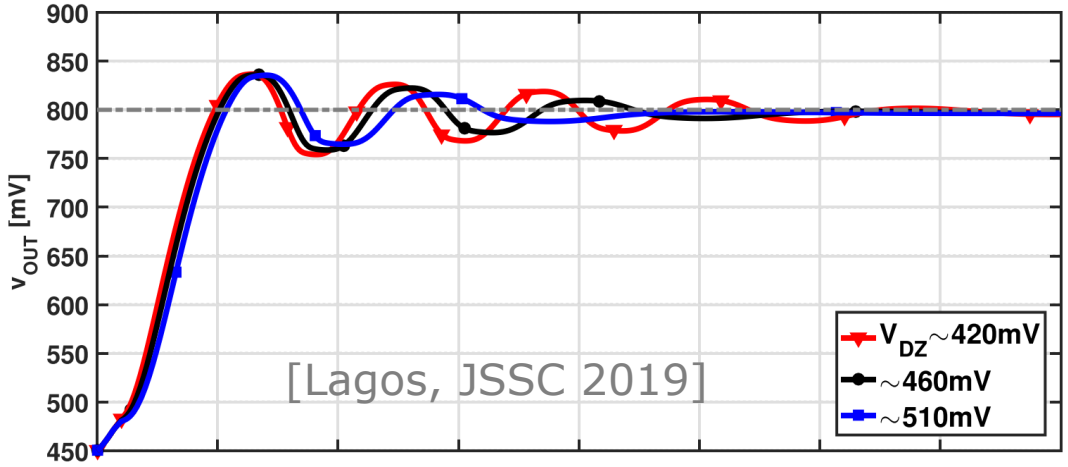
- Basic idea: Start in a high efficiency but unstable state and then dynamically stabilize with large-signal feedback

  [Hershberg, JSSC 2012]

- ☺ High efficiency
- ☺ High speed
- ☺ Wide output swing
- ☺ Excellent linearity
- ☺ Scales with digital
- ☺ Fully dynamic (switchable)
- 😐 Moderate PVT sensitivity



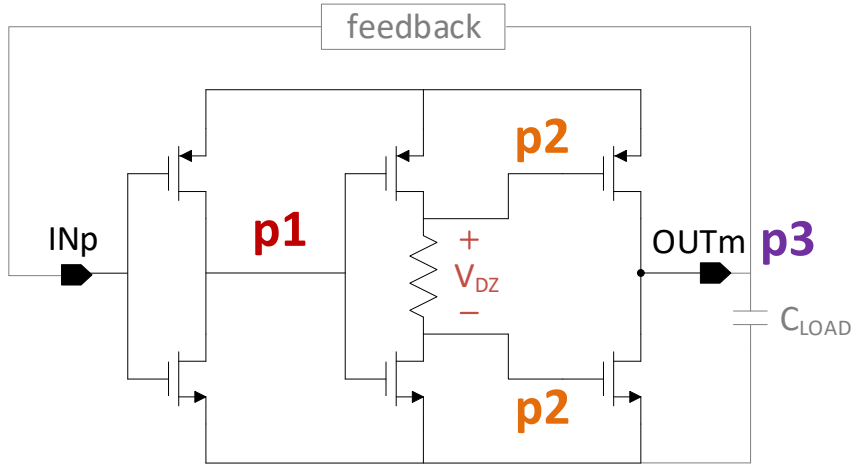
[Lim, JSSC 2015 (1)]

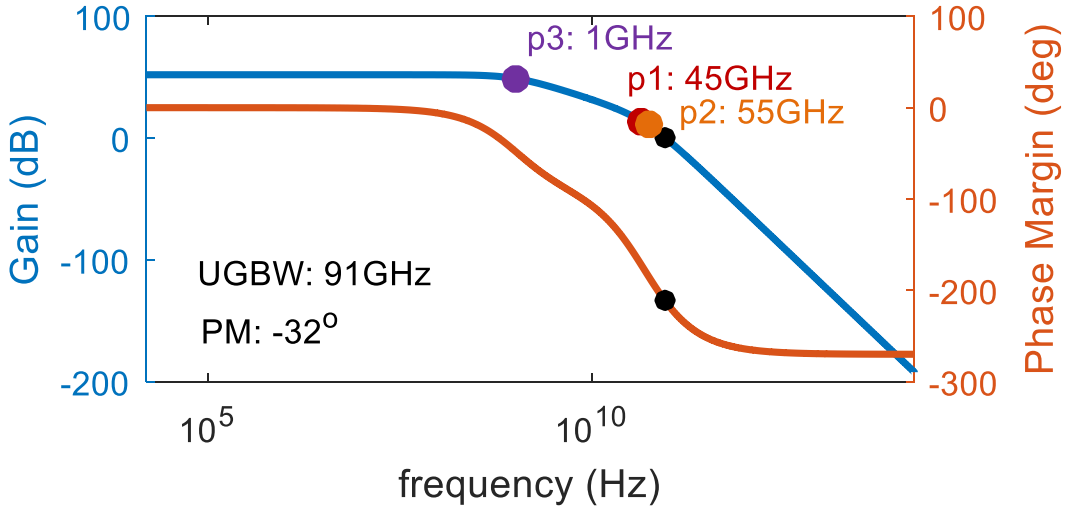


[Lagos, JSSC 2019]

Ring Amplifier

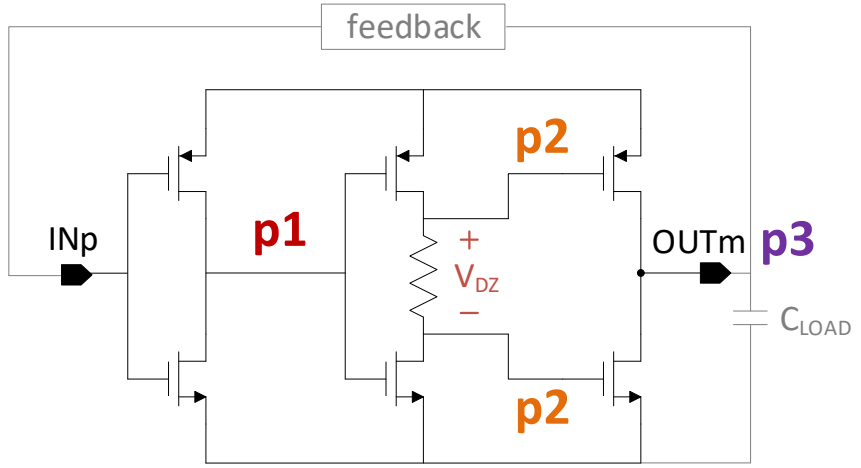
- Transient, large signal paradigm
- The AC view
  - **Make p1 & p2 as fast as possible**

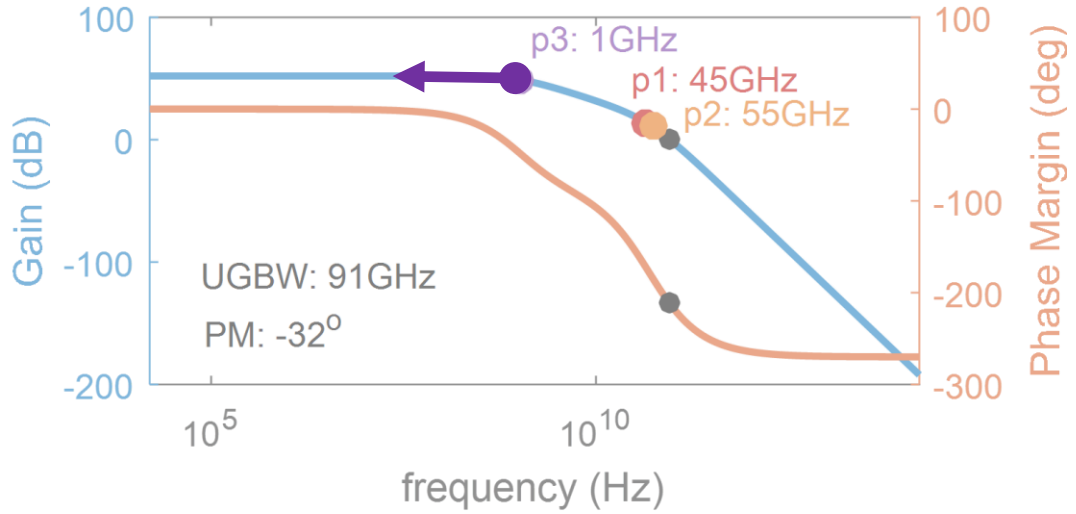




Ring Amplifier

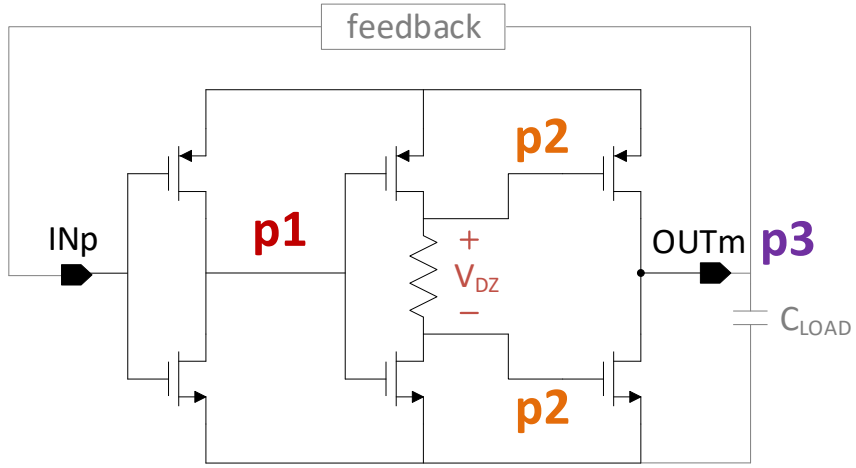
- Transient, large signal paradigm
- The AC view
  - Make p1 & p2 as fast as possible
  - **Dynamically reduce p3**

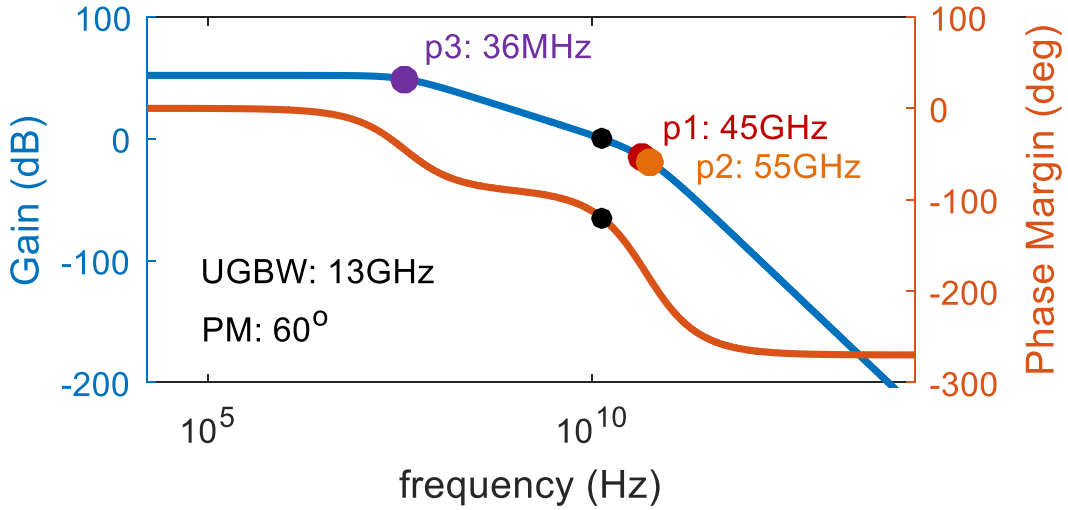




Ring Amplifier

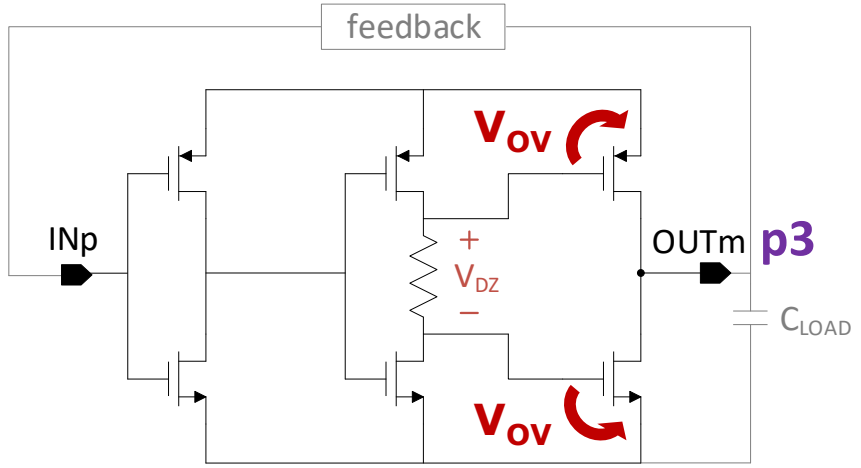
- Transient, large signal paradigm
- The AC view
  - Make p1 & p2 as fast as possible
  - Dynamically reduce p3
  - **ring oscillator → ring amplifier**

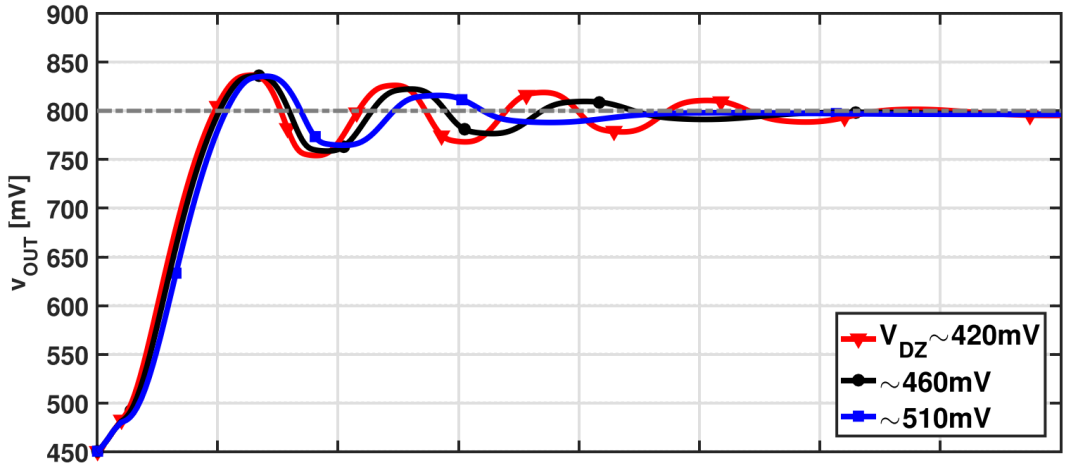




Ring Amplifier

- Transient, large signal paradigm
- The DC / transient view
  - **V_{ov} initially maximum**
    - Slew-rate at theoretical max. ☺

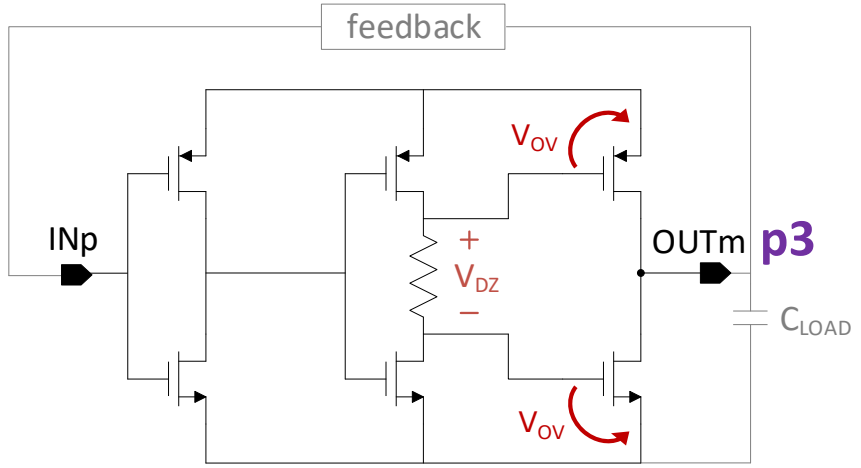


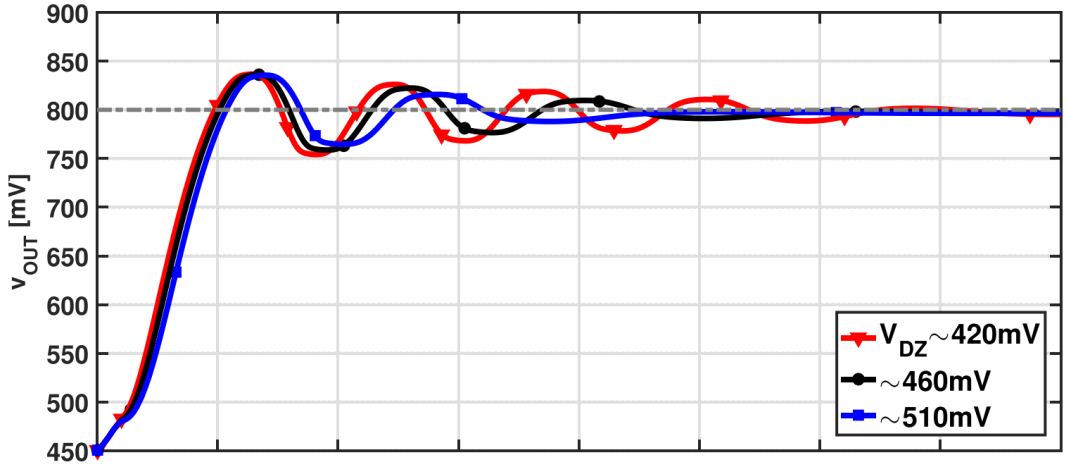


Ring Amplifier

- Transient, large signal paradigm

- The DC / transient view
  - V_{OV} initially maximum
    - Slew-rate at theoretical max. ☺
  - **V_{OV} dynamically reduced to adjust P3**
    - Reduces V_{DSAT} → swing/linearity ☺
    - Increases r_o → gain/linearity ☺
    - Reduces g_m → noise filtering ☺



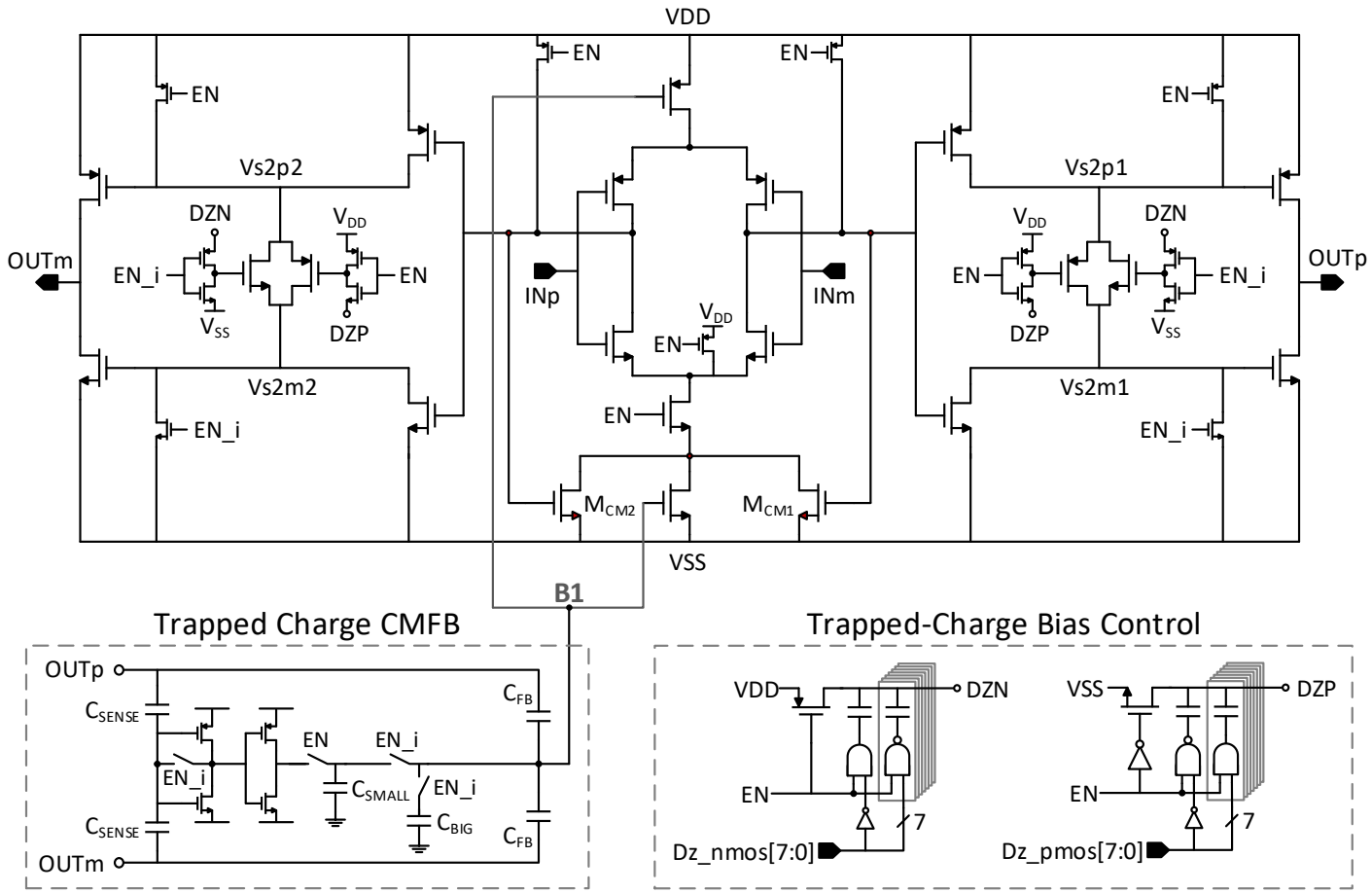


Case study: Ring Amplifier

[Hershberg, ISSCC 2019 (1)]

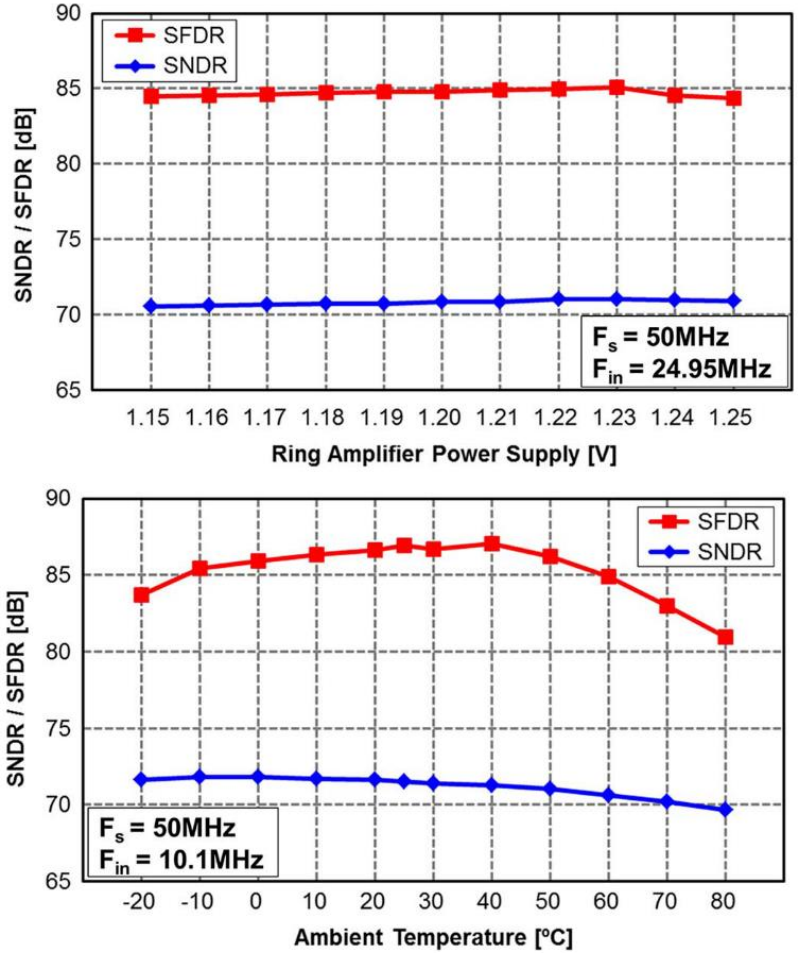
System	3.2 GS/s
Channel	800 MS/s
SNDR	63 dB
SFDR	80 dB
Power	61.3 mW
FoM_W	19 fJ/cs

- Order-of-magnitude improvement in SoTA
- 36 ringamps in system
  - Bottleneck solved?



Ringamp Robustness Techniques

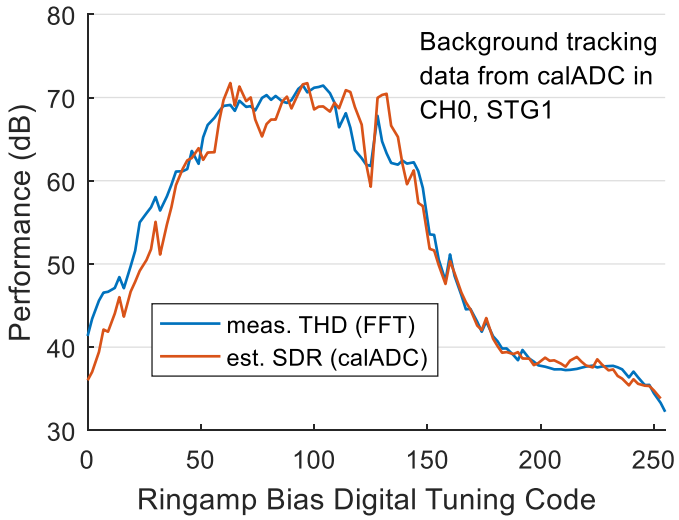
- Option 1: Design with extra margin
  - ☺ Calibration free
  - 😐 Requires some sacrifice in speed
- Still can achieve SoTA performance
  - 3 stage ringamp [Lim, JSSC 2015 (2)]
  - 4 stage ringamp [Lim, VLSI 2017]

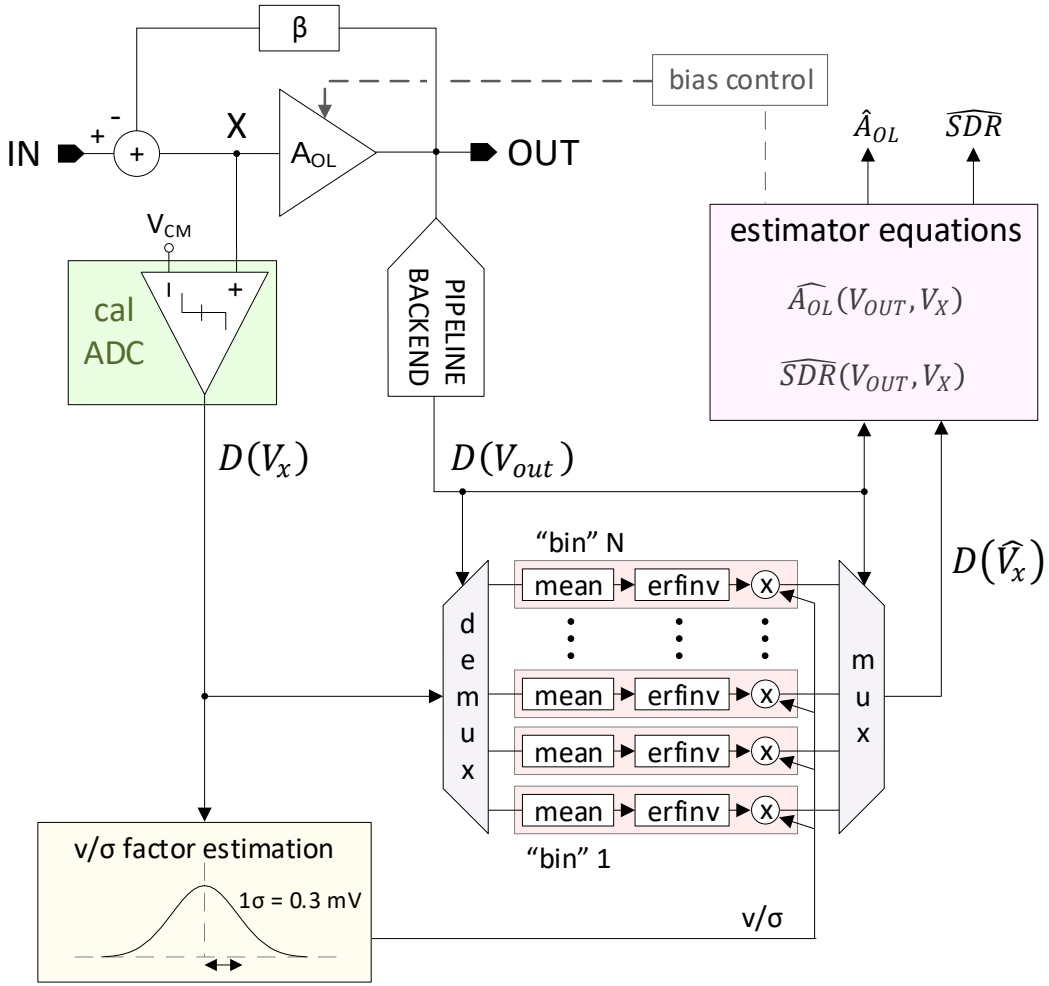


[Lim, JSSC 2015]

Ringamp Robustness Techniques

- Option 2: Use background tracking or calibration techniques
  - ☺ Optimum performance
  - 😐 Extra analog/digital complexity

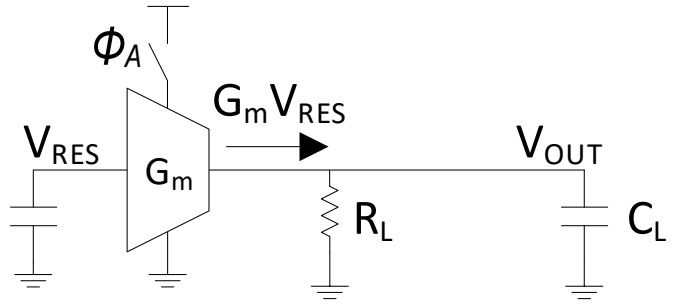




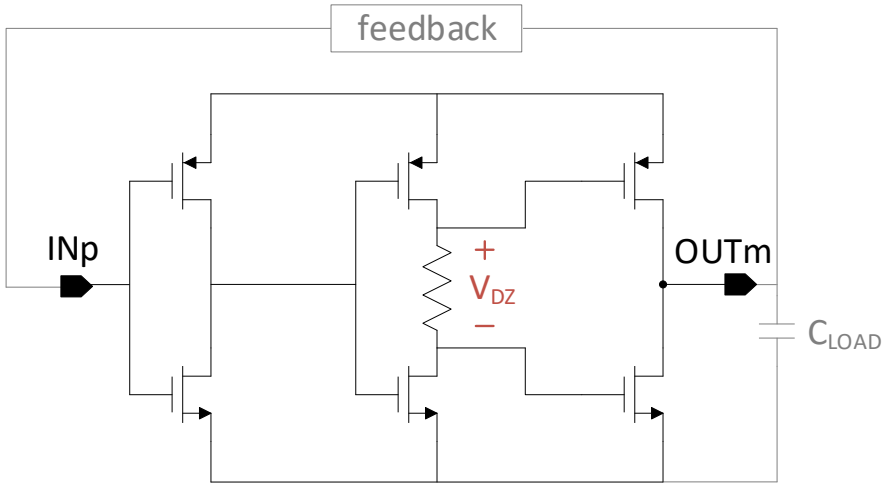
[Hershberg, ISSCC 2019 (1)]

Conclusion: Emerging Amplification

- Open-loop where it makes sense
  - E.g. for *very* fast amplification



- Ringamps for everything else
  - Any input swing, any output swing
  - Any resolution, any speed
  - All circuits: ADC, VGA, Filter, PLL, etc.



DESIGNING FOR RECONFIGURABILITY

5G NR FR2 specs revisited

Wide range of channel bandwidths and modulations:

- 5G Bandwidth Specs
  - Channel: 50MHz, 100MHz, 200MHz, 400MHz
  - Max. Aggregation: 800MHz
  - Widest Band: 3.25GHz (24.25GHz – 27.50GHz)
  - Agg. 28GHz Bands: 5.25GHz (24.25GHz – 29.50GHz)

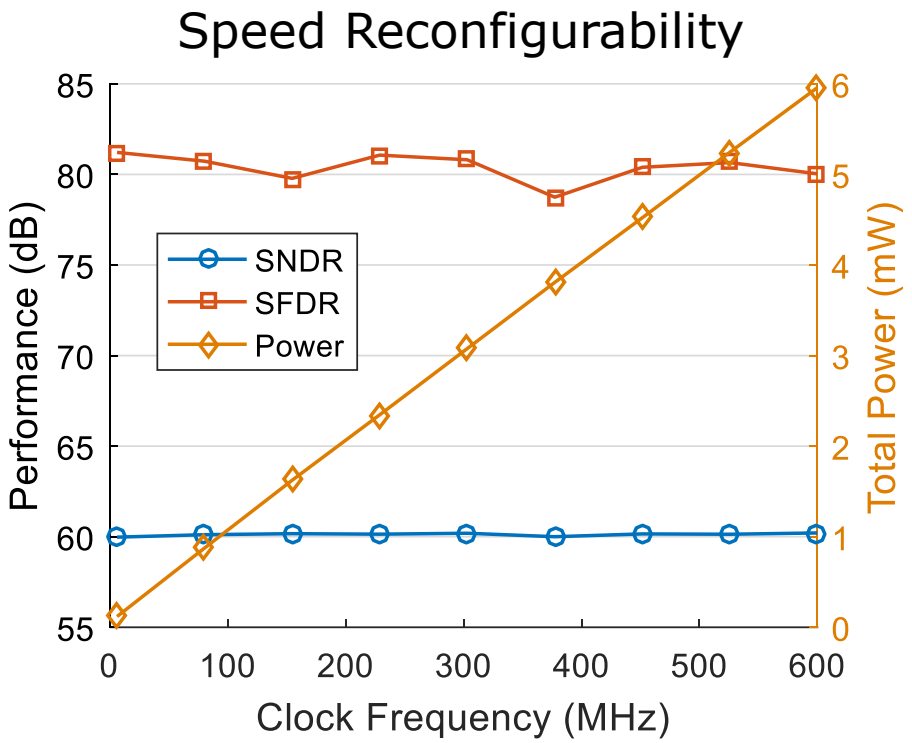
- 5G Modulation Specs
  - QPSK, 16 QAM, 64 QAM, 256 QAM
  - Future: 1024 QAM

➔ A reconfigurable multi-standard ADC is a clear advantage

ADC Reconfigurability

- Run-time
  - ★ Speed
  - ■ Resolution
- Design-time
  - ★ Architecture

★ = most relevant for 5G

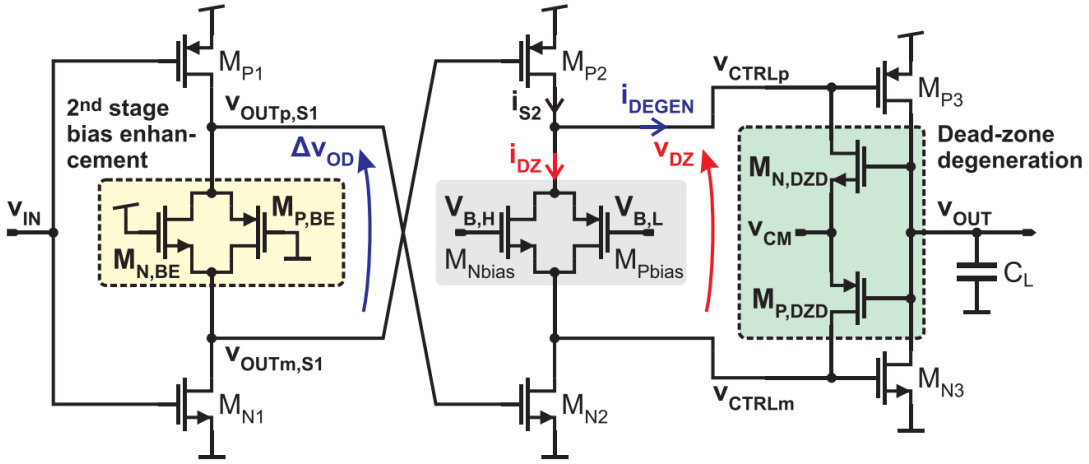


[Hershberg, ISSCC 2019 (2)]

Speed Reconfigurability

- Motivation: constant power efficiency
- 2 ingredients required
  - Event-driven control (clocking)
  - Fully-dynamic power consumption
- Fully-dynamic = no static power
- "Next-gen" amplifiers support this
  - Gm-C
  - Gm-R
  - Ringamp

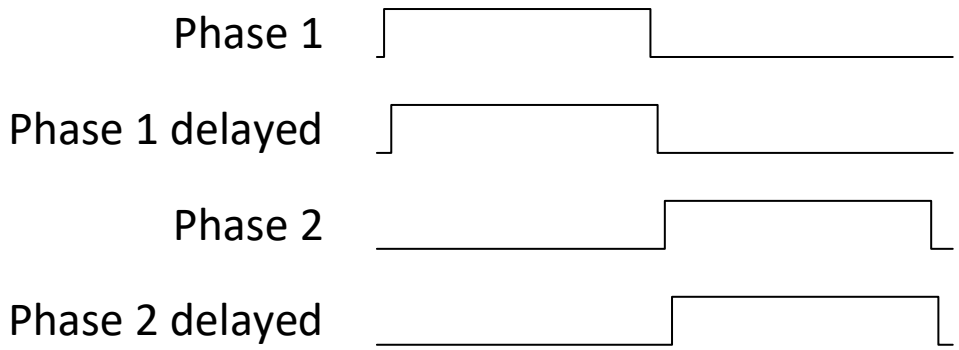
Ringamp with power-gating function

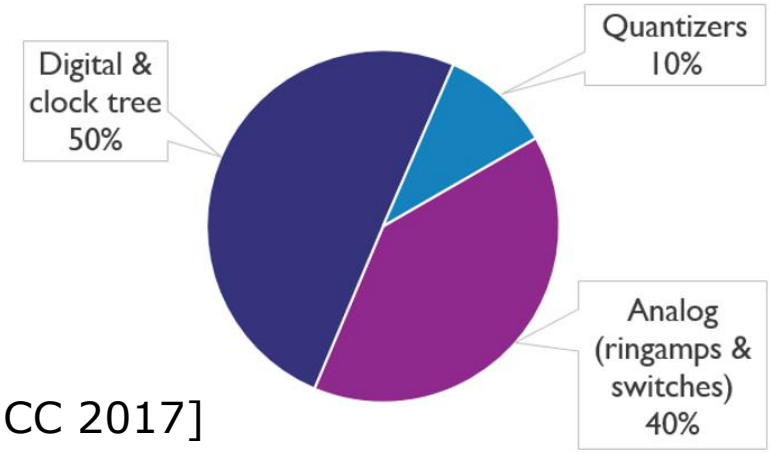


[Lagos, JSSC 2019]

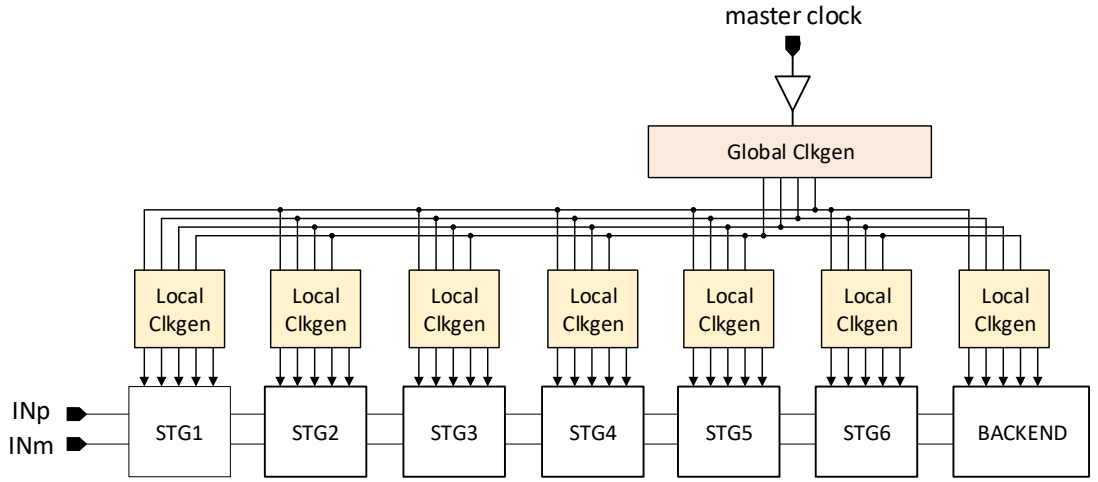
Event-Driven Control: Deep Pipeline

- Conventional: Synchronous 2-phase non-overlapping clock tree
  - Simple & effective at lower speeds
  - But many hidden drawbacks at high speed
- With improvements in amplification tech., clocking becomes the new bottleneck





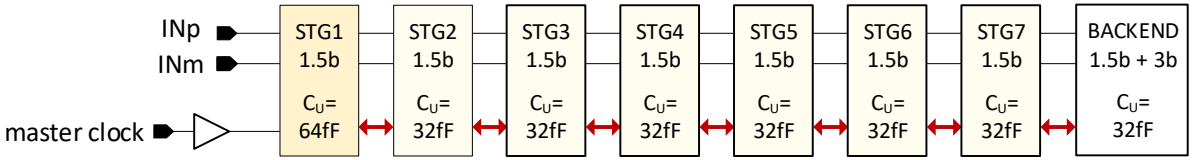
[Lagos, CICC 2017]

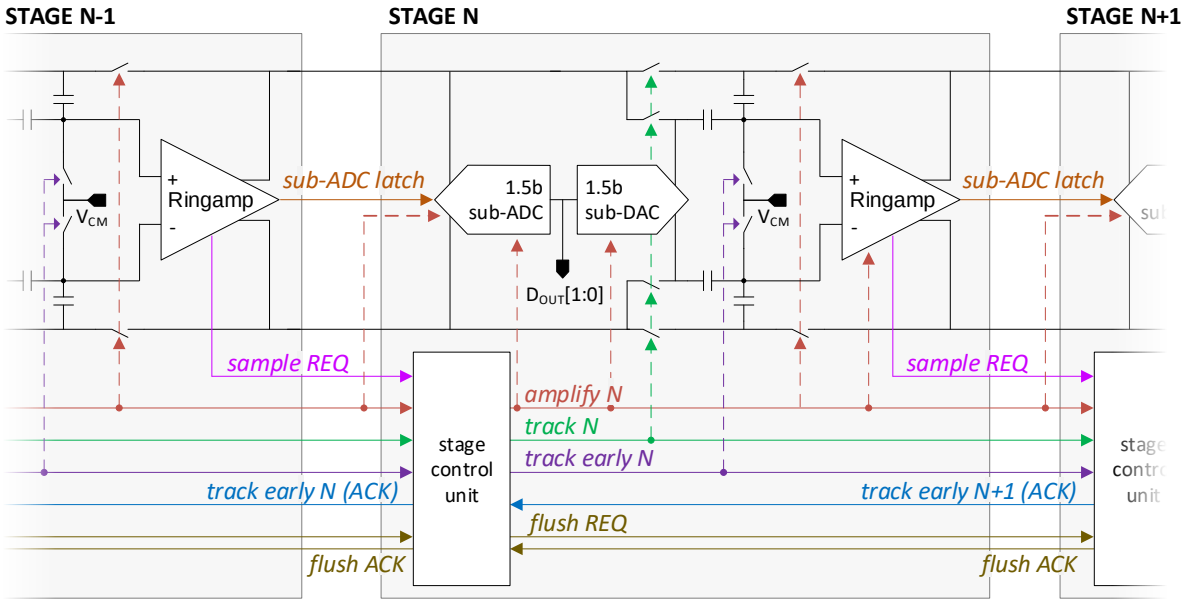


Event-Driven Control: Deep Pipeline

- Local "Stage Control Units" connected by inter-stage control busses
  - Communication
  - Driving local circuits

☺ Correct-by-construction
☺ Minimal global routing
☺ Interleaving advantages
☺ Less sampling jitter
☺ Faster (less timing overhead)



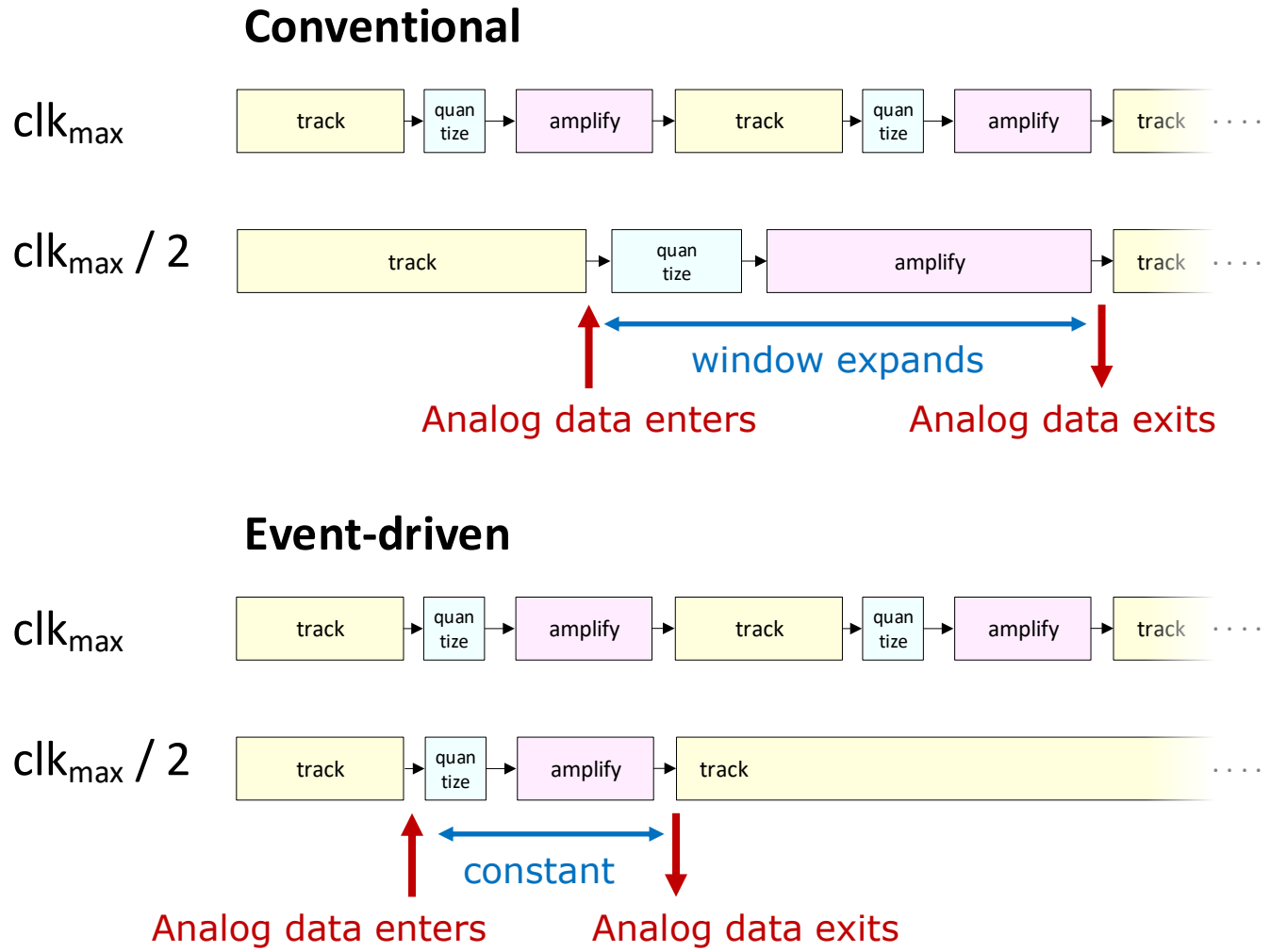


[Hershberg, ISSCC 2019 (2)]

Event-Driven Control: Deep Pipeline

- Internal "chain-reaction" of processing is independent of external clock rate
  - 1MS/s same as 1GS/s

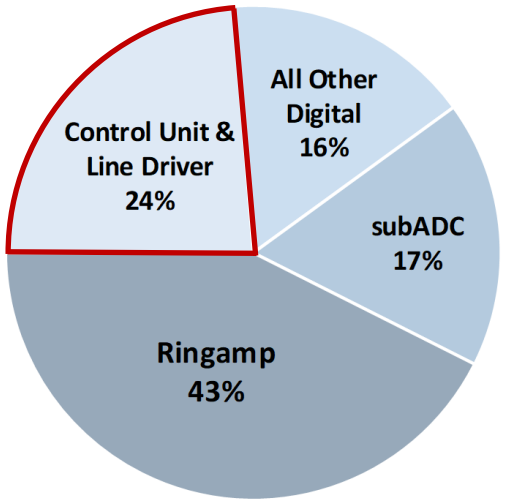
☺ Enables fully-dynamic operation
☺ Auto maximizes track time
☺ Removes many leakage issues

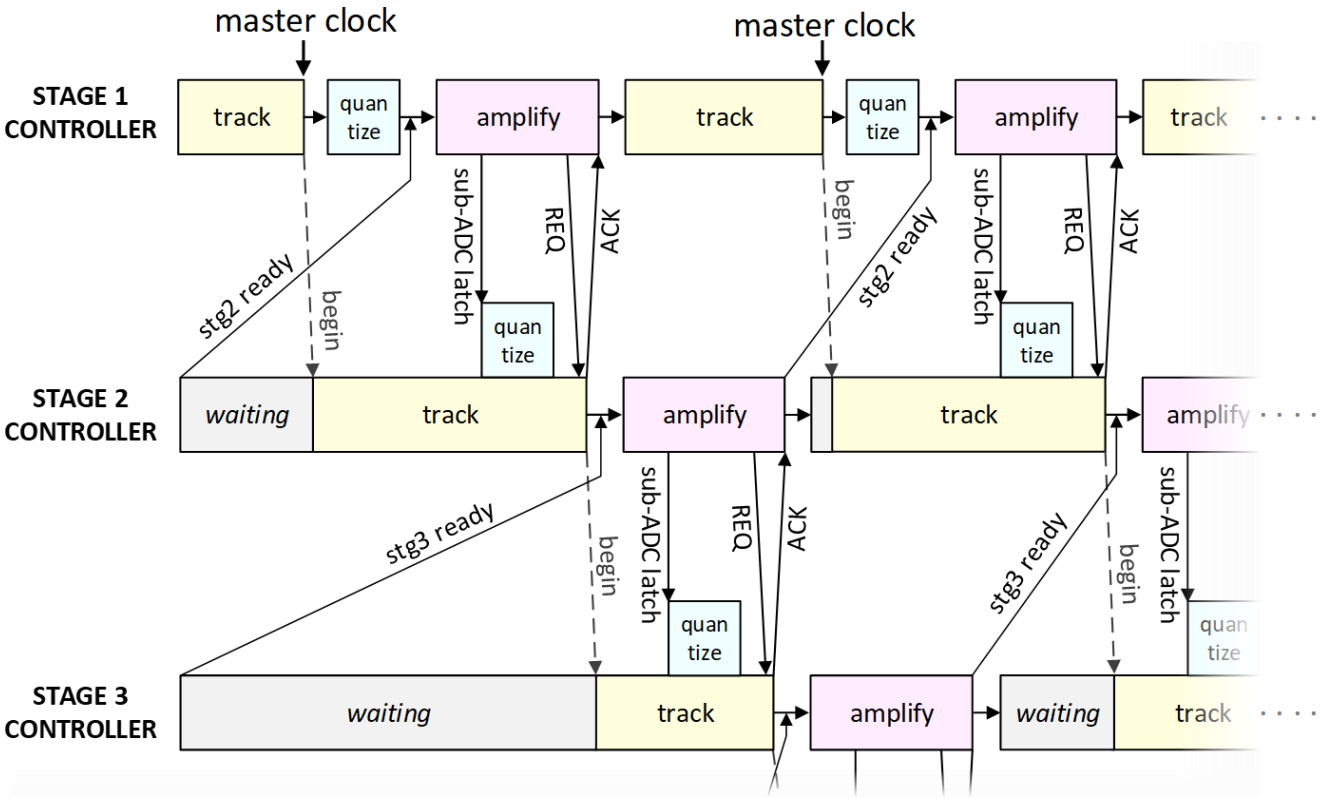


[Hershberg, ISSCC 2019 (2)]

Event-Driven Control: Deep Pipeline

- ☺ More efficient (less power)
- ☺ Reconfigurable behavior
- ☺ No limit to # of clocks/phases
- 😐 Must be careful about deadlocks
- 😐 Validation effort increased





[Hershberg, ISSCC 2019 (2)]

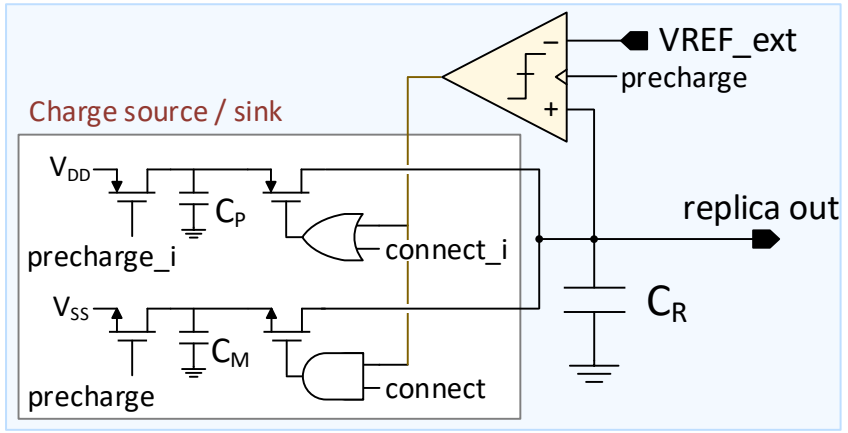
Fully Dynamic Reference Regulation

** Sneak Peek! **

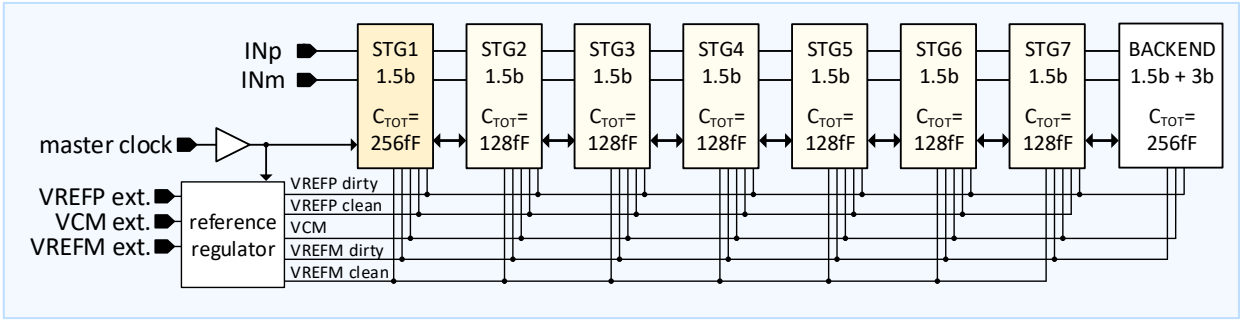
- General-purpose solution
  - Discrete-time comparator-based
    - [Kull, JSSC 2013]
  - Can sub-divide into dirty/clean replicas for low-noise and high-accuracy

☺ Low power
☺ General purpose
😐 Still requires some decap area

Discrete-time regulation circuit:

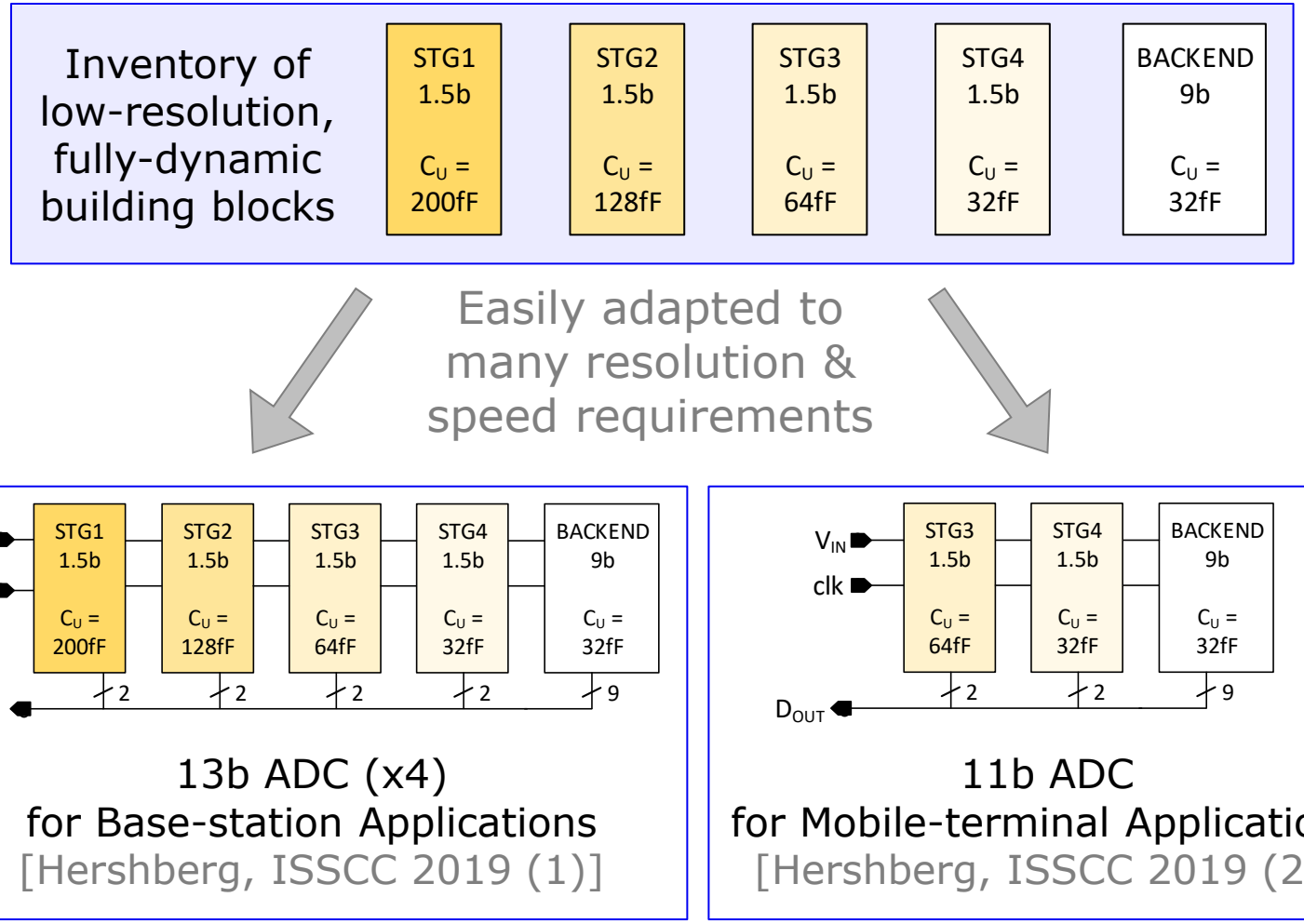


Deep pipeline with dirty/clean reference replicas:



Architecture Reconfigurability

- Design-time circuit re-use
  - Faster time-to-market
  - Less manpower
- Simple, low resolution stages
  - Use "cheap" high performance amplifiers
  - Can simply "chain" together using asynchronous, event-driven control protocols



SUMMARY & CONCLUSION

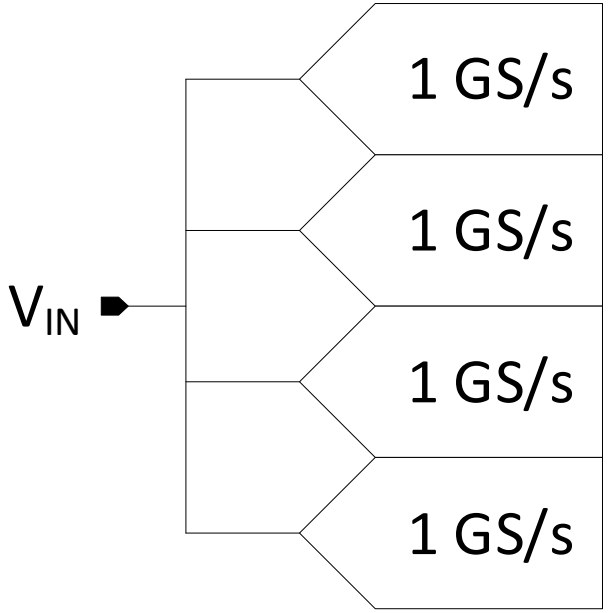
Final Summary

For best performance at high speeds:

First maximize the per-channel speed...

1 GS/s

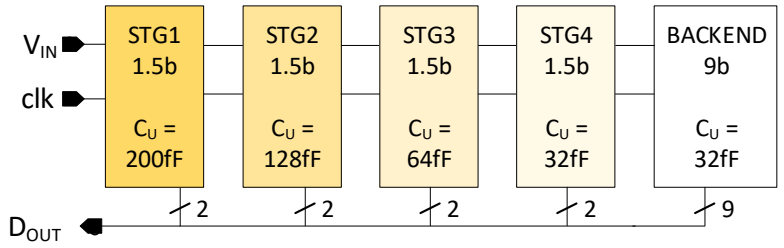
...then interleave as necessary



Final Summary

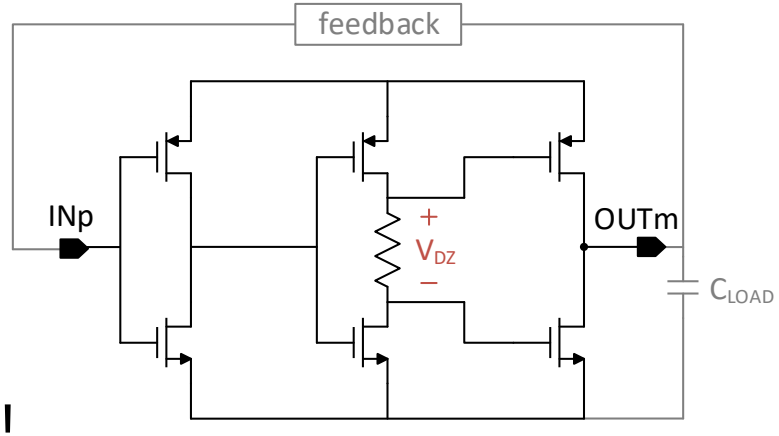
1 GS/s

Pipelining can maximize the per-channel speed



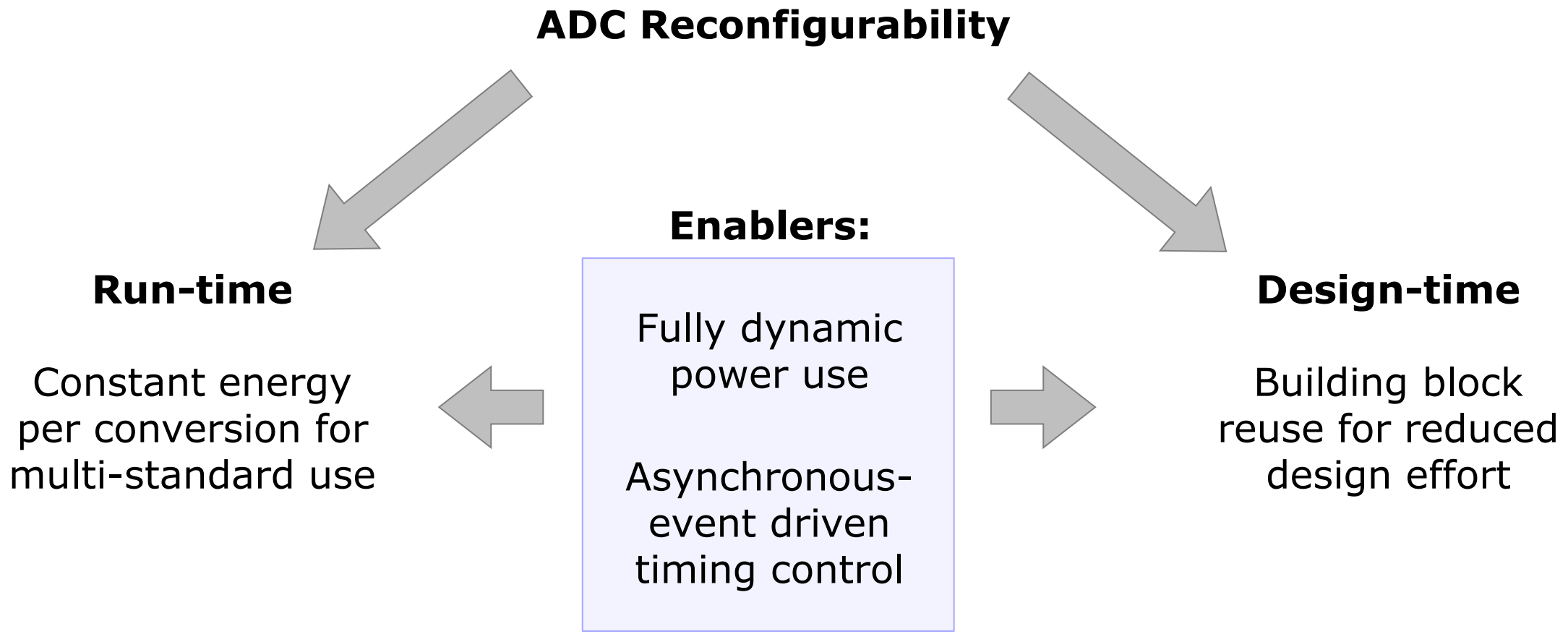
But it is amplifier intensive!

Ringamp



Luckily, new amplification techniques are now available

Final Summary



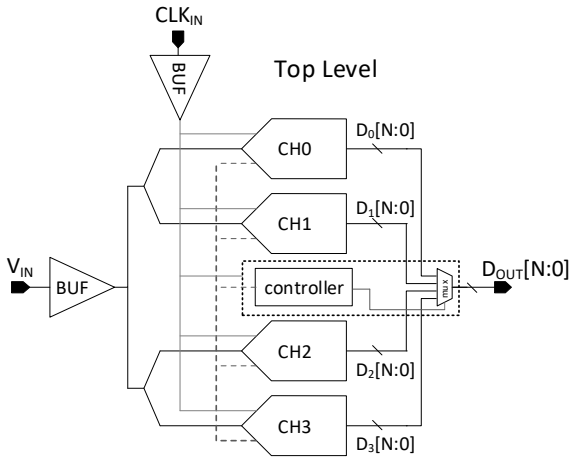
Closing the Gap

Industry SoTA

	Vaz ISSCC 2017	Devarajan ISSCC 2017	Straayer ISSCC 2016	Wu ISSCC 2016	Ali VLSI 2016
Architecture	Pipe-SAR	Pipeline	Pipeline	Pipeline	Pipeline
Sampling rate [Gsps]	4	10	4	4	5
Technology [nm]	16	28	65	16	28
ENOB Nyquist [bit]	9.2	8.8	8.9	9.0	9.3
SFDR Nyquist [dB]	67.0	64	64.0	68.0	70
Power [mW]	513	2900	2214	300	2300
FoM_{Walden} [fJ/c.step]	214	631	1130	145	709
$FoM_{Schreier}$ [dB]	153	147	145	154	148
Area [mm²]	1.04	20.2	11.0	0.34	14.4

R&D SoTA

Hershberg ISSCC 2019
Pipeline
3.2
16
10.0
73.3
61
19
166
0.194



Coming soon, to a product near you...

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