A 1MS/s to 1GS/s Ringamp-Based Pipelined ADC with Fully Dynamic Reference Regulation and Stochastic Scope-on-Chip Background Monitoring in 16nm

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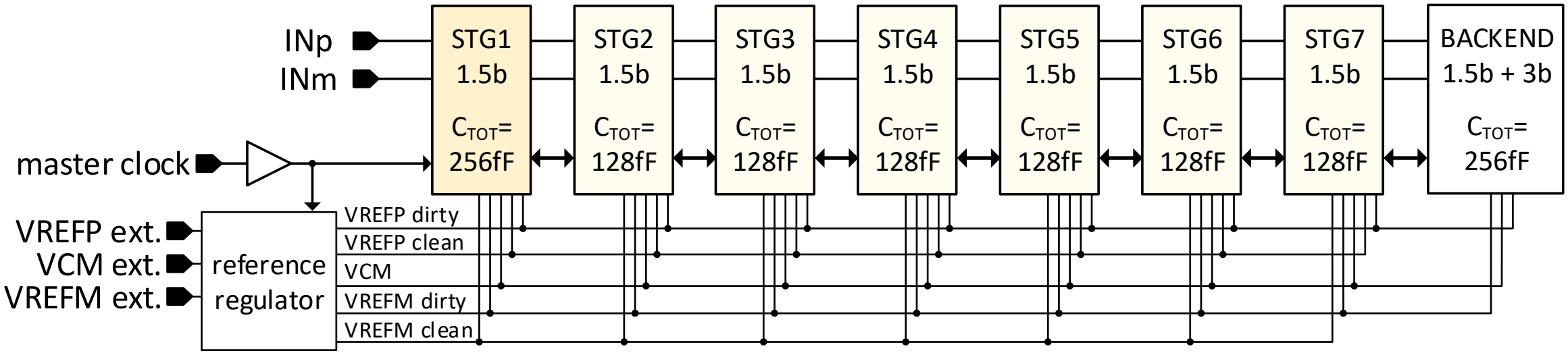
Architecture Overview



- **Ringamp "deep" pipeline based on:**
  [Hershberg, ISSCC 2019, Paper 3.6]
  [Hershberg, ISSCC 2019, Paper 3.1]
  - Fully Dynamic Power Consumption
  - Asynchronous event-driven timing control
  - MDAC with passive-hold mode in STG1
  - Early quantization in STG2-9

- **New in this work:**
  - Reference Regulation
  - Stochastic Scope-on-Chip
  - Ringamp Topology

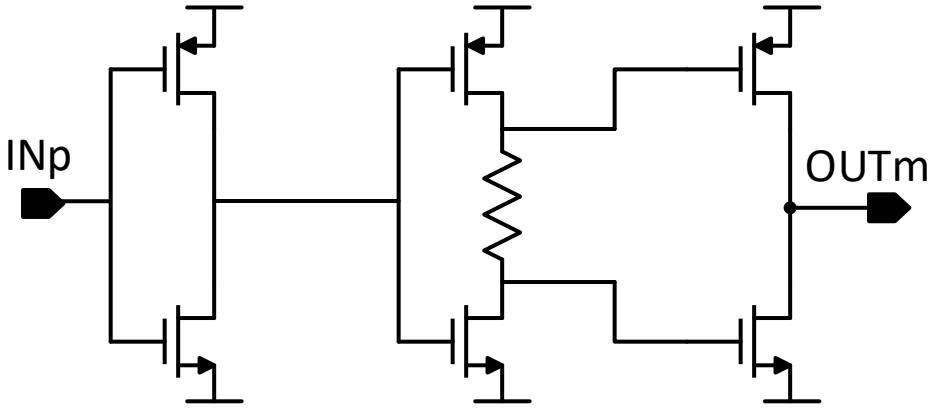
Outline

- Ringamp Topology
- Fully Dynamic Reference Regulation
- Scope-on-Chip Amplifier Settling Monitor
- Performance Summary & Conclusion

Ringamp Topology

- What is a ringamp?
  - Multi-stage amplifier
  - Dominant output pole
  - Dynamic stabilization

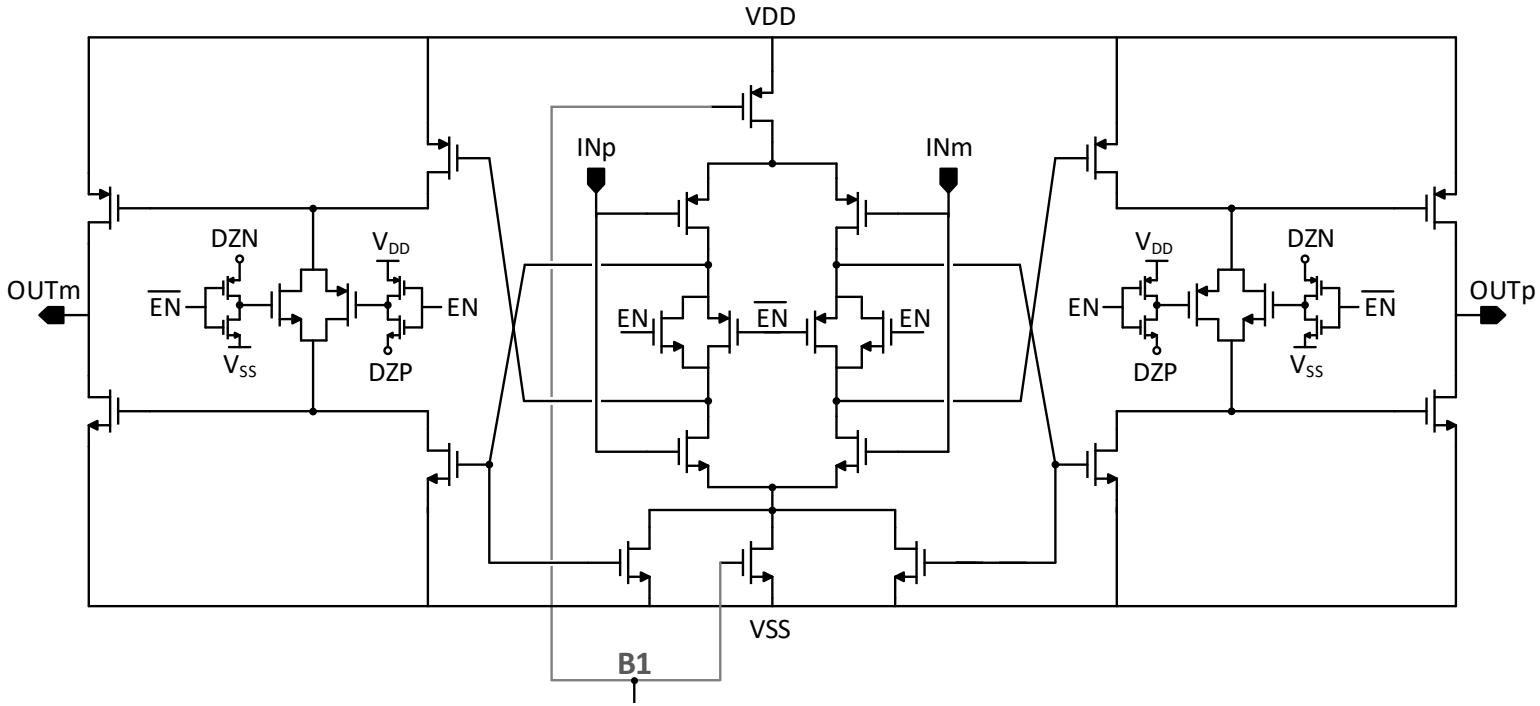
☺ High efficiency
☺ High linearity
☺ High speed
☺ Wide output swing
☺ Fully dynamic (switchable)
☺ Scales with Digital



[Hershberg, JSSC 2012]

Ringamp Topology

- Fully-Differential
- Multi-Path CMFB
- Trapped-Charge Biasing
- CMOS-Resistor
- Bias-Enhanced
- Self-Resetting
- Slew-Done Detector



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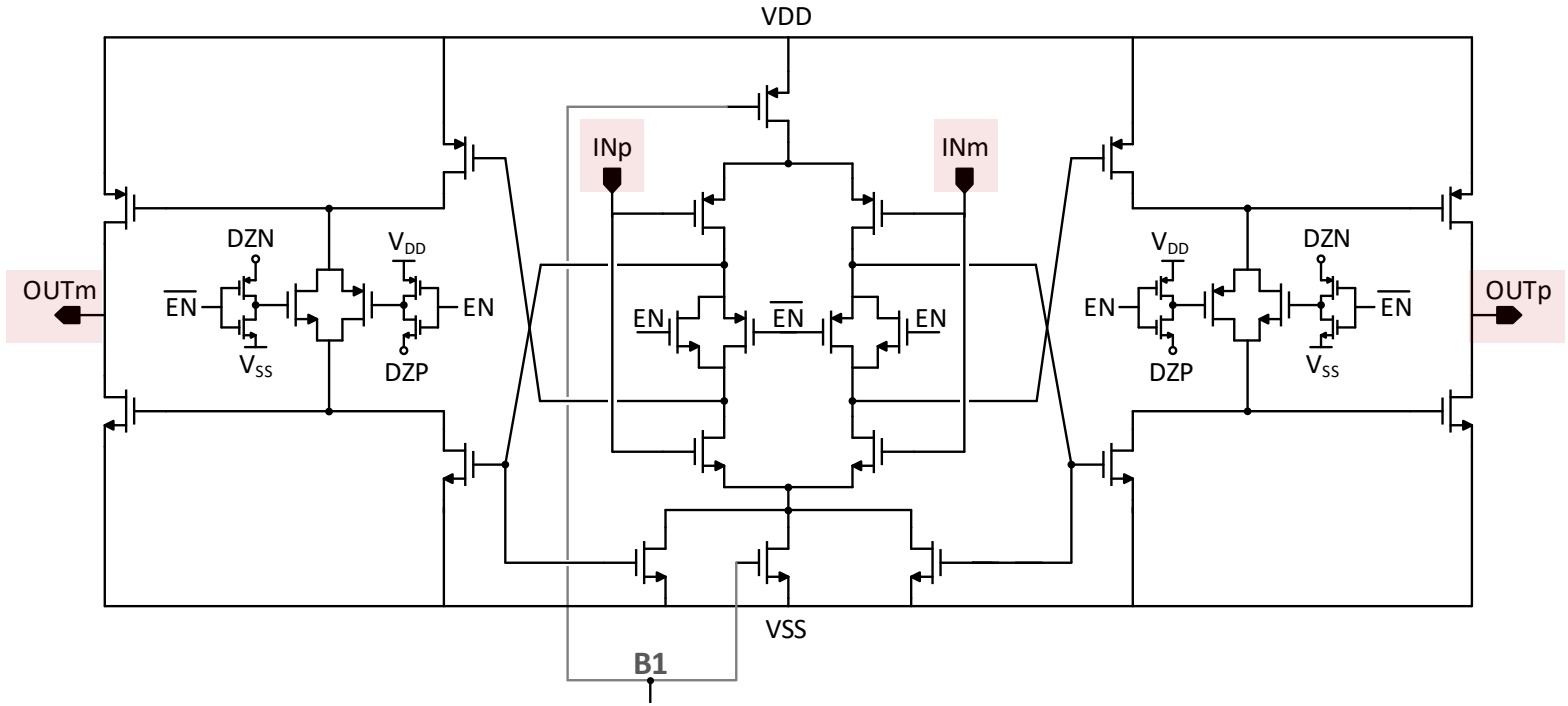

[Lim, JSSC Dec. 2015]

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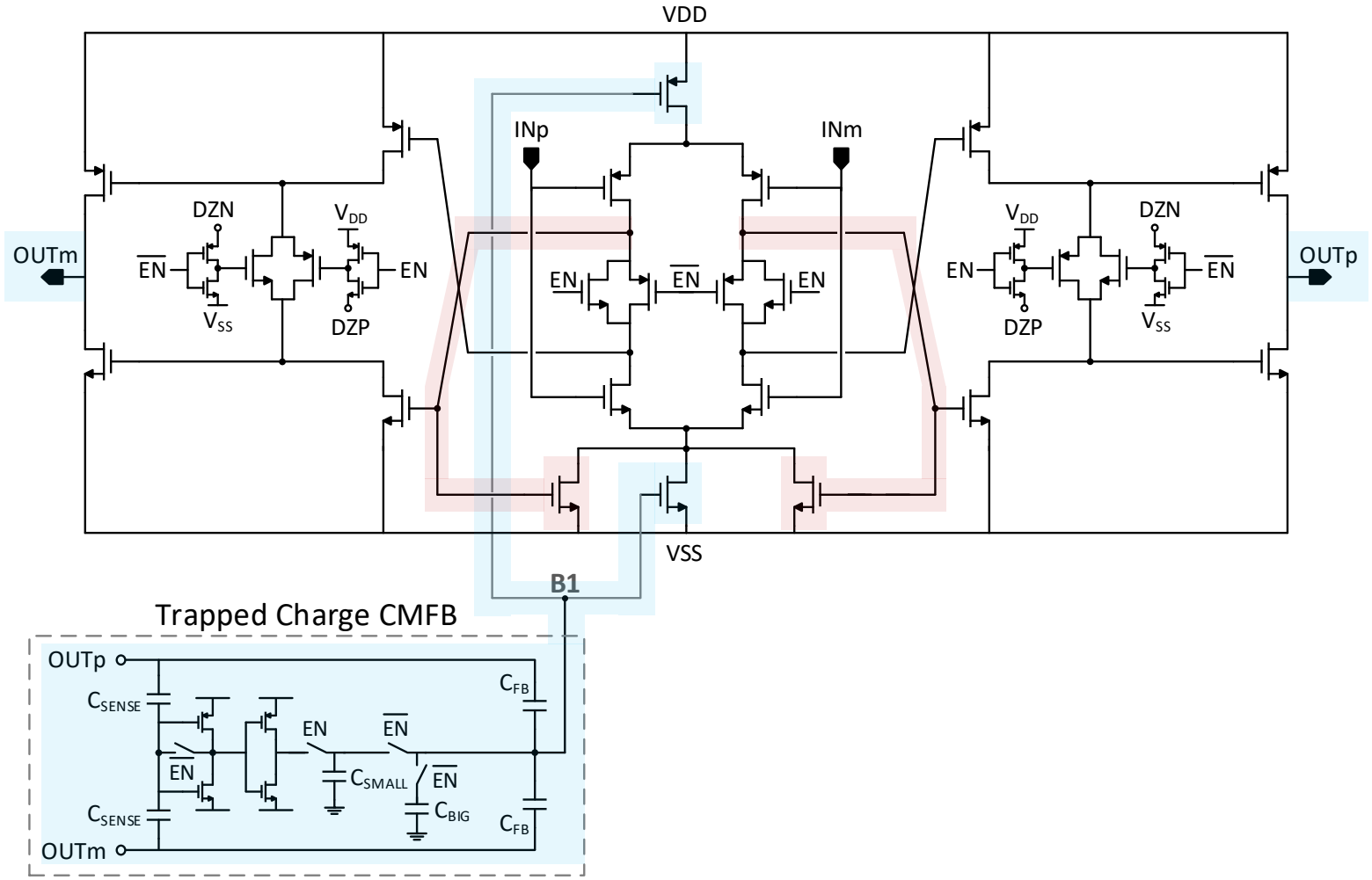
(Paper 3.1)



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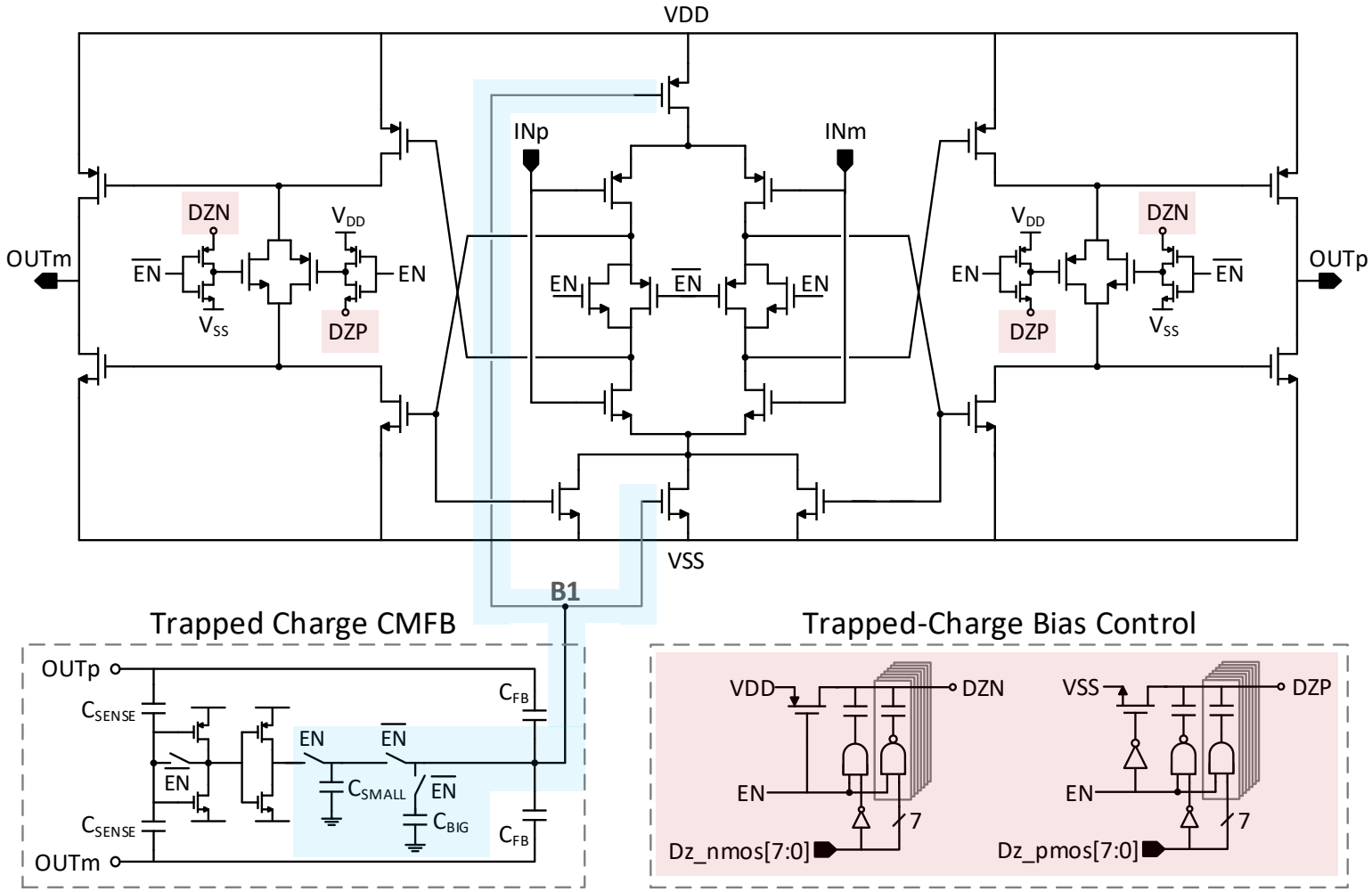
[Hershberg, ISSCC 2019] (Paper 3.1)



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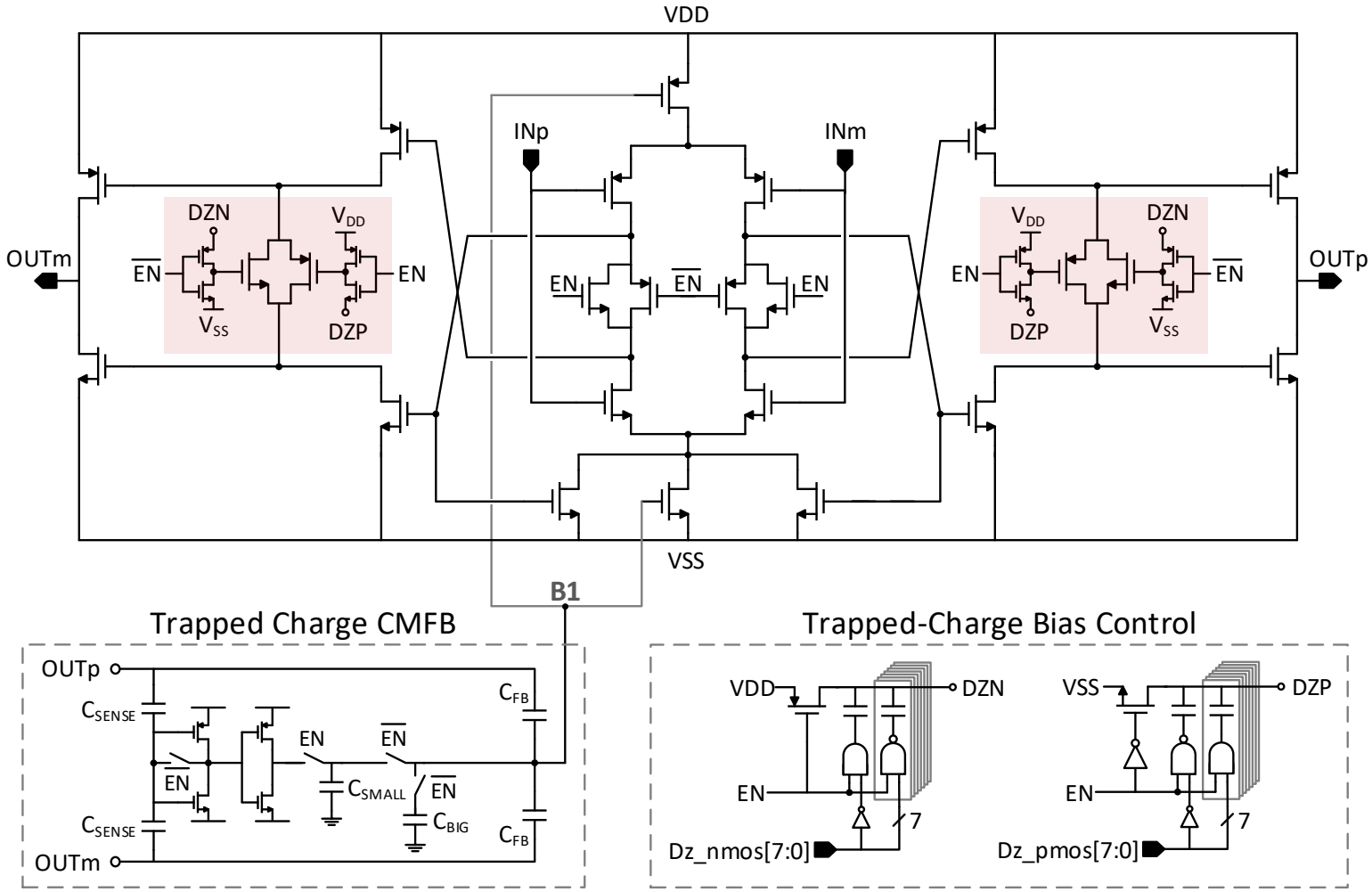
[Lagos, JSSC Feb. 2019]



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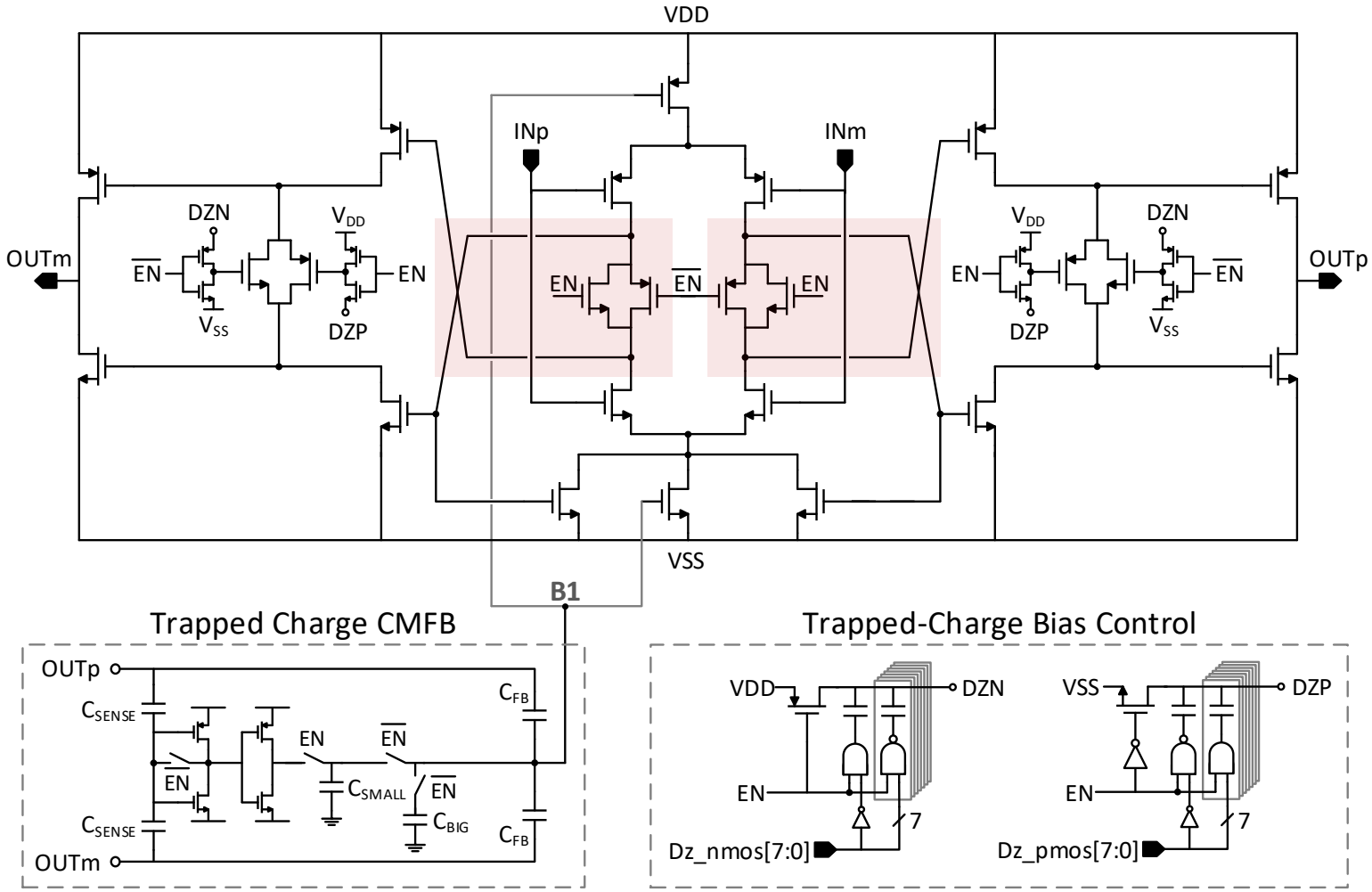
[Chen, TCASII 2018]
[Lagos, JSSC Mar. 2019]



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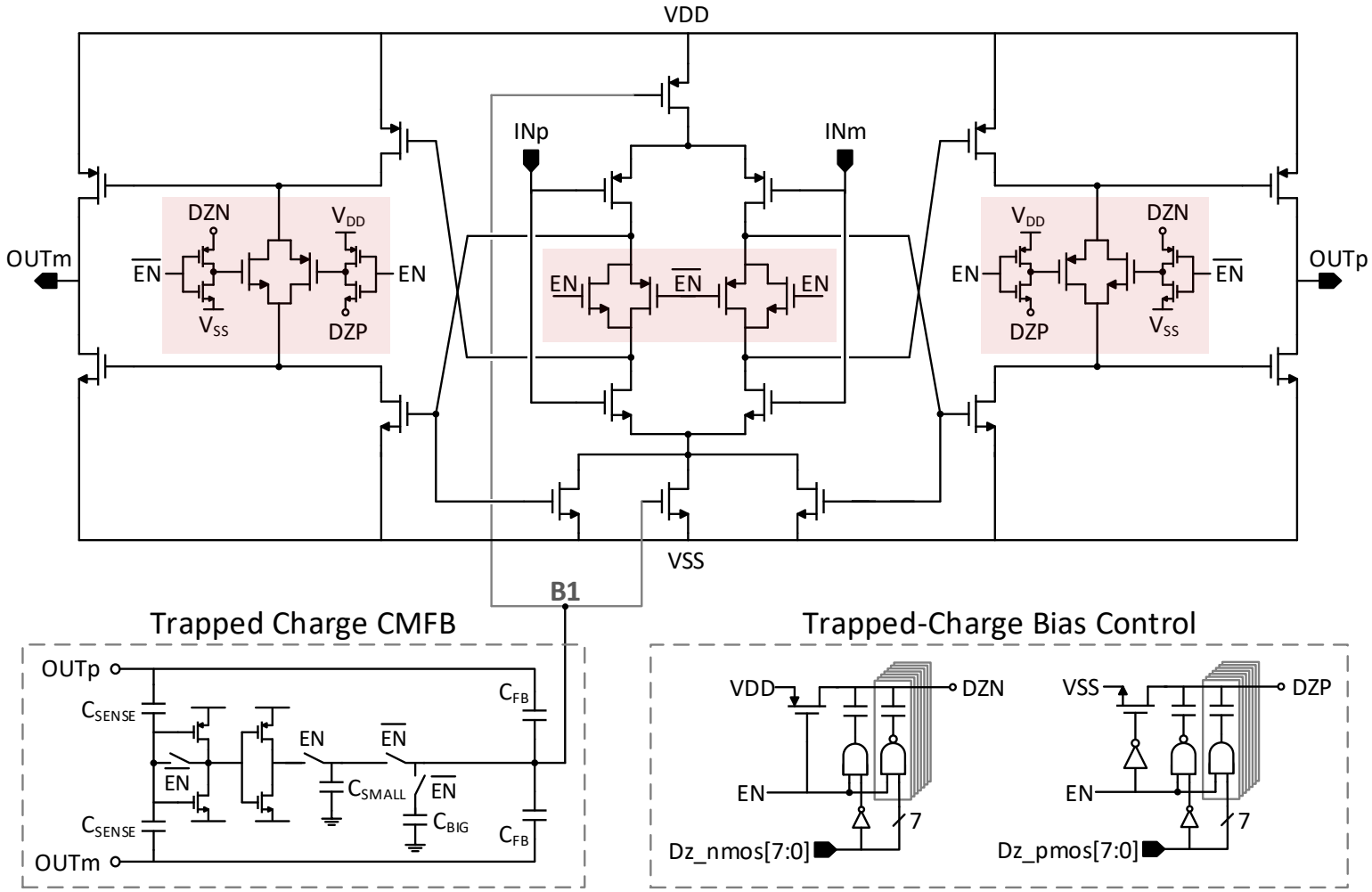

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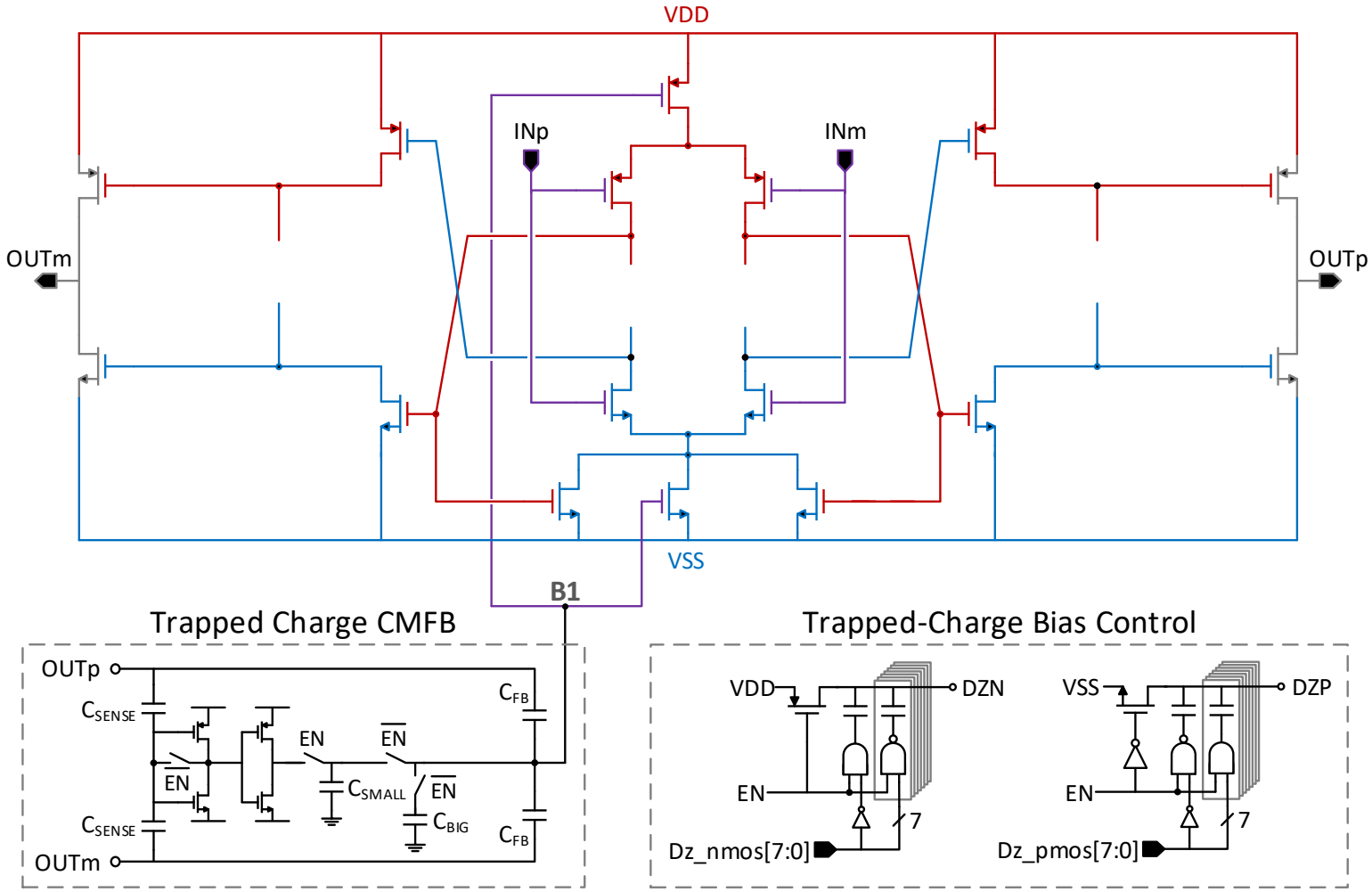

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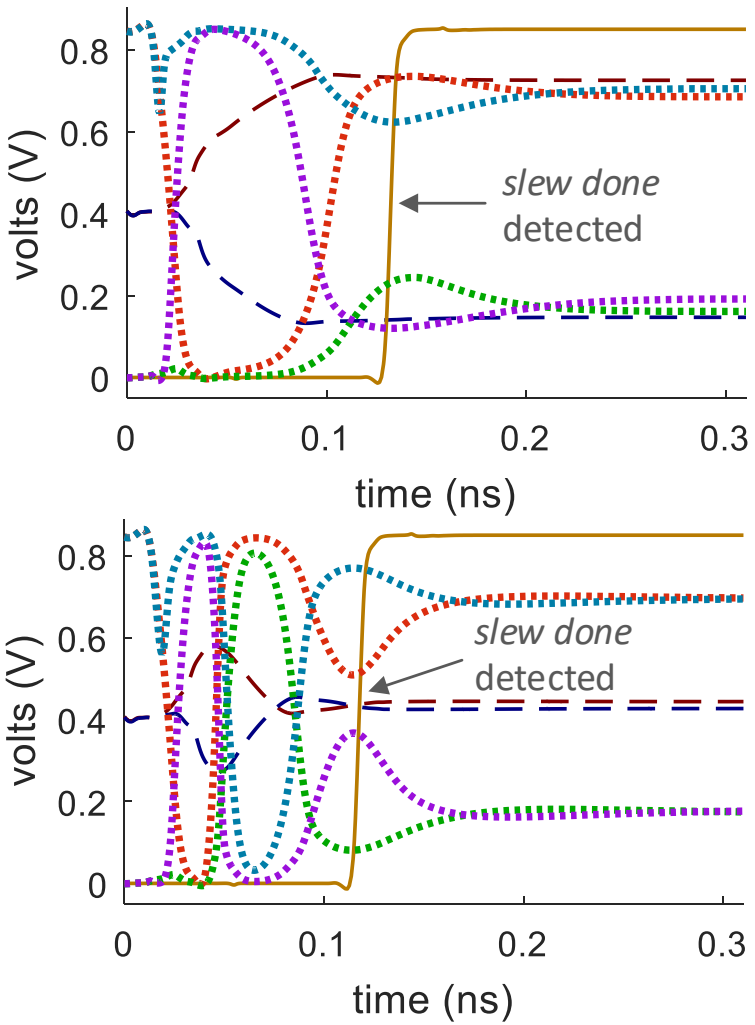
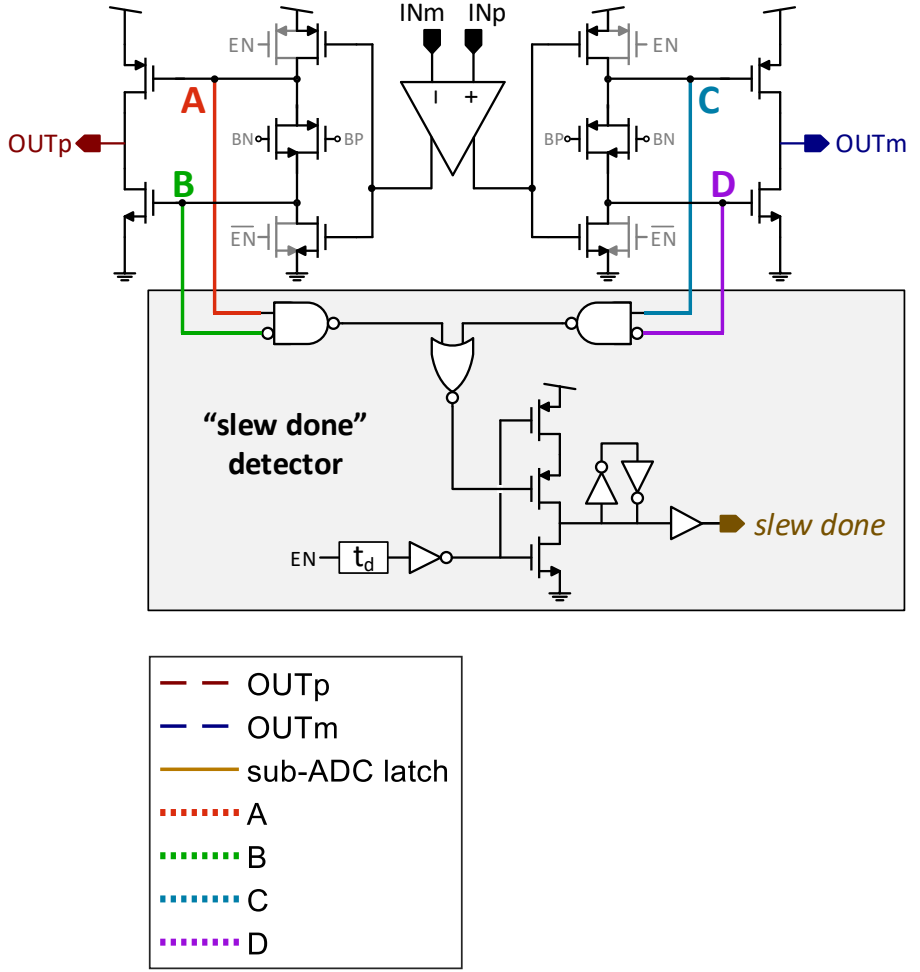
[Hershberg, ISSCC 2019] (Paper 3.6)





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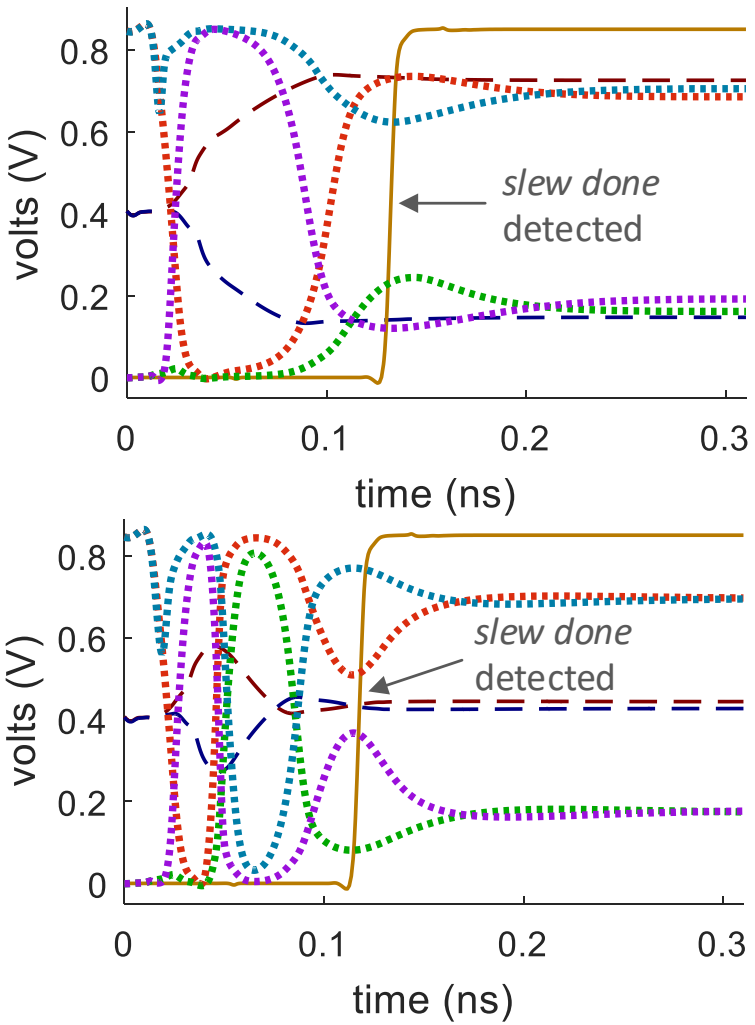

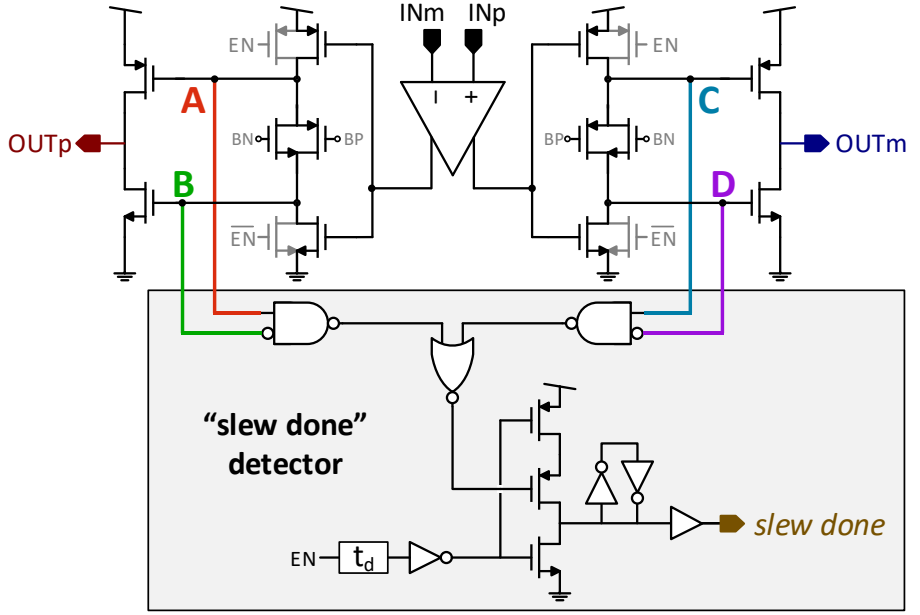

Not Mandatory
Using a fixed time-delay to generate *slew done* also ok.

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Fully Dynamic Reference Regulation

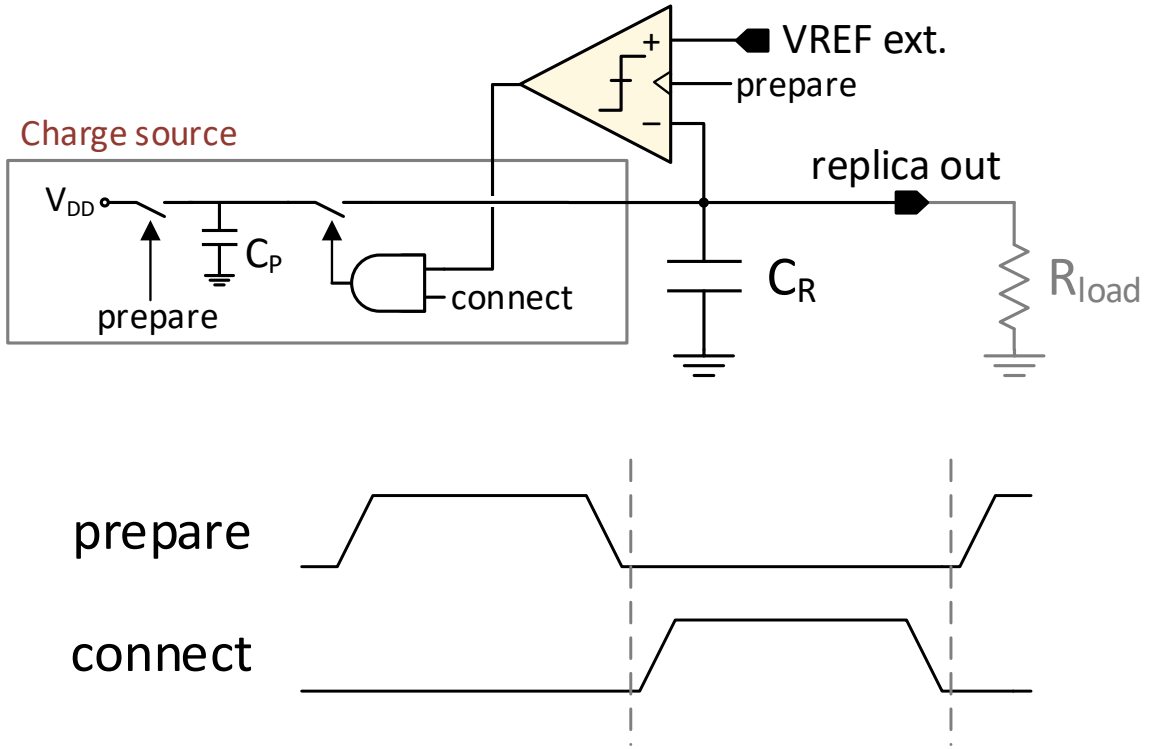
- **Goal:** fully dynamic power for complete system (core + reference)
  - Constant FoM for any clock rate
  - Enables reconfigurable, multi-standard ADCs

- ADC core fully dynamic by design ✓ *[Hershberg, ISSCC 2019, Paper 3.6]*
  - Enabler: Asynchronous timing control
  - Enabler: Ring amplifier with fast on/off switching

- Reference Regulation
  - How can we make this fully dynamic too?

Fully Dynamic Reference Regulation

- Discrete Time Regulator Loop
  - Comparator monitors replica level
  - Feeds back "charge packet" (C_P) update into charge reservoir (C_R)



[Kull, JSSC 2013]

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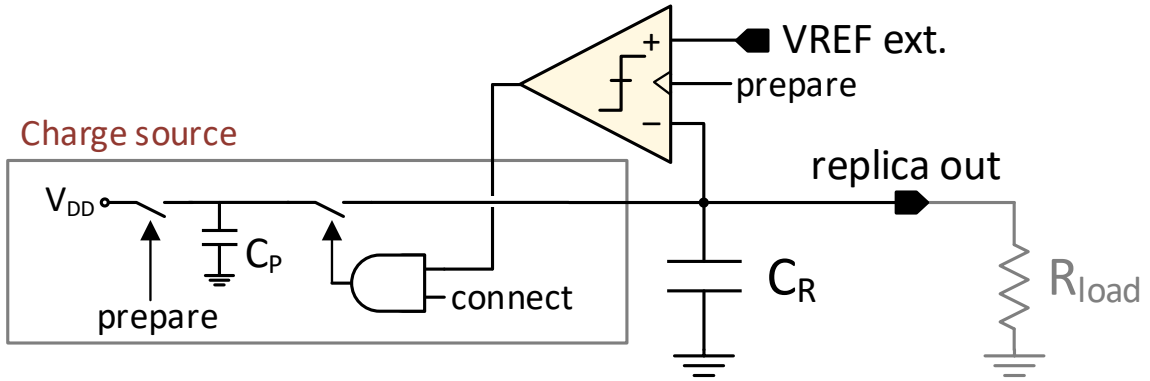
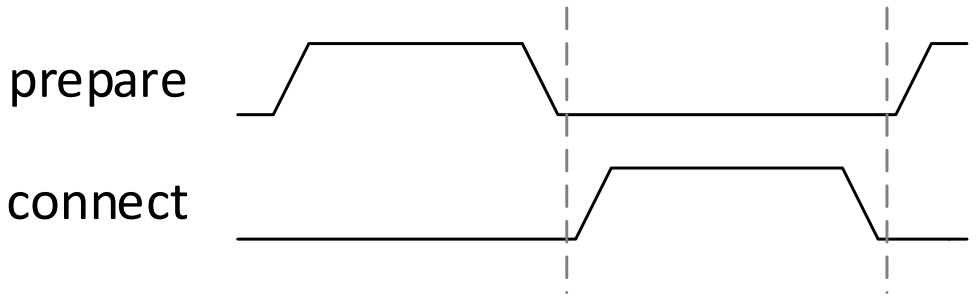


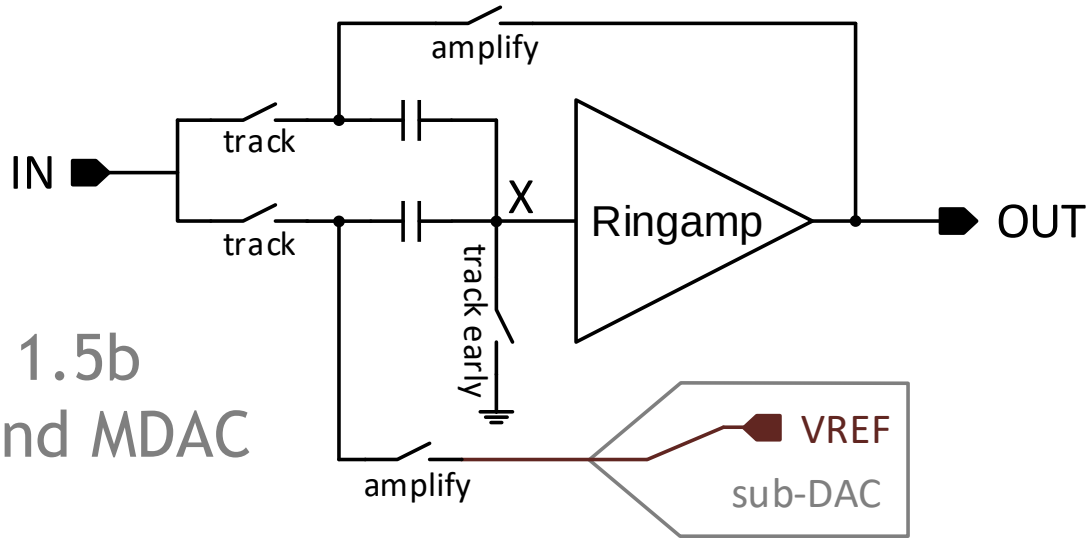
- Limitations
  - Must source all charge for an ADC conversion in a single charge packet
  - Reference ripple error a problem
  - Acceptable for ADCs < 8 bit
  - C_R too large for ADCs > 8 bit (> 1nF)



[Kull, JSSC 2013]

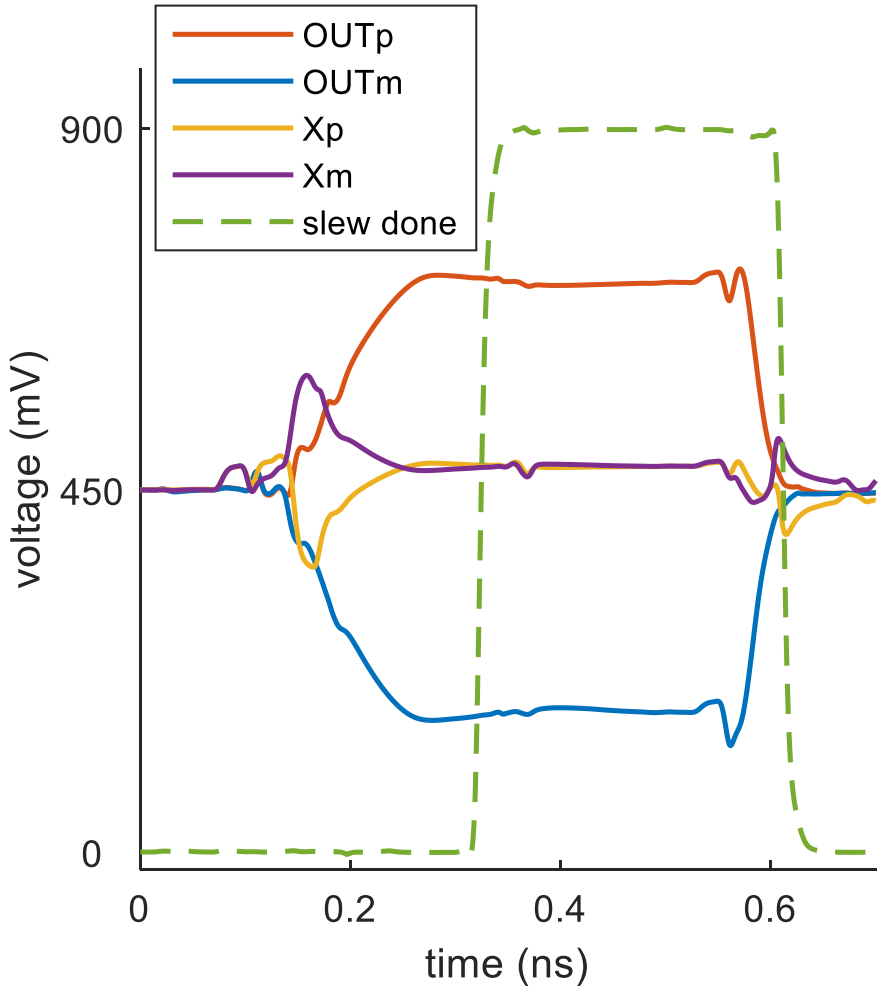
Proposed: Split-Reference Regulation

- **Key observation:** V_{REF} accuracy & current requirements are decoupled w.r.t. time
  - Initial: large current, low accuracy
  - Final: small current, high accuracy



Example 1.5b flip-around MDAC

Example Settling Waveform



Proposed: Split-Reference Regulation

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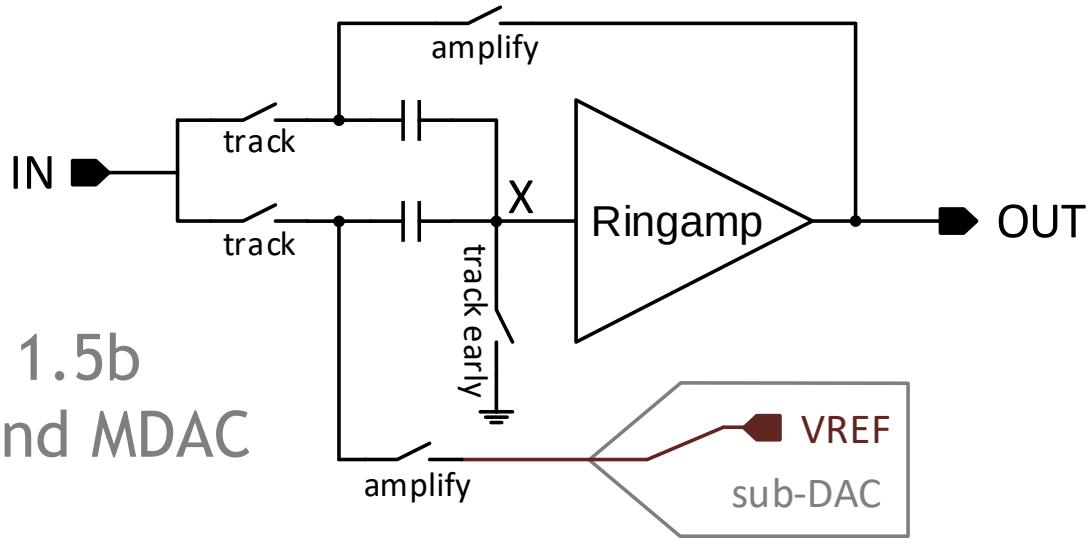
  - Final: small current (2%), high accuracy



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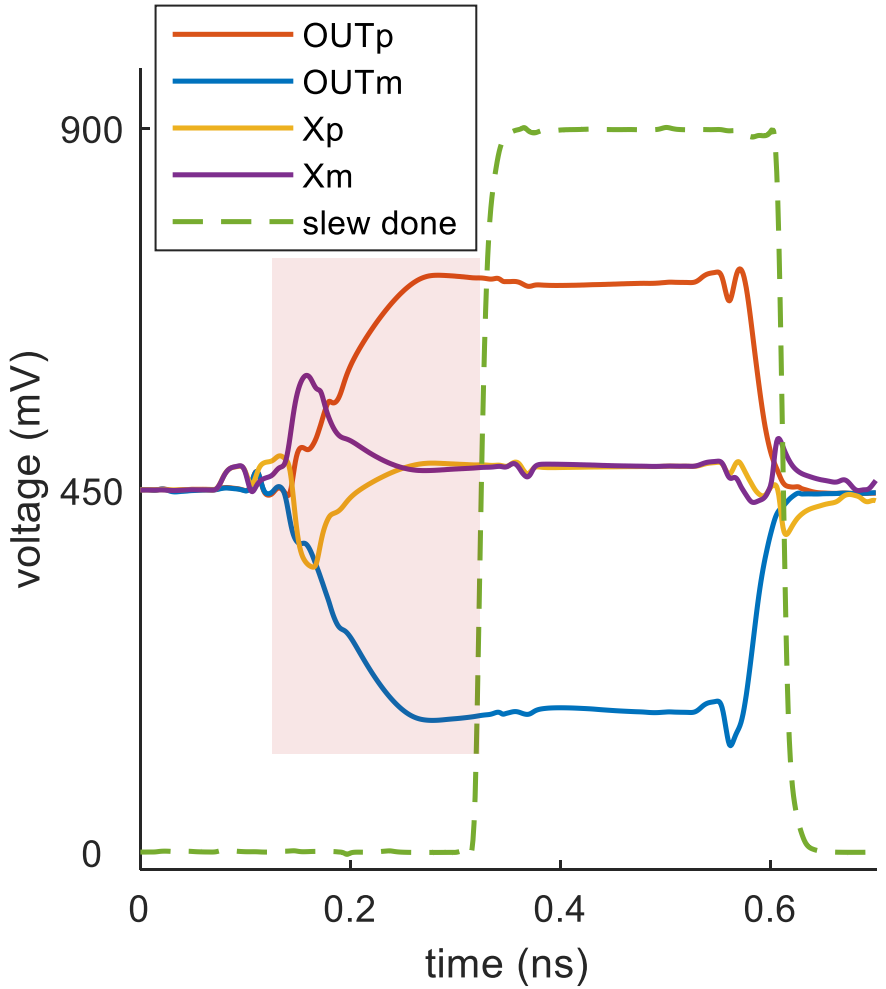

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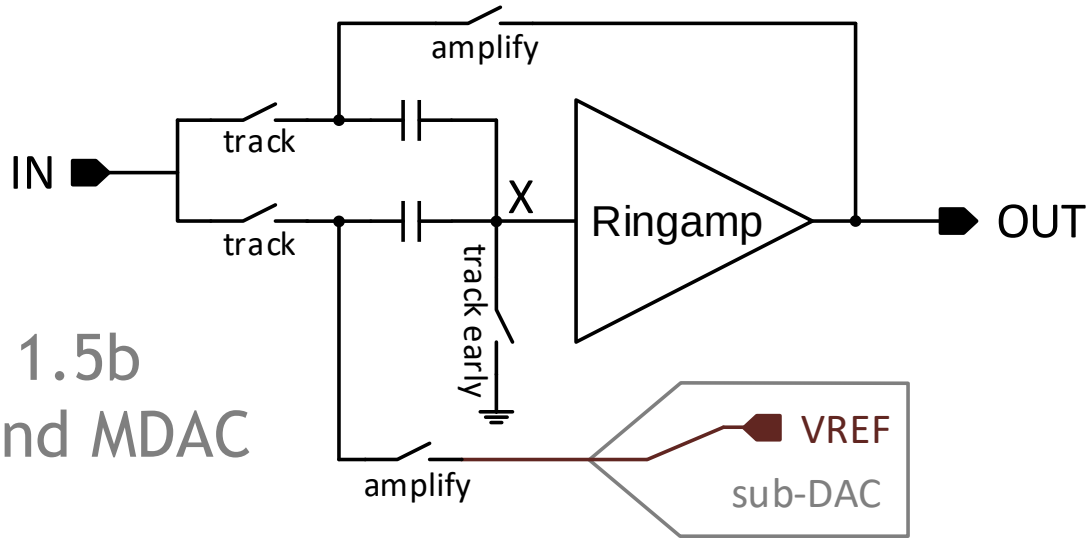

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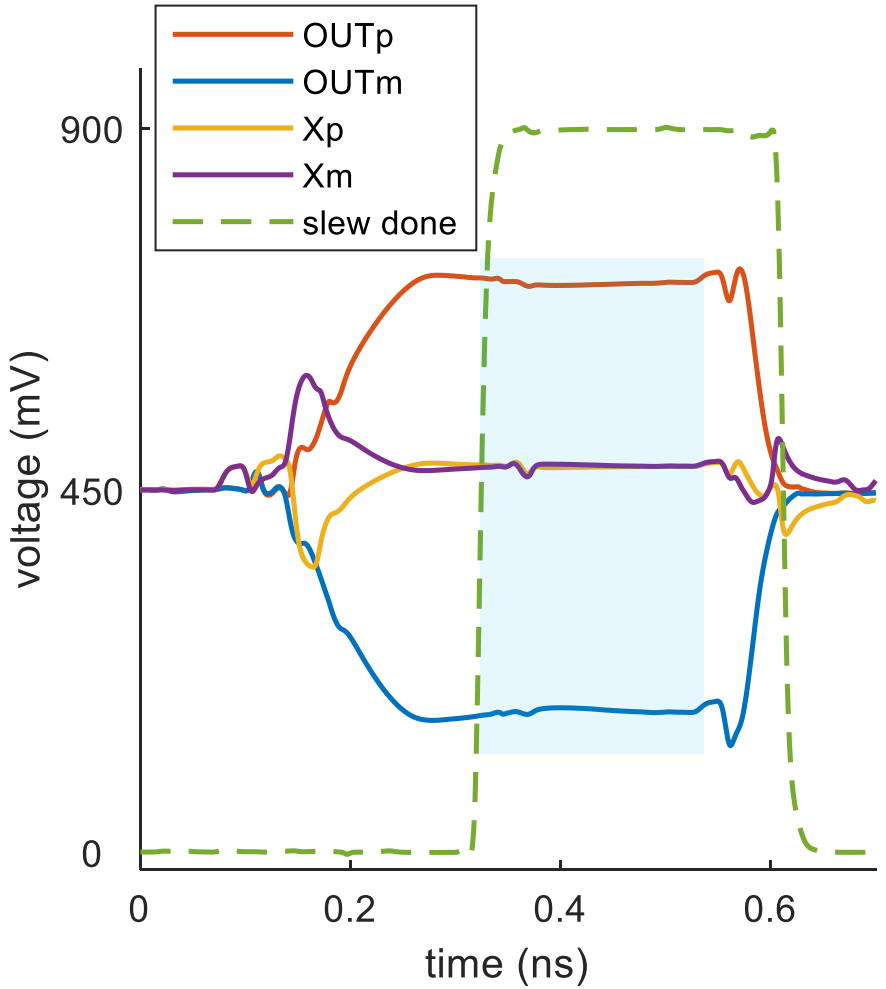

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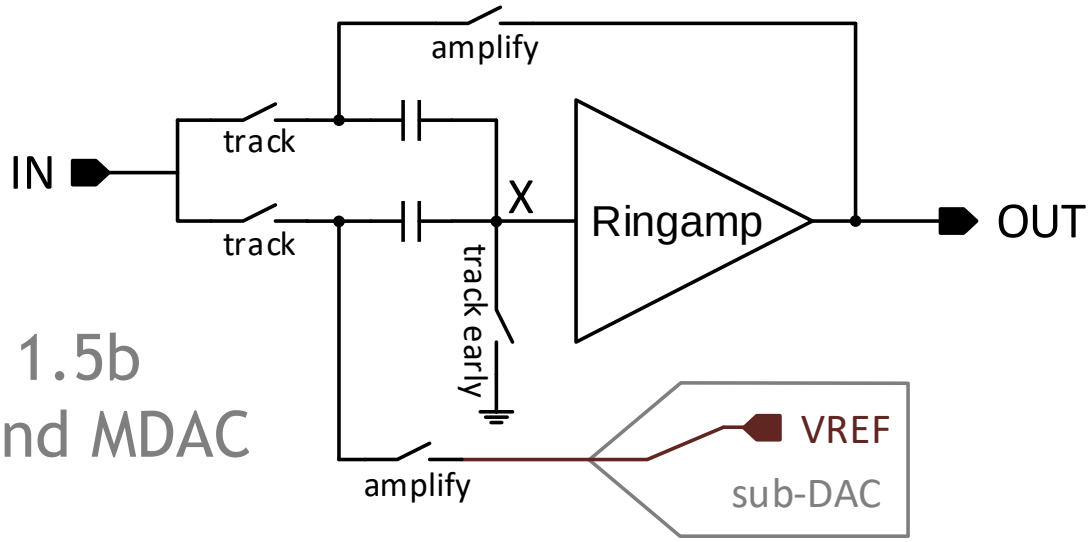
True for many applications

- Residue Amplifiers (Slew->Settle)
- SAR DACs (MSB->LSB)



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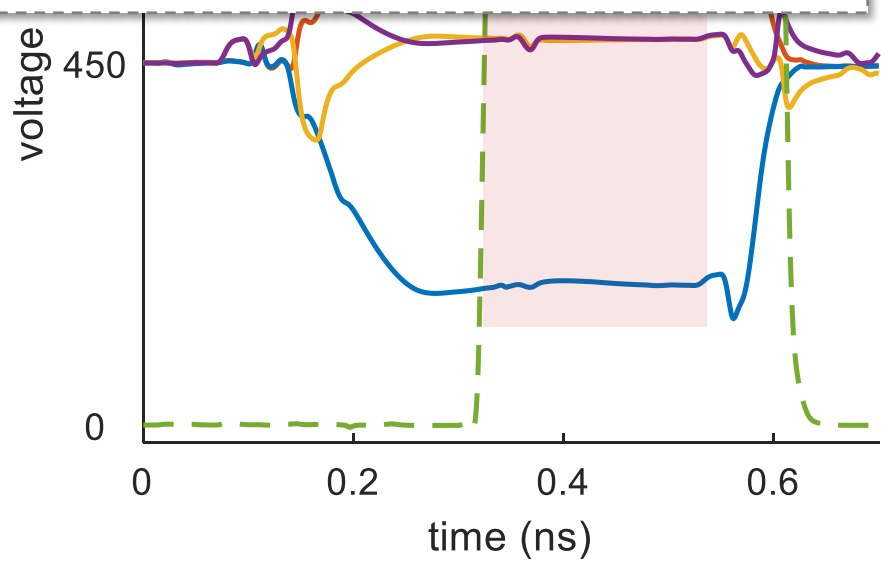
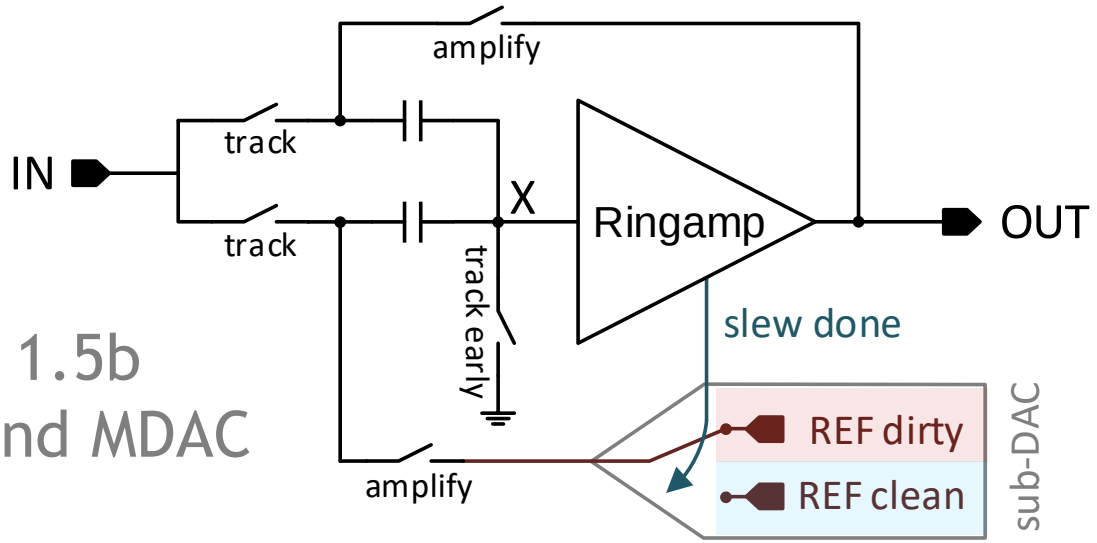


Proposed: Split-Reference Regulation

- **Solution: Use 2 copies of V_{REF}**
  - V_{REF} dirty: low-impedance, low-accuracy
  - V_{REF} clean: high-impedance, high-accuracy
- Relaxes requirements of both copies



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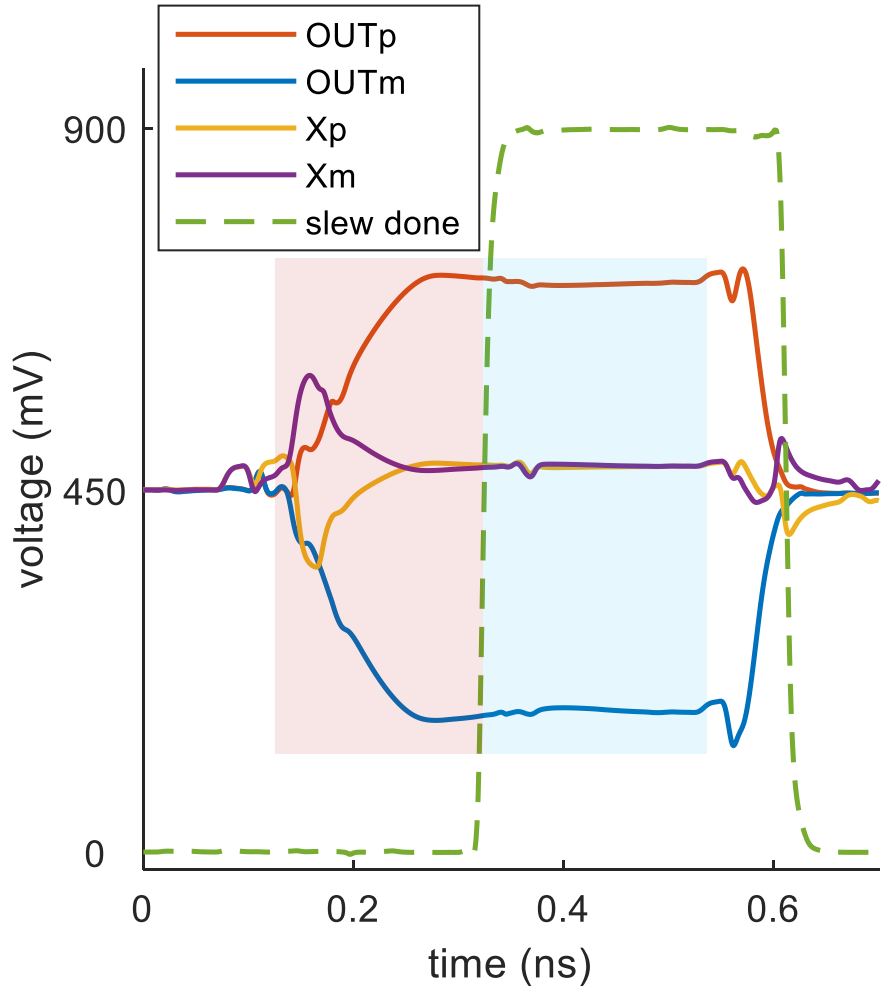
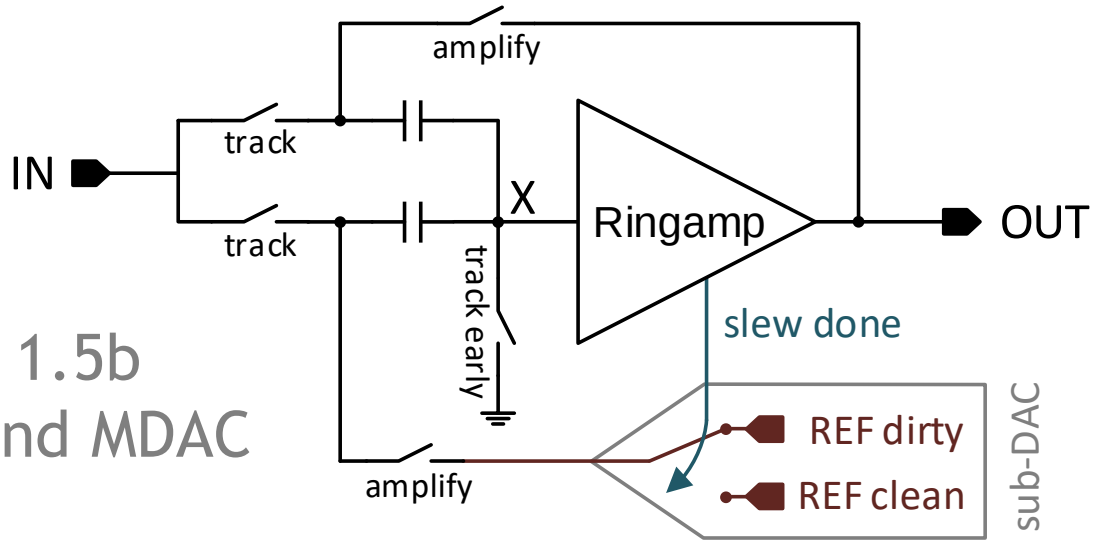


Switching from Dirty to Clean Reference

- Need break-before-make
  - Must isolate clean from dirty



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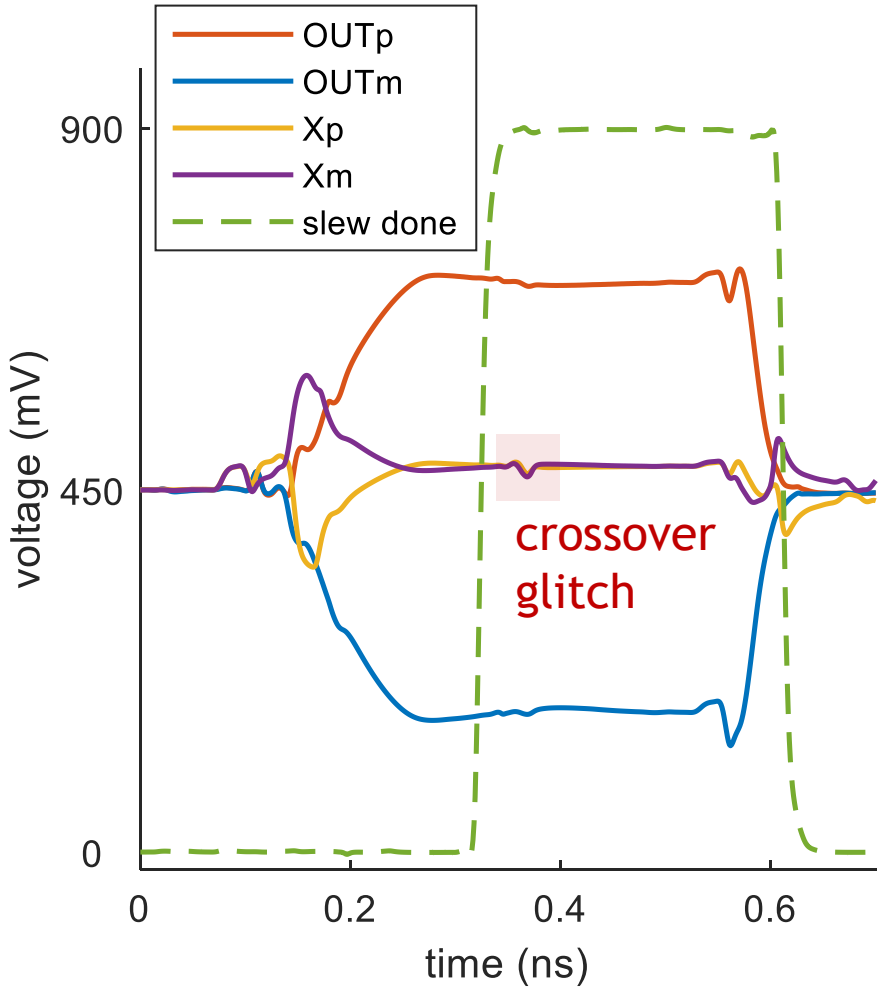
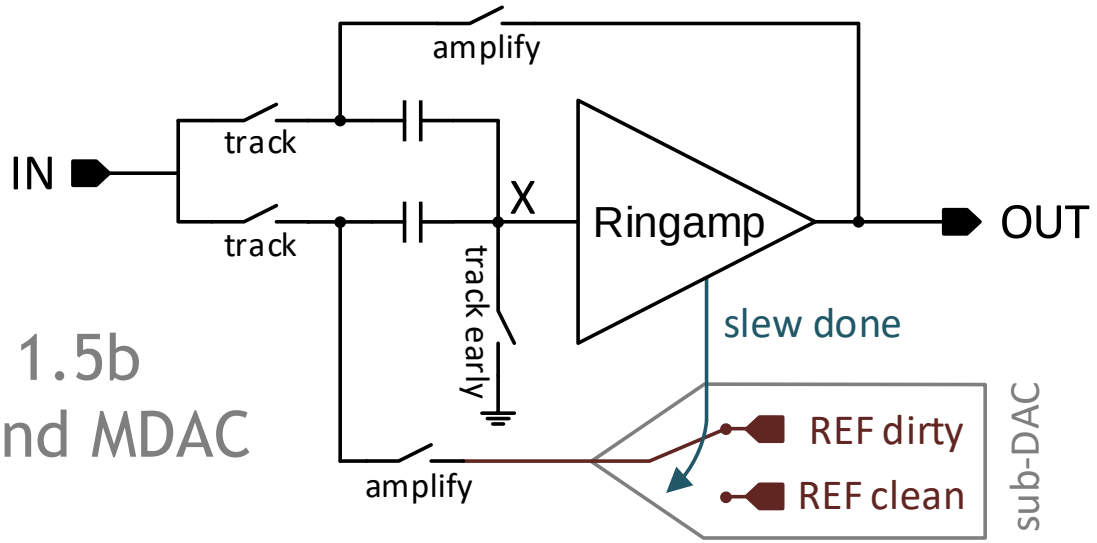


Switching from Dirty to Clean Reference

- Need break-before-make
  - Must isolate clean from dirty
- Want fast & clean crossover
  - Amplifier feedback is “paused”, time lost
  - Any injected errors must be re-settled



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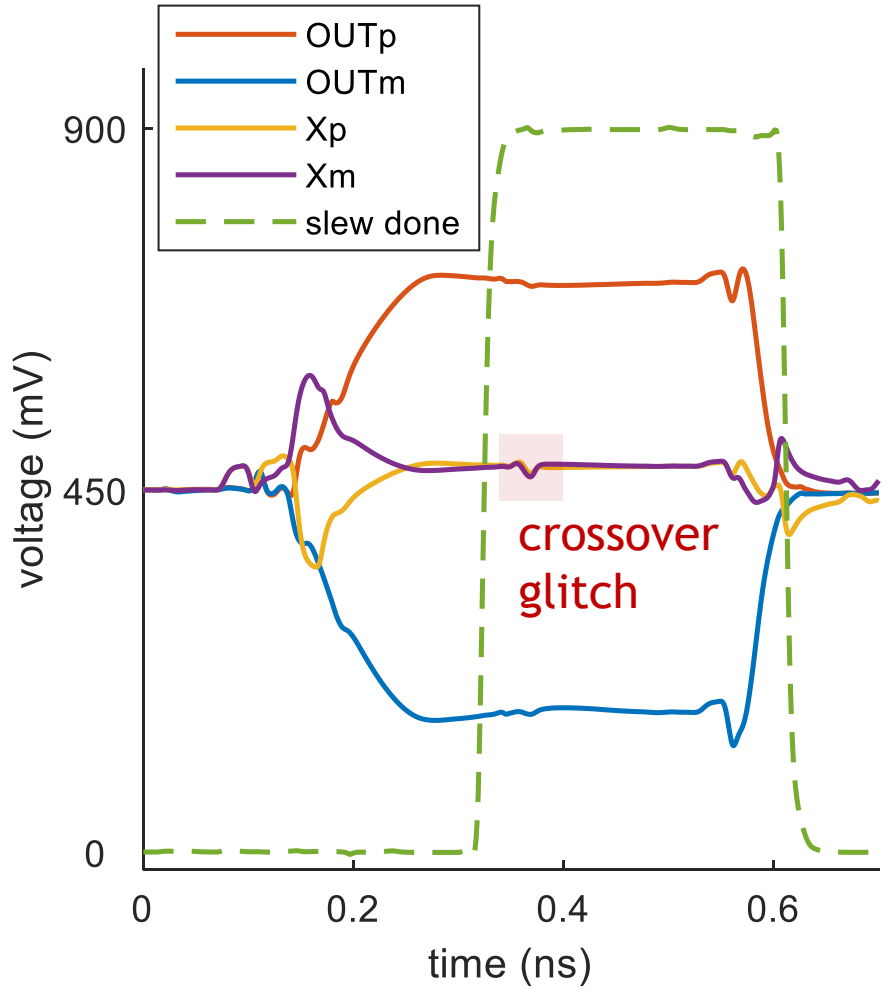
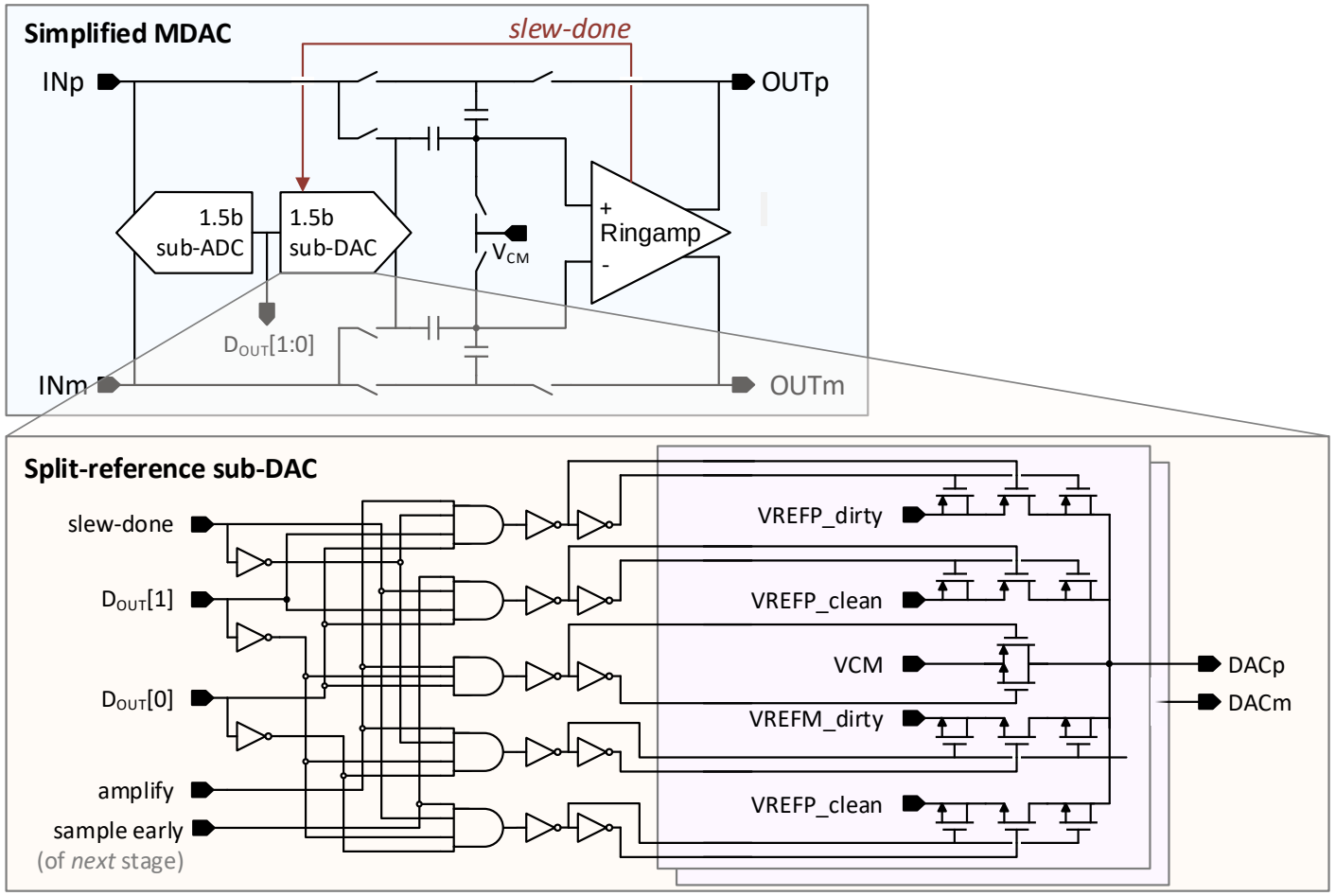


Sub-DAC Design Details

- Optimized control logic
  - Non-overlap
  - Fast crossover (< 30ps)
  - No corruption of *REF_clean*
- Dummy switches to cancel clock feedthrough & charge injection
- Minimal impact on settling performance ✓



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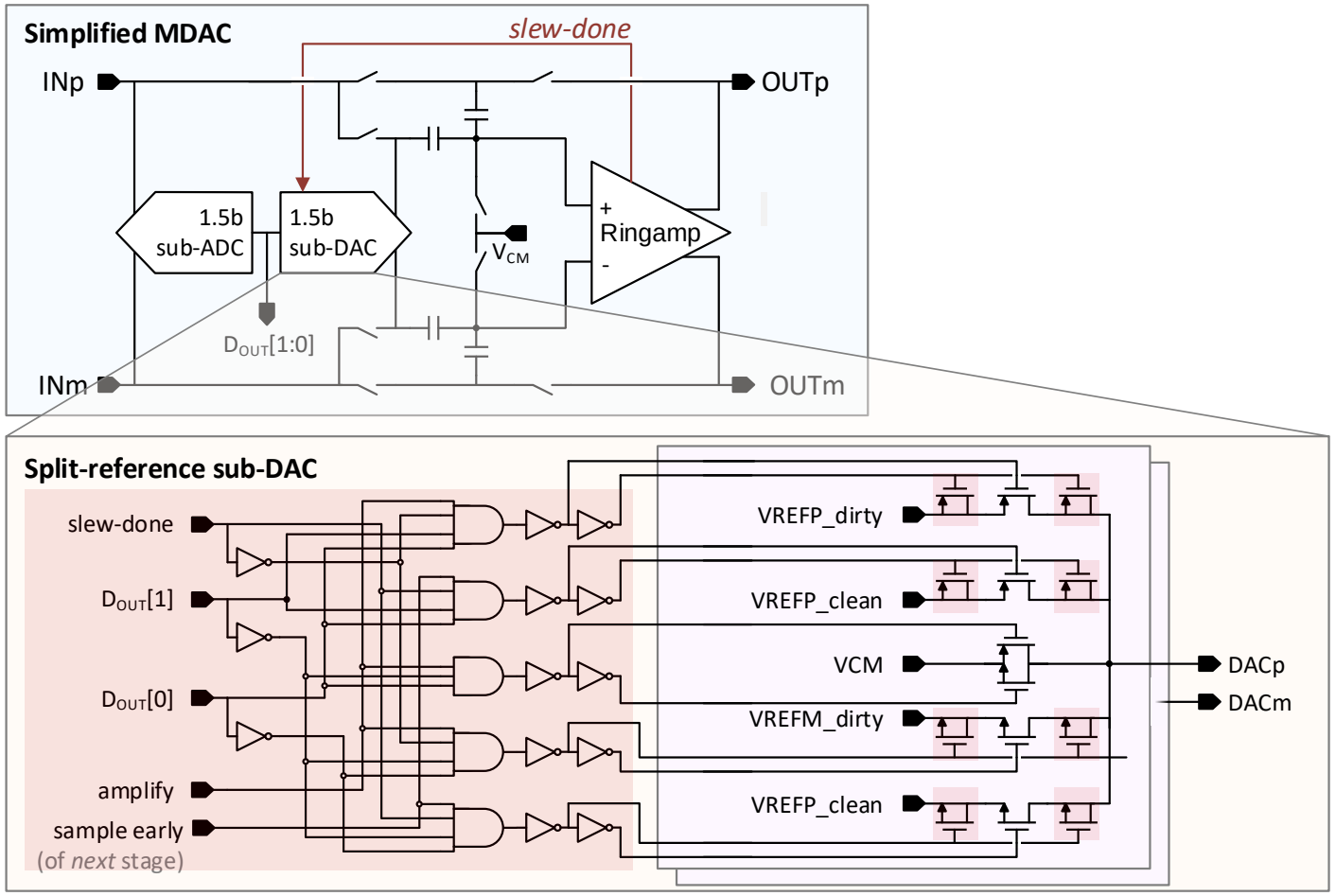

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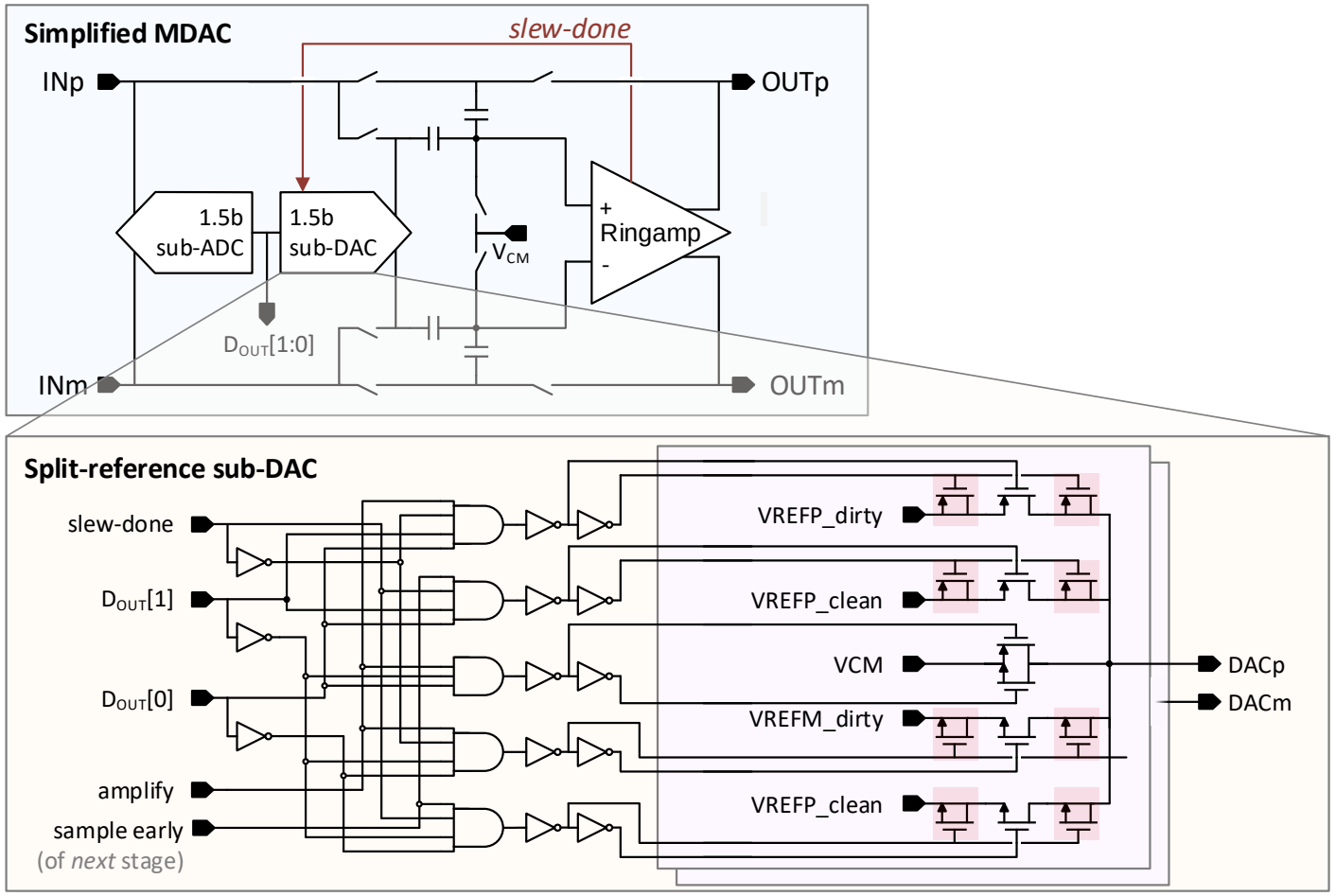
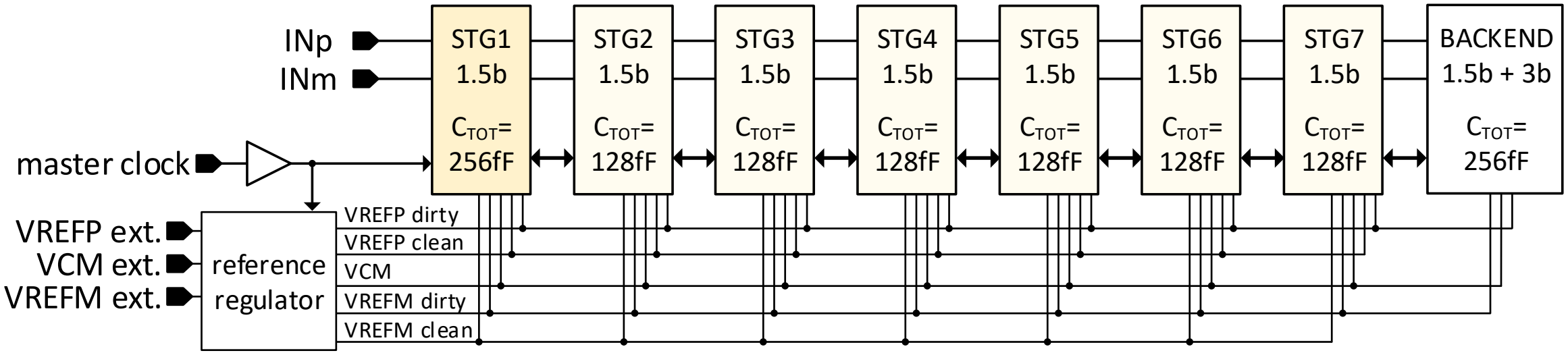


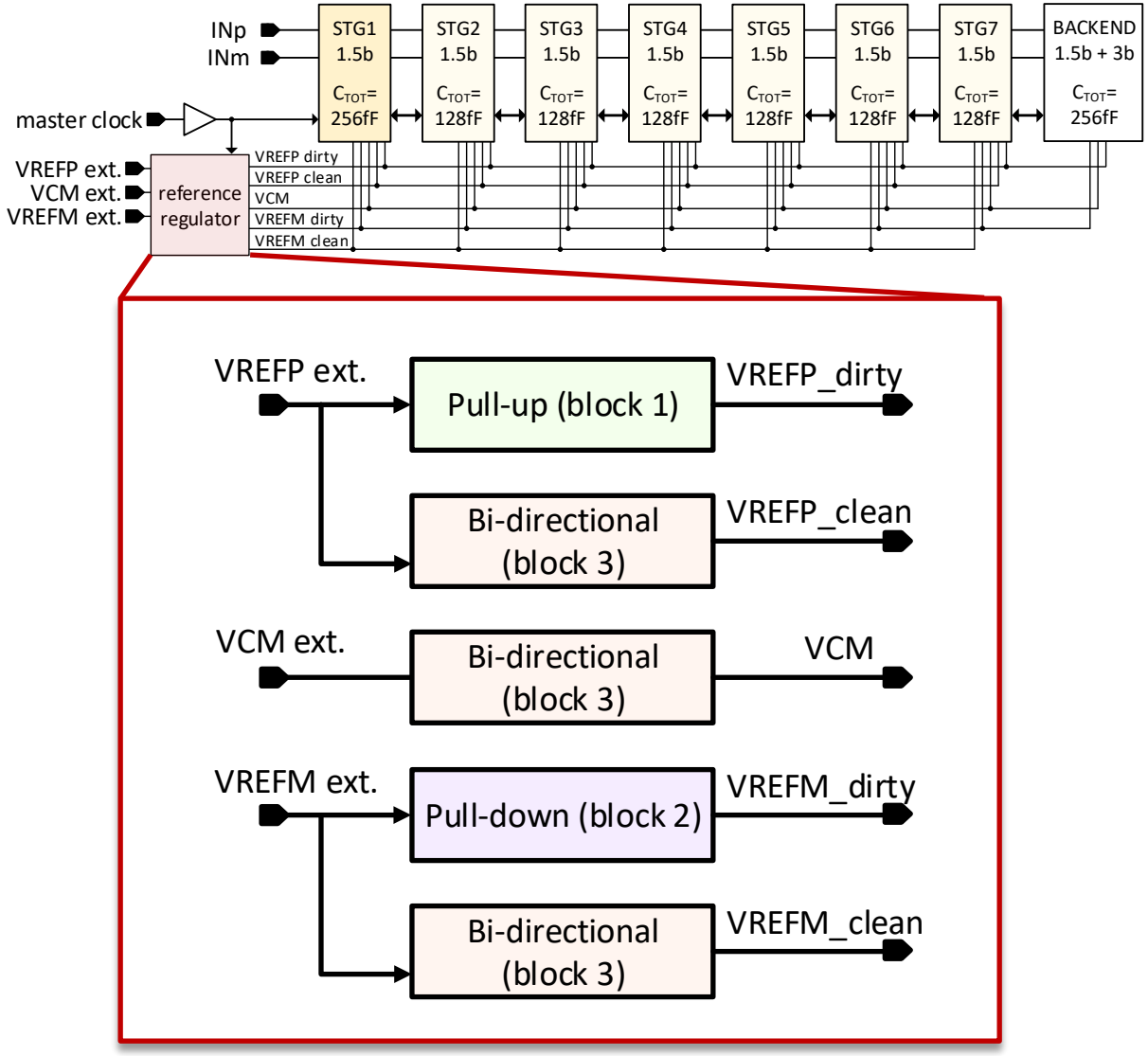
Reference Generation



- Single set of regulated references shared by all stages
  - Regulators only update once per cycle

Global Reference Generation

- Standard Pipeline
  - VREFP
  - VCM
  - VREFM
- Here: 5 discrete-time loops
  - VREFP dirty
  - VREFP clean
  - VCM
  - VREFM dirty
  - VREFM clean



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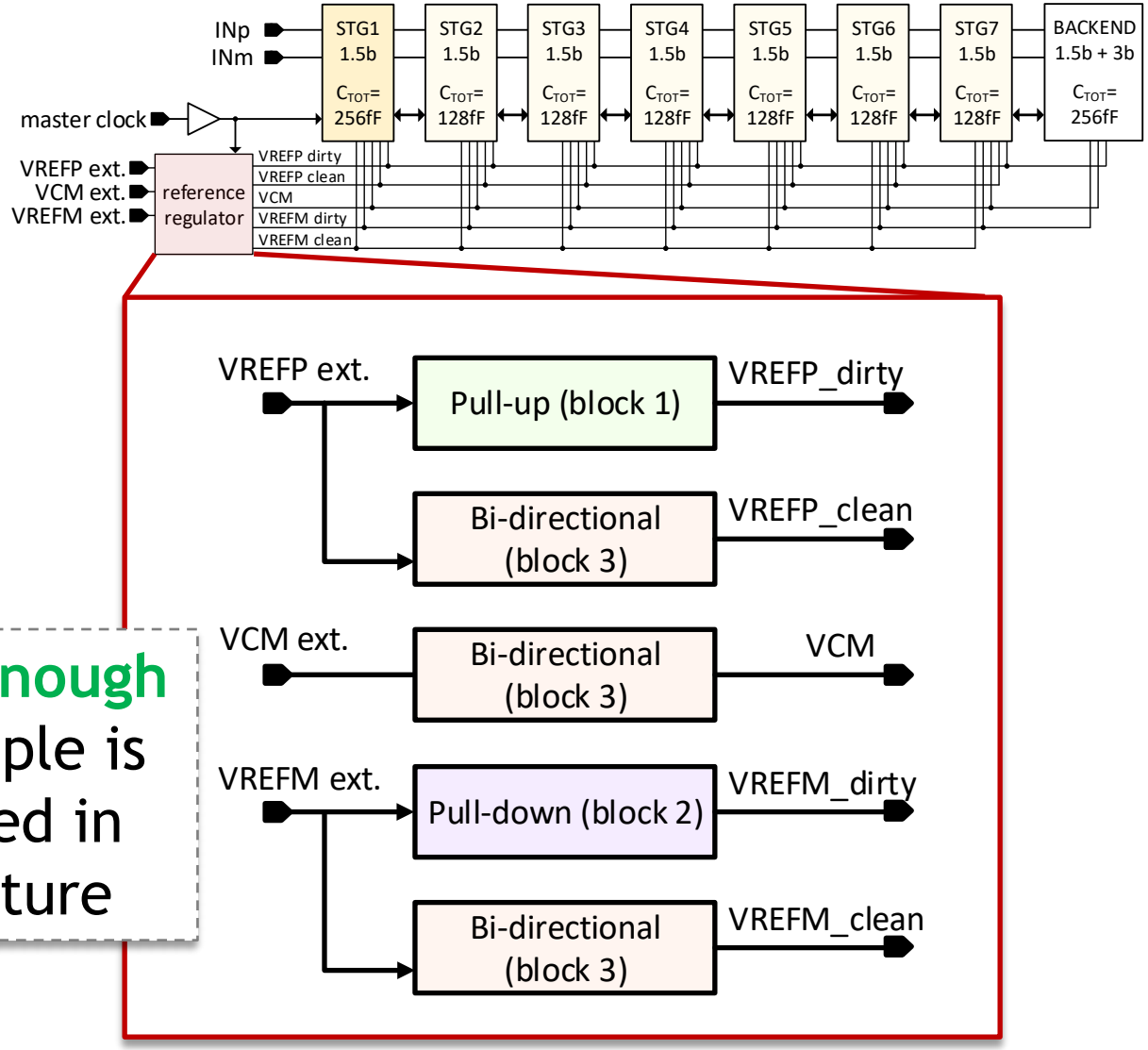
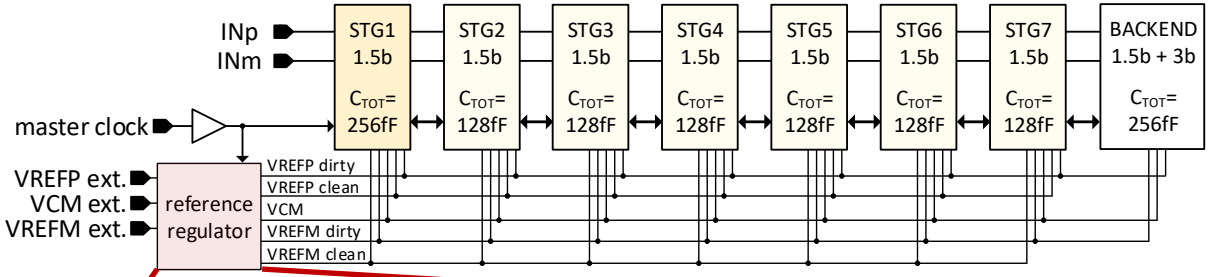
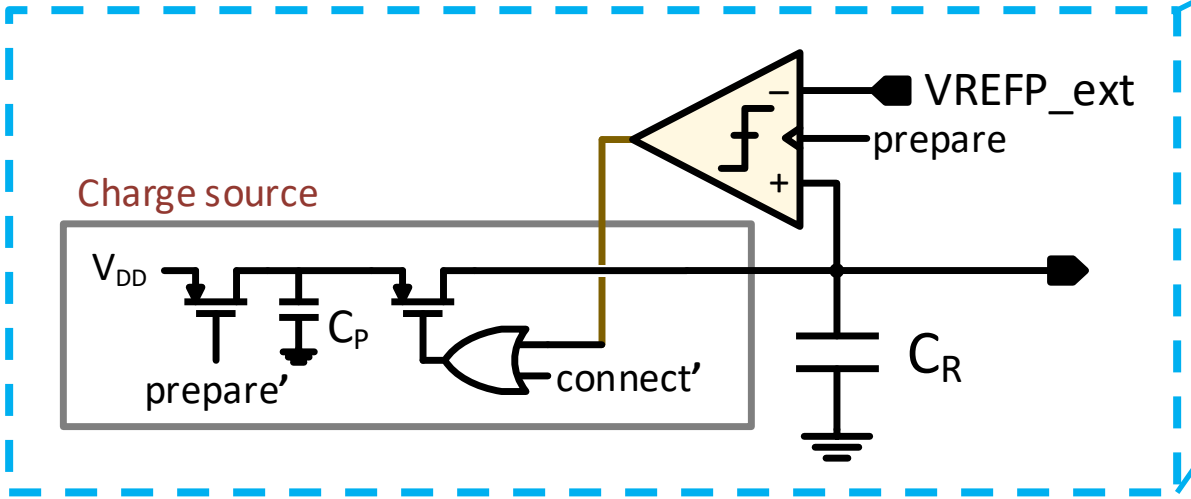
1 “Dirty” VCM is enough
Common-mode ripple is inherently rejected in differential structure

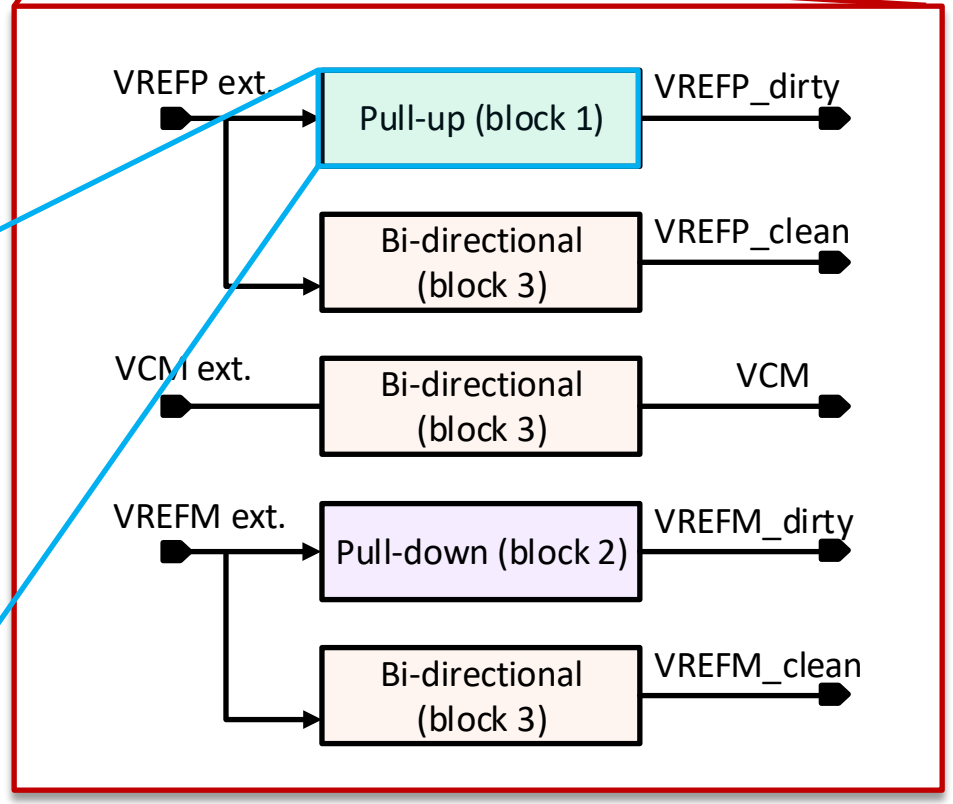


Global Reference Generation

- Uni-directional feedback for dirty references
  - MDAC always sinks charge from VREFP dirty
  - MDAC always sources charge to VREFM dirty







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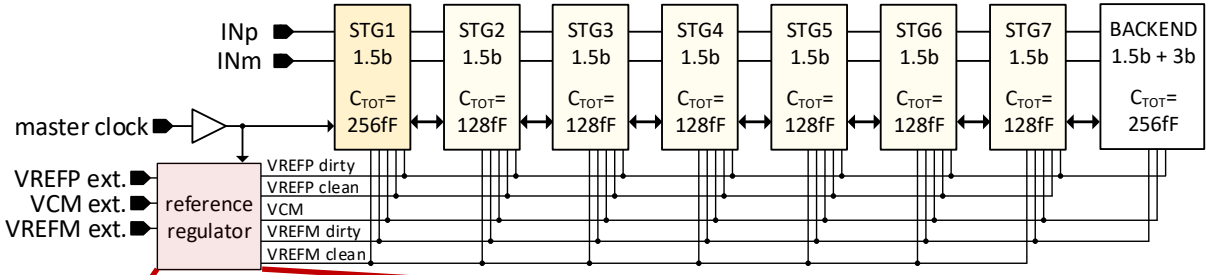
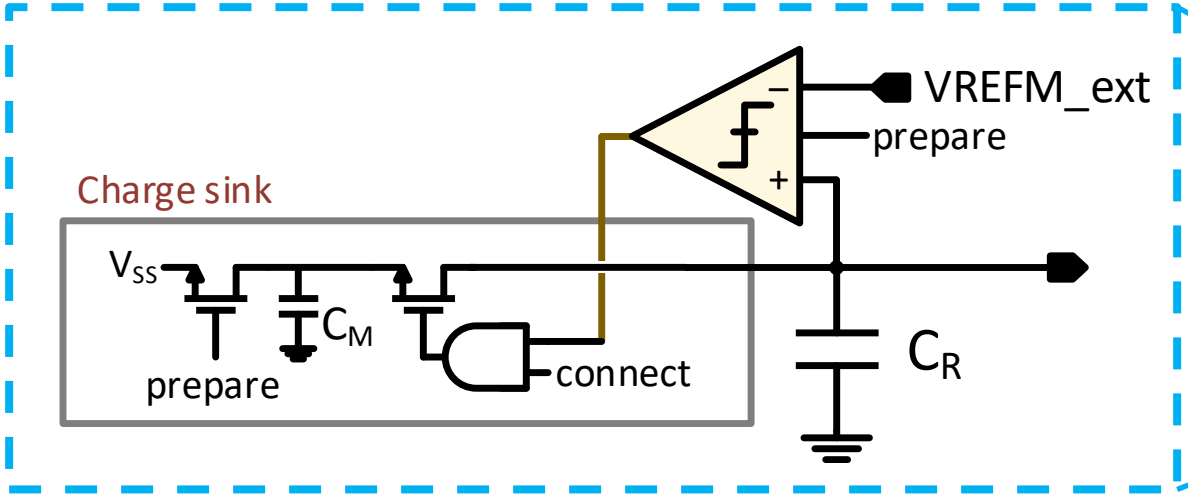
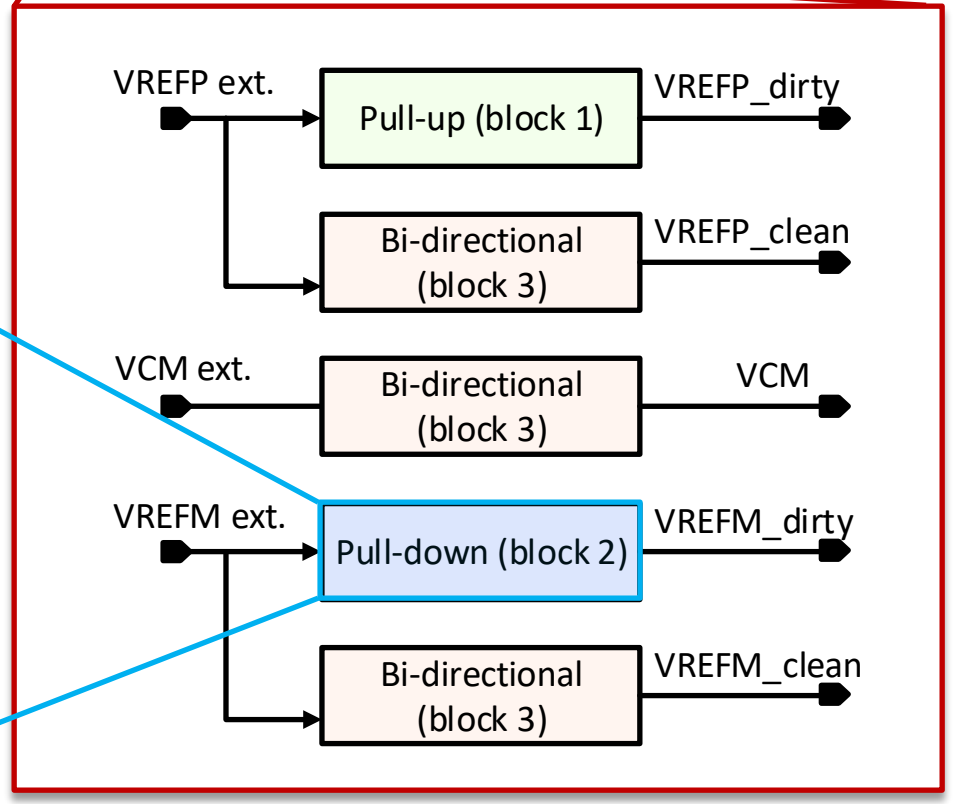
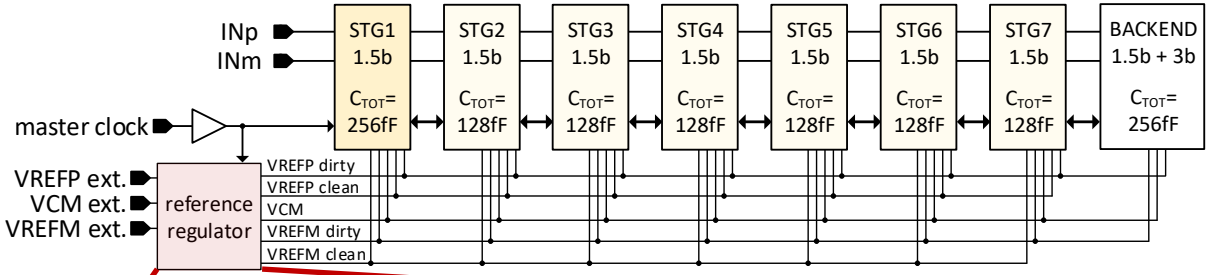


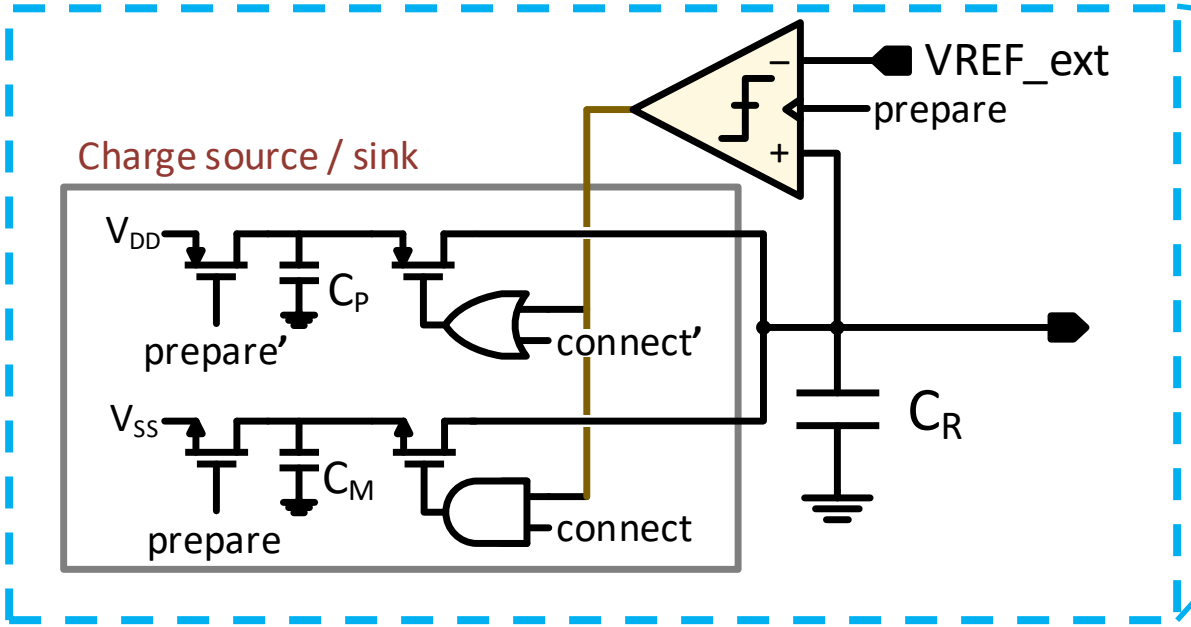


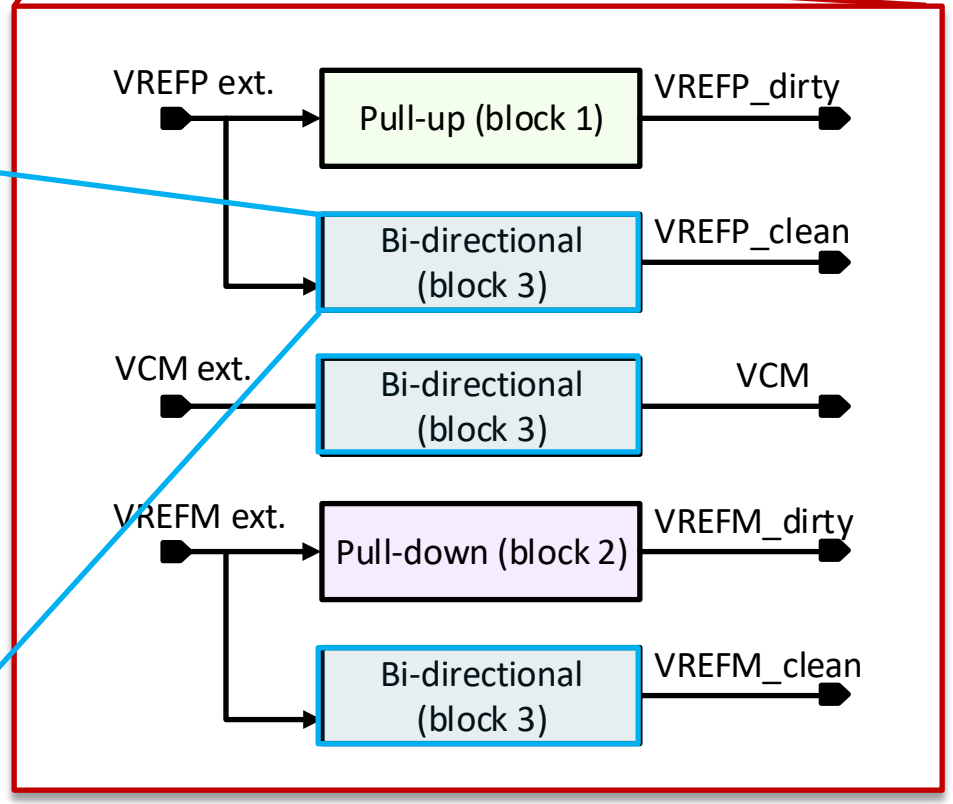


Global Reference Generation

- Bi-directional feedback for clean references and VCM
  - Must be able to sink or source

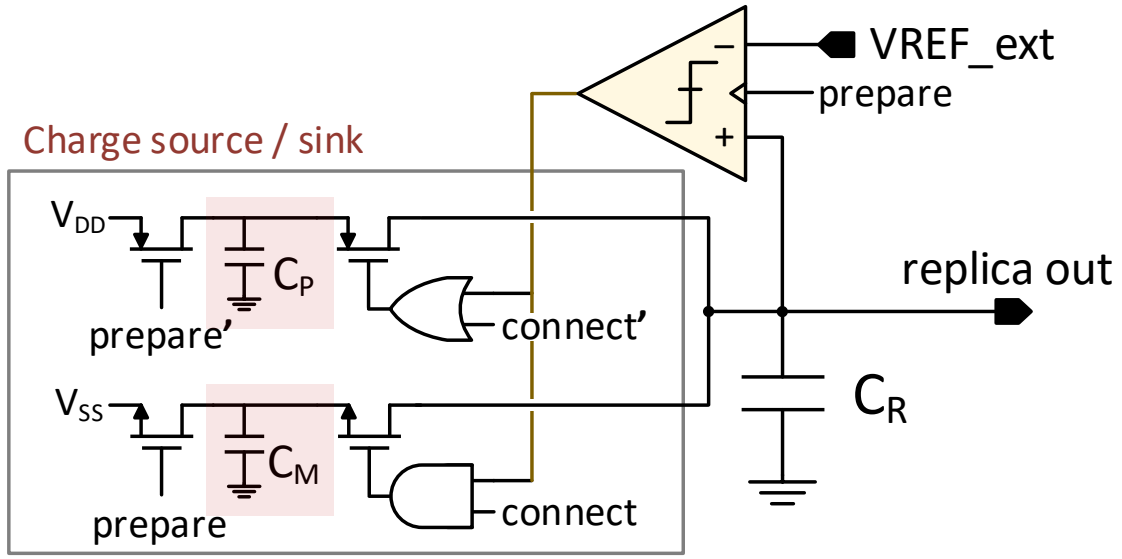






Regulator Design Considerations

- C_P / C_M sizing
  - Determined by max current pulled by load
- C_R sizing
  - Determined by reference ripple amplitude requirements (accuracy / noise)



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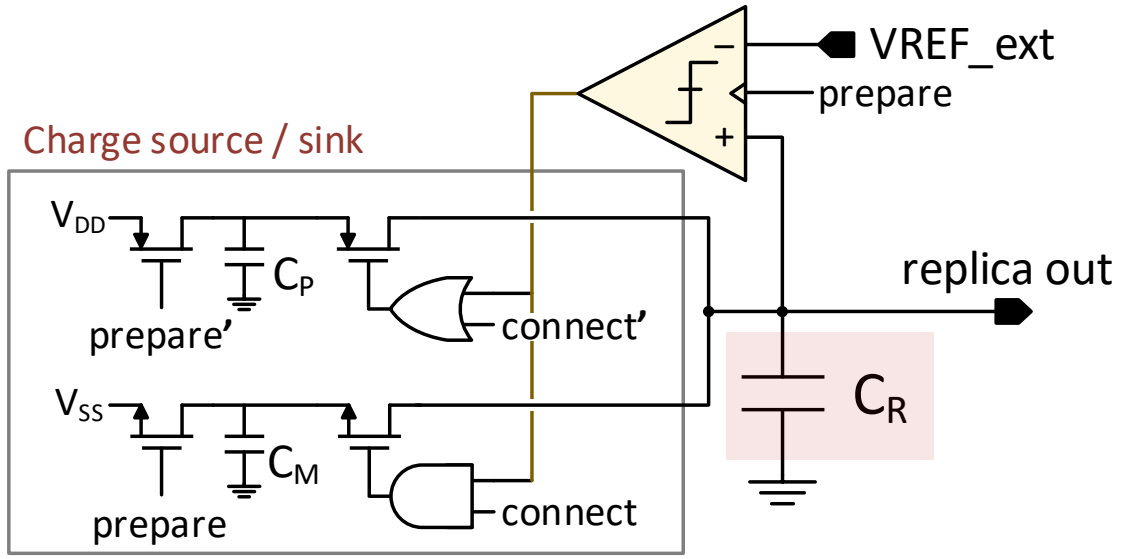
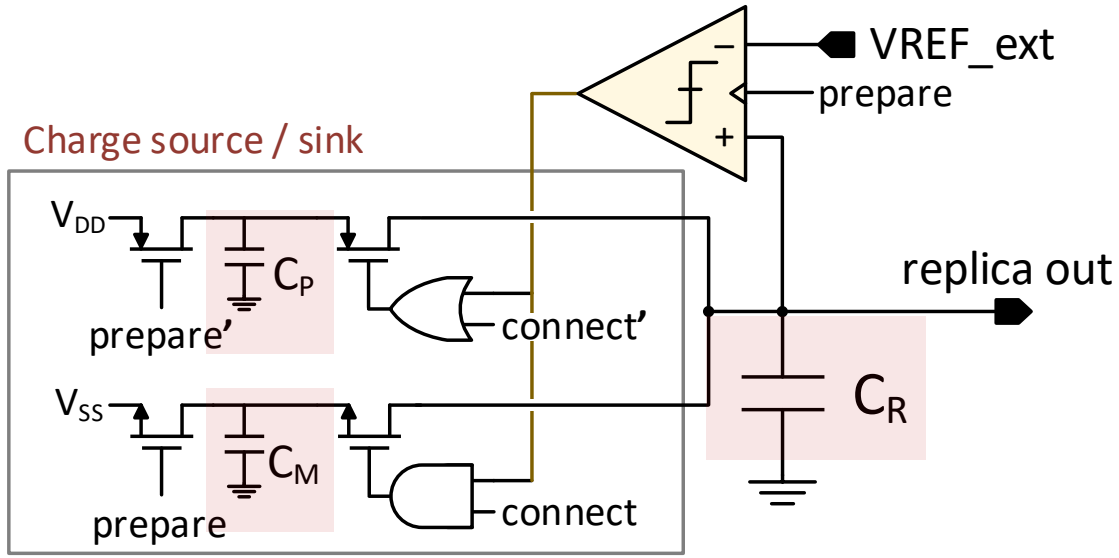


Regulator Design Considerations

- Dirty REF accuracy limited by reference ripple
  - Function of C_P/C_M vs. C_R
- Clean REF accuracy limited by comparator noise
  - Over-designed for low-noise
  - Can decimate to save power (only operate once every N cycles)



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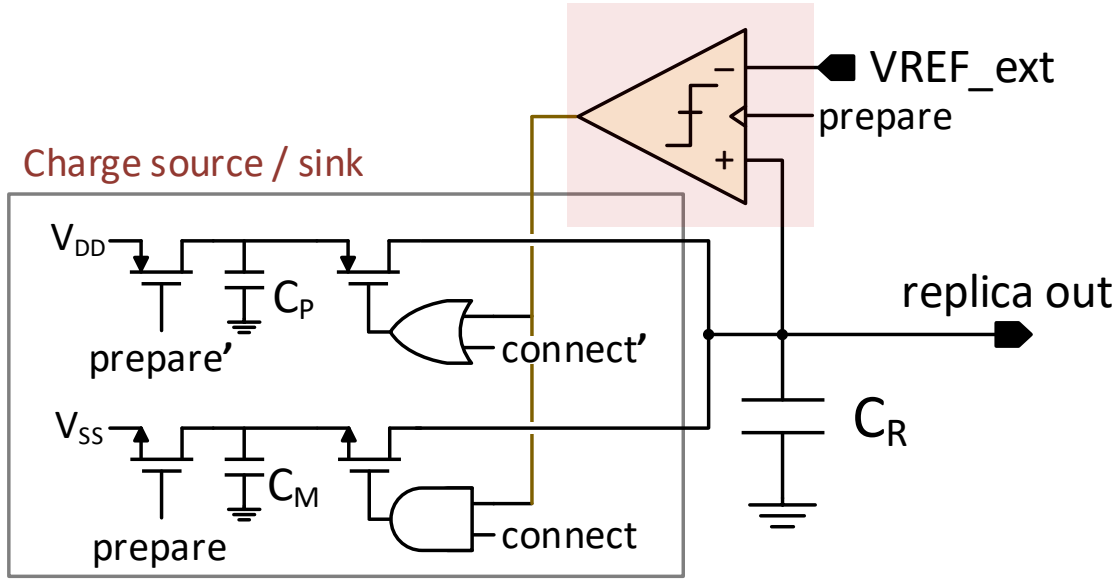


Regulator Design Values

- All capacitors made tunable for testing purposes
- Regulator area can be significantly reduced
  - Many non-essential test features

Nominal Capacitor Values

	C_P	C_M	C_R
VCM	130 fF	130 fF	45 pF
VREFP_dirty	4pF	-	45 pF
VREFM_dirty	-	2 pF	45 pF
VREFP_clean	320 fF	24 fF	120 pF
VREFM_clean	20 fF	320 fF	120 pF

Outline

- Ringamp Topology
- Fully Dynamic Reference Regulation
- Scope-on-Chip Amplifier Settling Monitor
- Performance Summary & Conclusion

2 Approaches to Ringamp Robustness

- Robust by design
  - No calibration, but needs design margin
  - Several SoTA designs using this:

    [Hung, ISSCC 2020] 100MS/s, 71.7dB SNDR, 2.2fJ/c-step FoM_W

    [Lim, JSSC Dec. 2015] 50MS/s, 70.9dB SNDR, 6.9fJ/c-step FoM_W

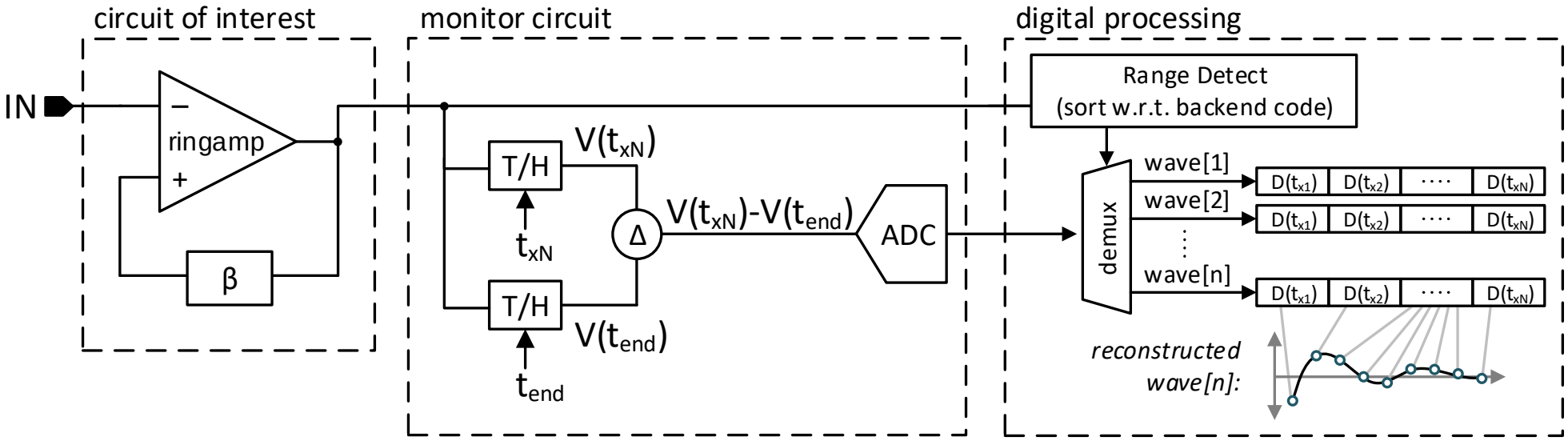
    [Lim, VLSI 2017] 100MS/s, 73.2dB SNDR, 6.1fJ/c-step FoM_W

- Robust by background tuning / calibration / digital assistance
  - Max performance, but possibly more complex
  - Less has been tried here - interesting research questions!

    [Hershberg, ISSCC 2019, Paper 3.1]

Ringamp Waveform Capture

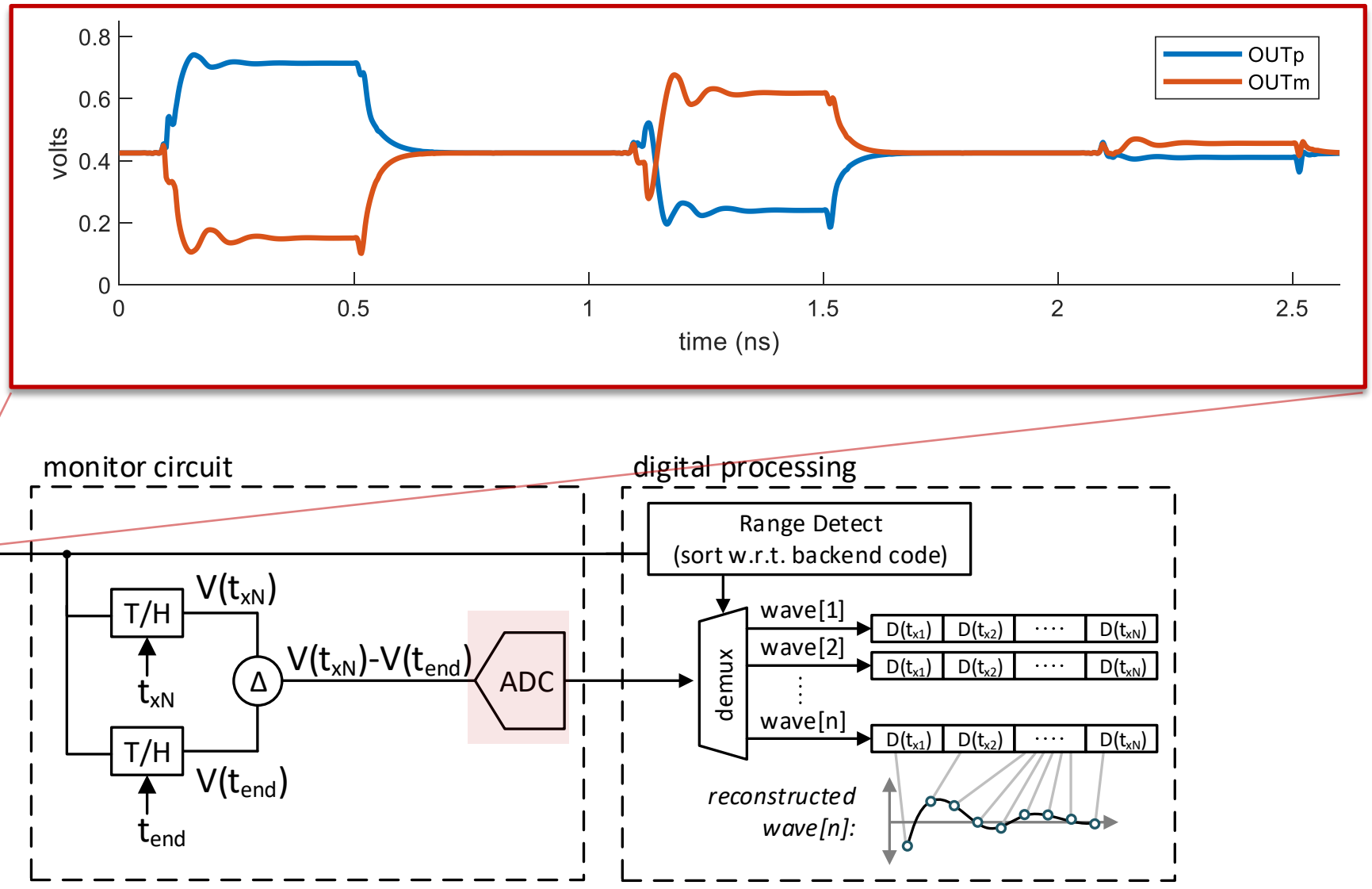
- Main goals:
  1. Background capture of amplifier settling waveform
  2. Use this information to optimize ringamp biasing / performance



Ringamp Waveform Monitoring

Challenge 1:

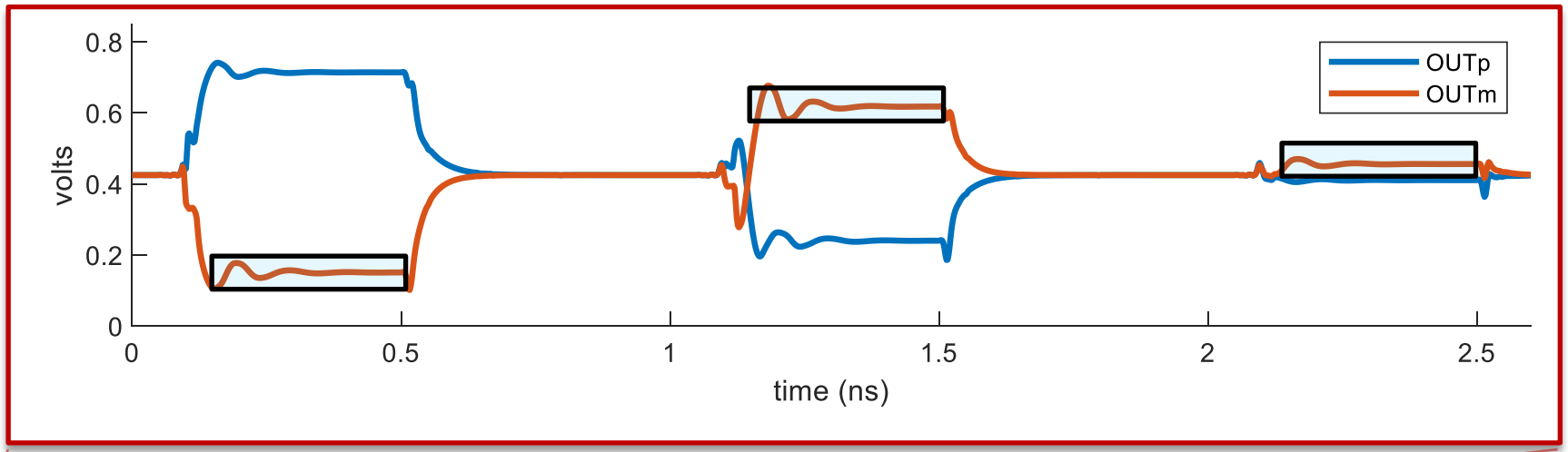
Large residue range

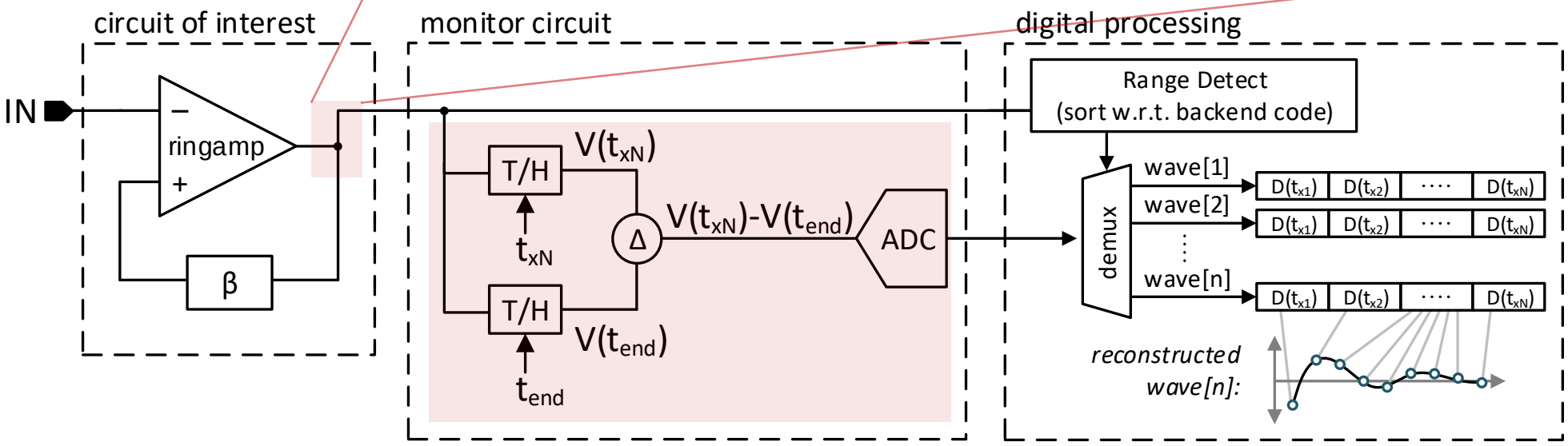


Ringamp Waveform Monitoring

Challenge 1:
Large residue range

Solution: Sample w.r.t. final value

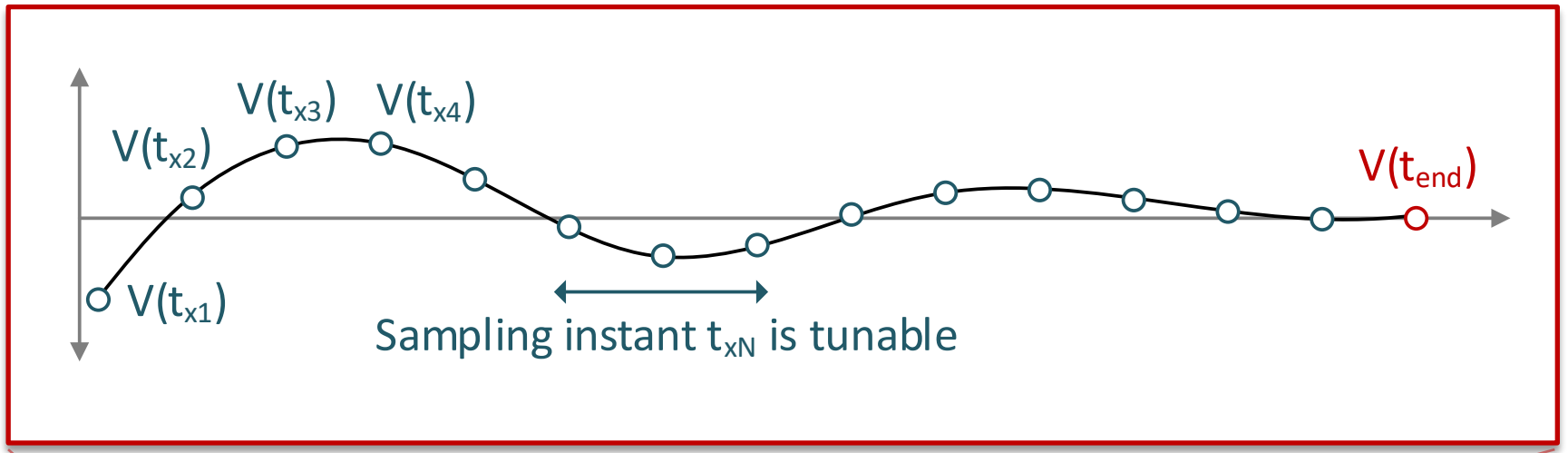


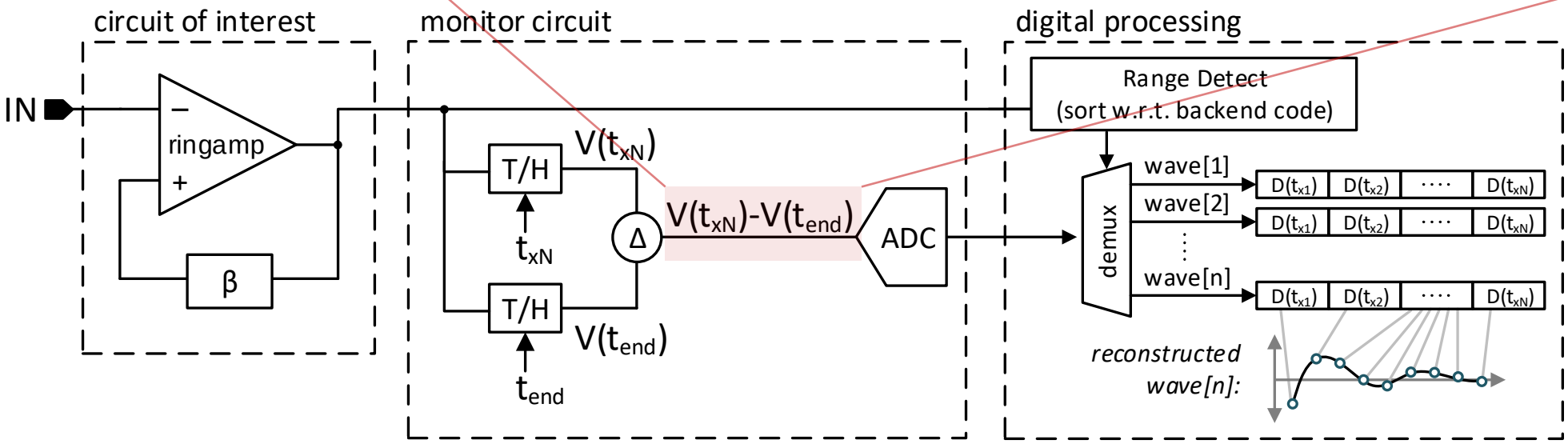


Ringamp Waveform Monitoring

Challenge 2:
Time-series capture

Solution: Combine cycles with similar $V(t_{end})$





Ringamp Waveform Monitoring

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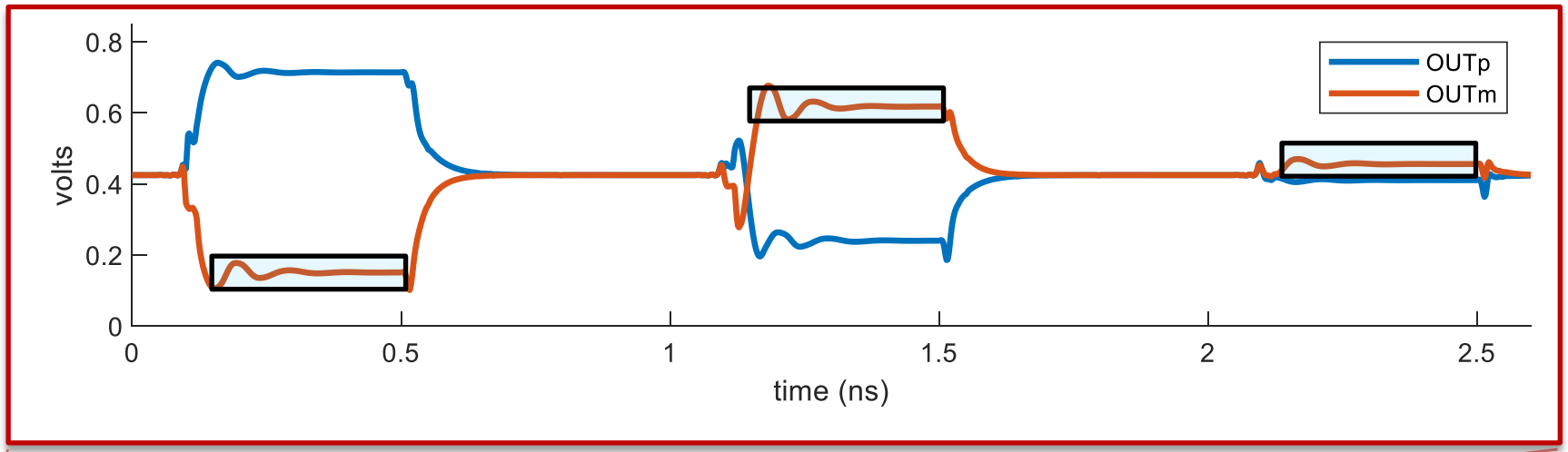

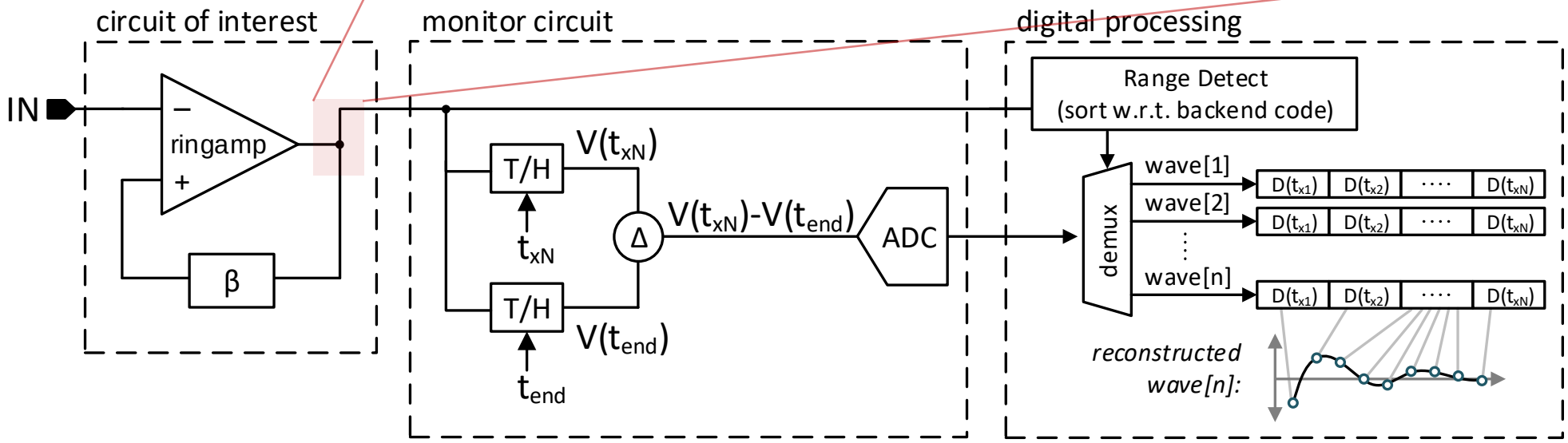

Ringamp Waveform Monitoring

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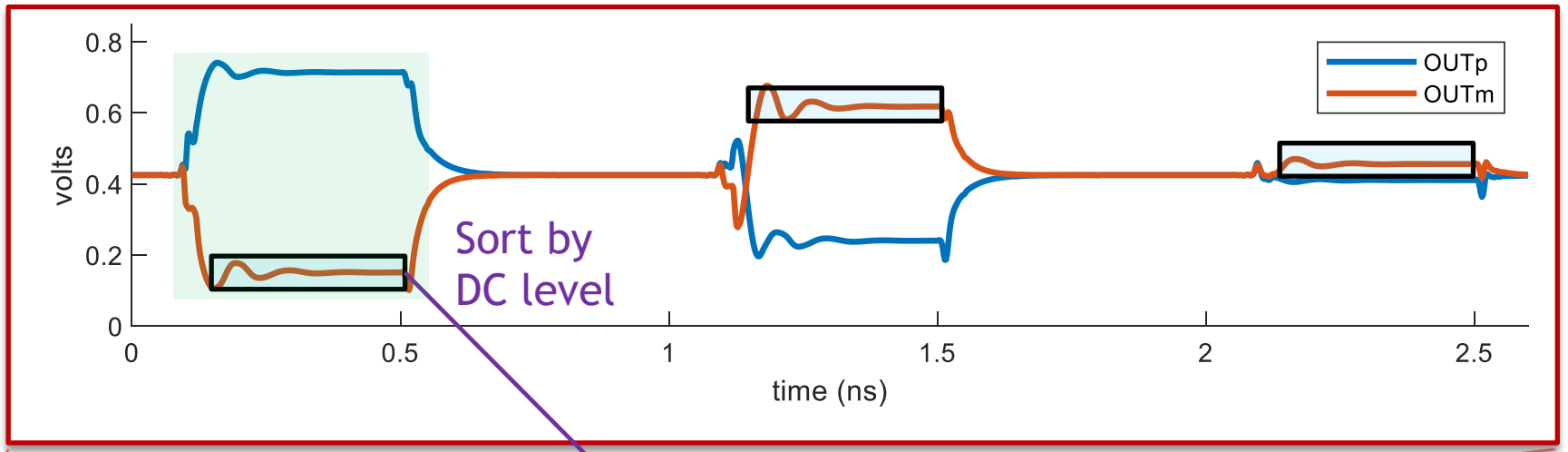
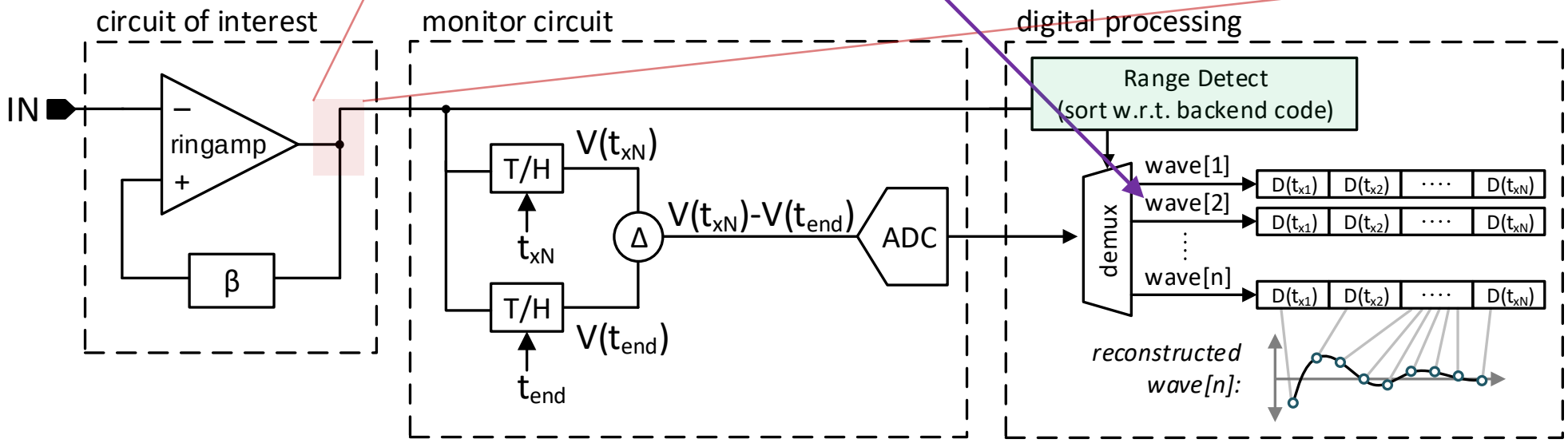
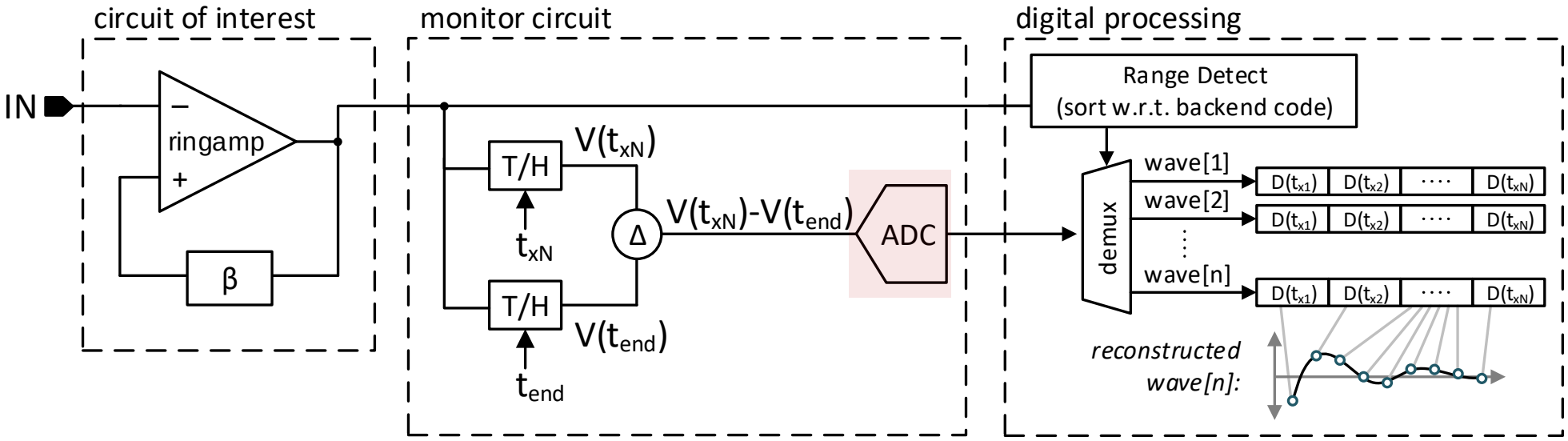




Ringamp Waveform Monitoring

Challenge 3:

Low complexity

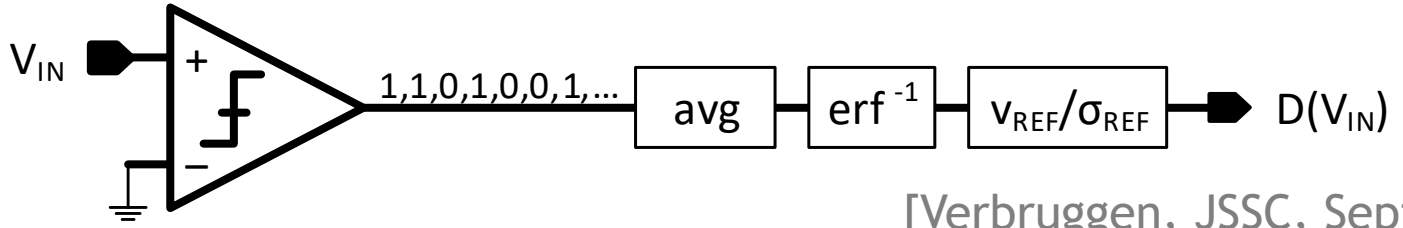


Ringamp Waveform Monitoring

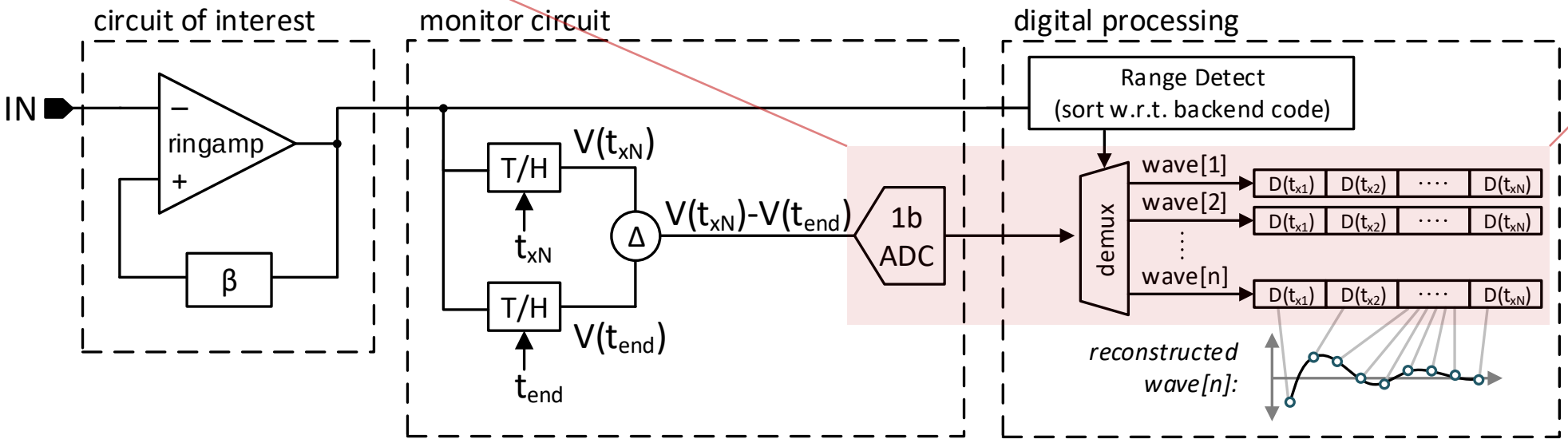
Challenge 3:
Low complexity

Solution: 1-bit stochastic ADC

Concept: use a comparator's gaussian noise distribution to quantize



[Verbruggen, JSSC, Sept. 2015]



Ringamp Waveform Monitoring

Challenge 3:
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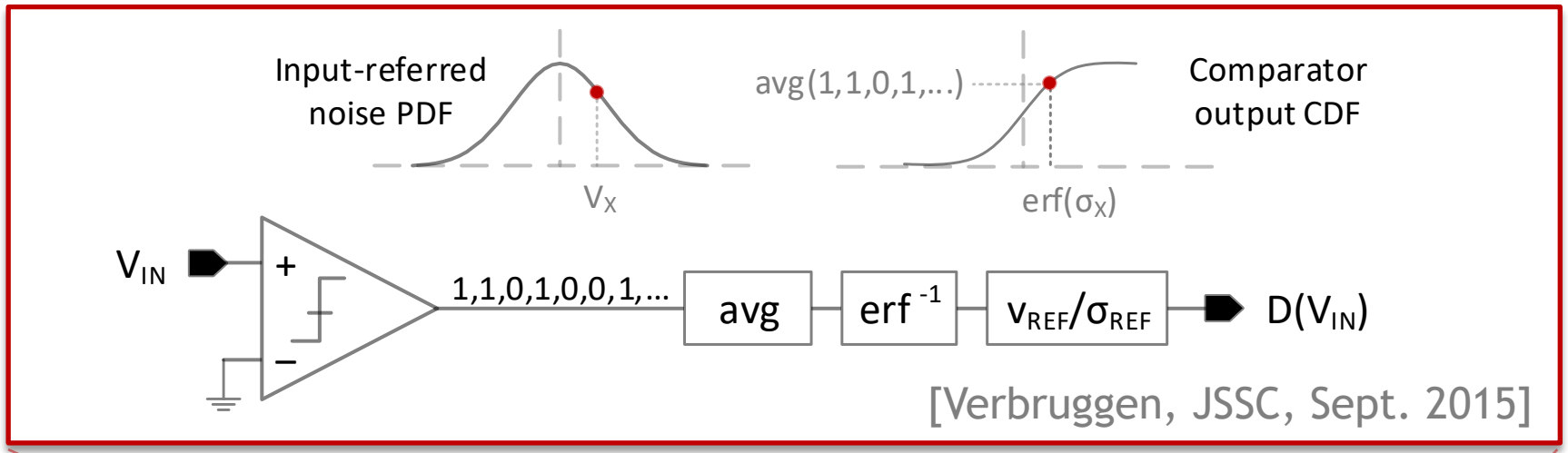
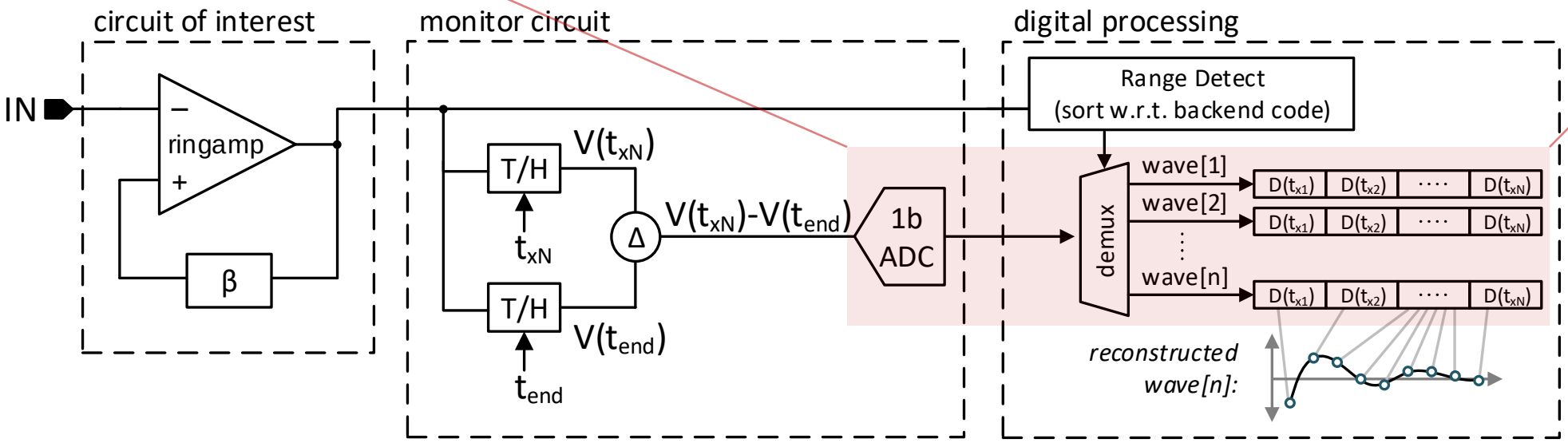
Solution: 1-bit stochastic ADC



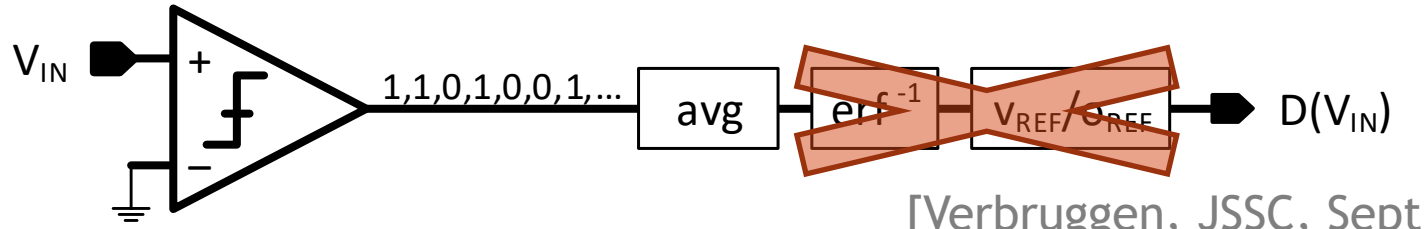


Ringamp Waveform Monitoring

Challenge 3:
Low complexity

Solution: 1-bit stochastic ADC

If some distortion acceptable, can skip these steps



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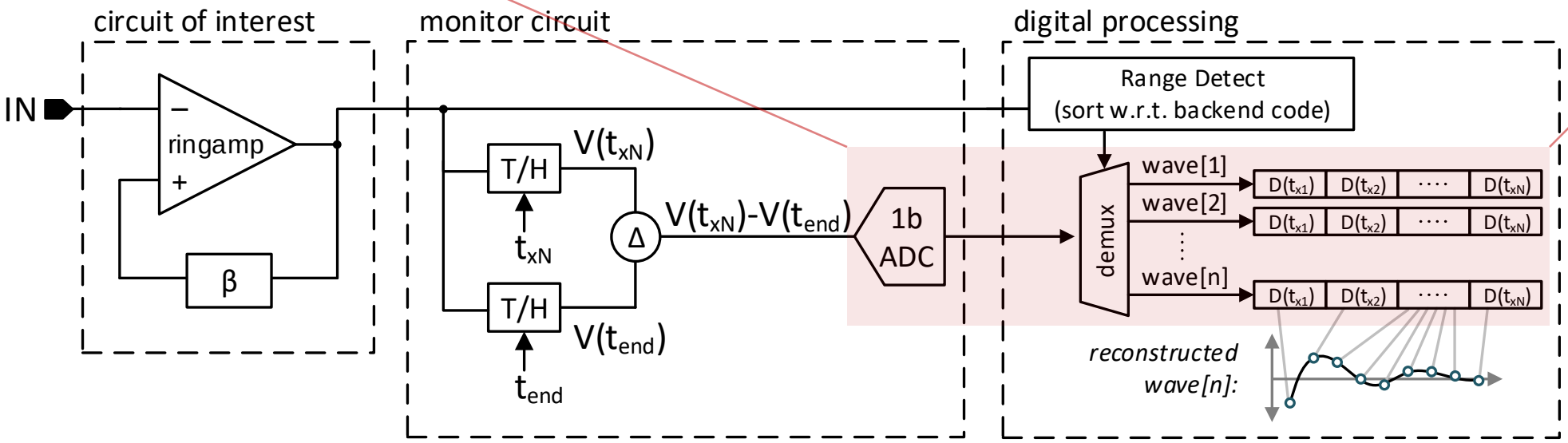

Ringamp Waveform Monitoring

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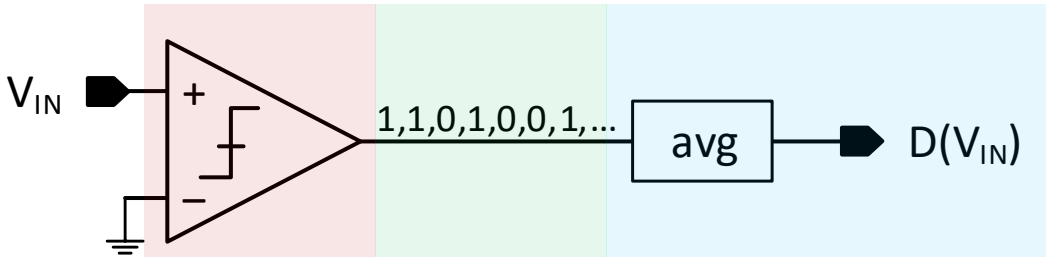
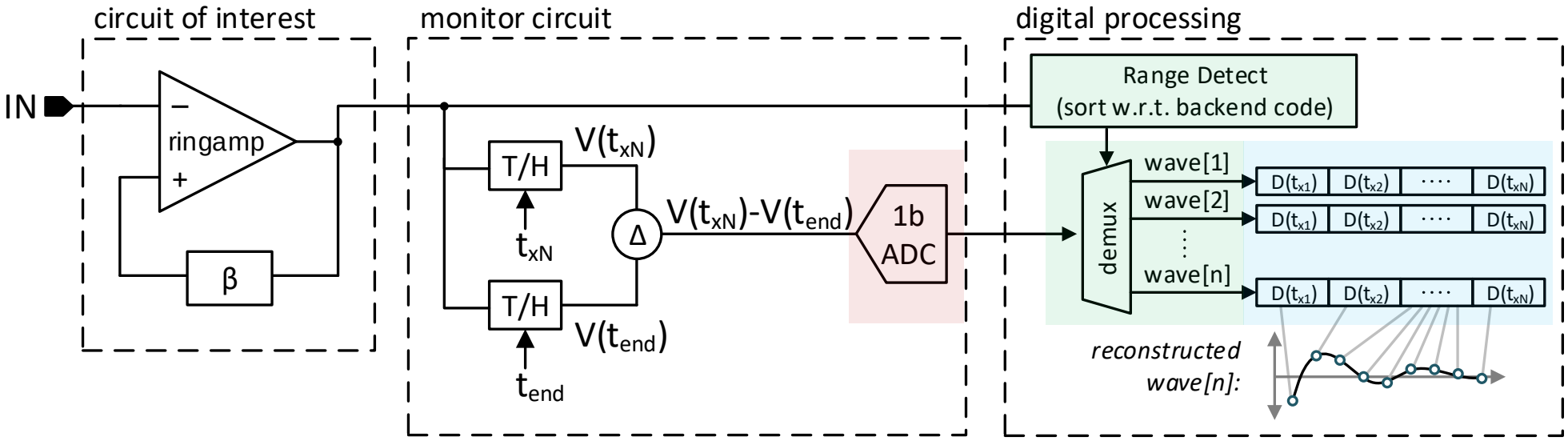
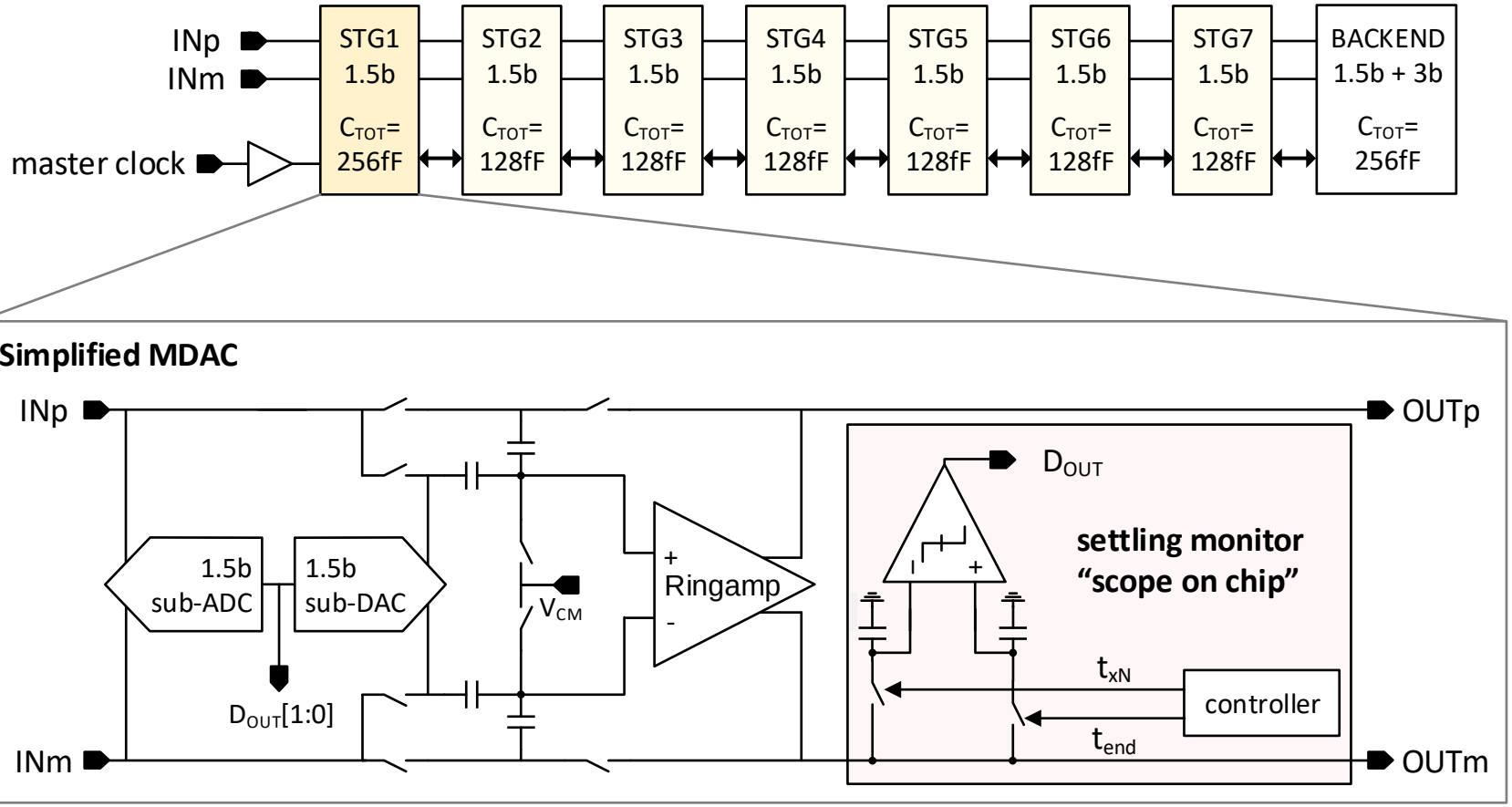




Practical Implementation

- Monitor circuit added to output of each stage
- Single-ended scheme here
  - Dummy sampler also on OUTp
  - Fully differential also possible



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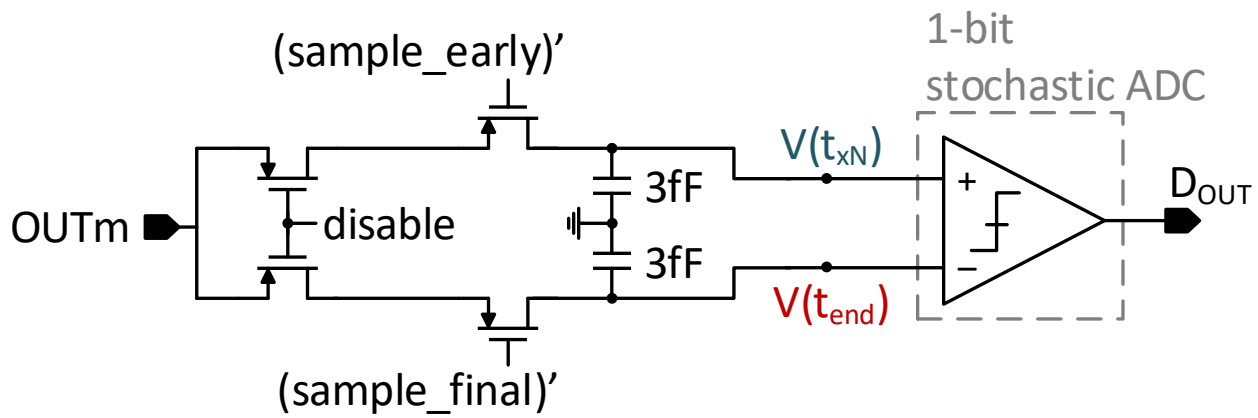

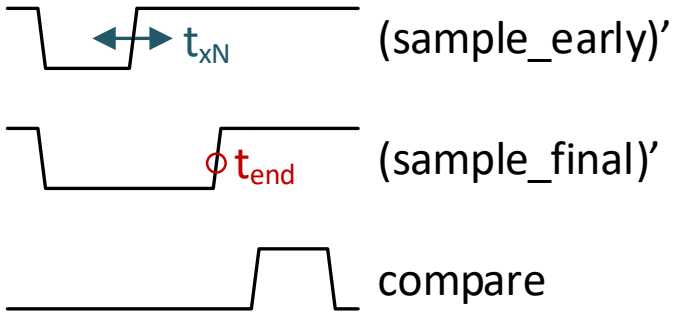

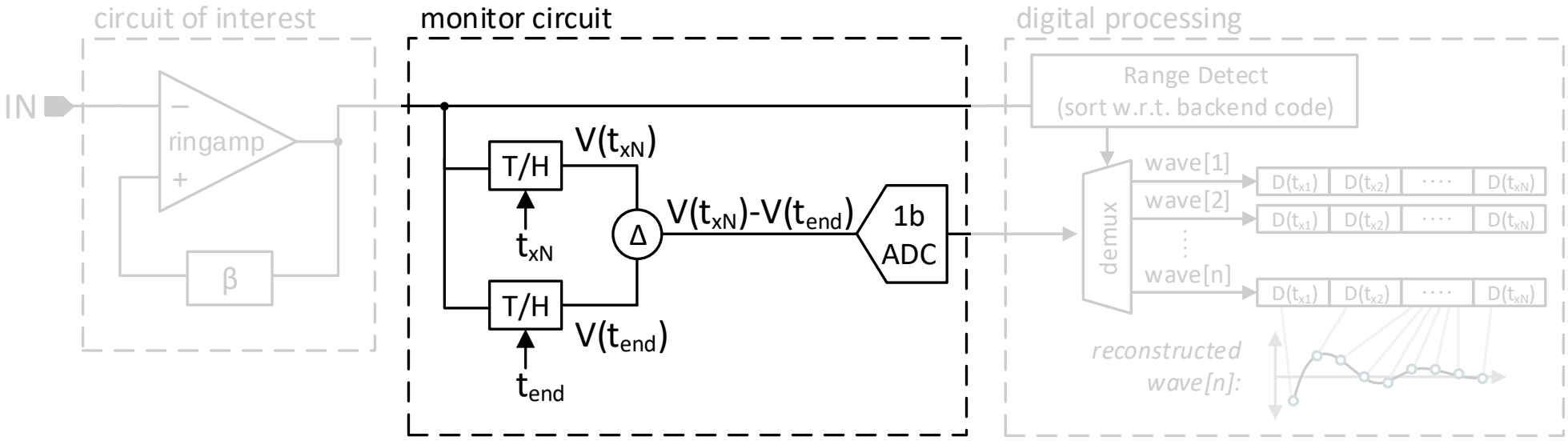

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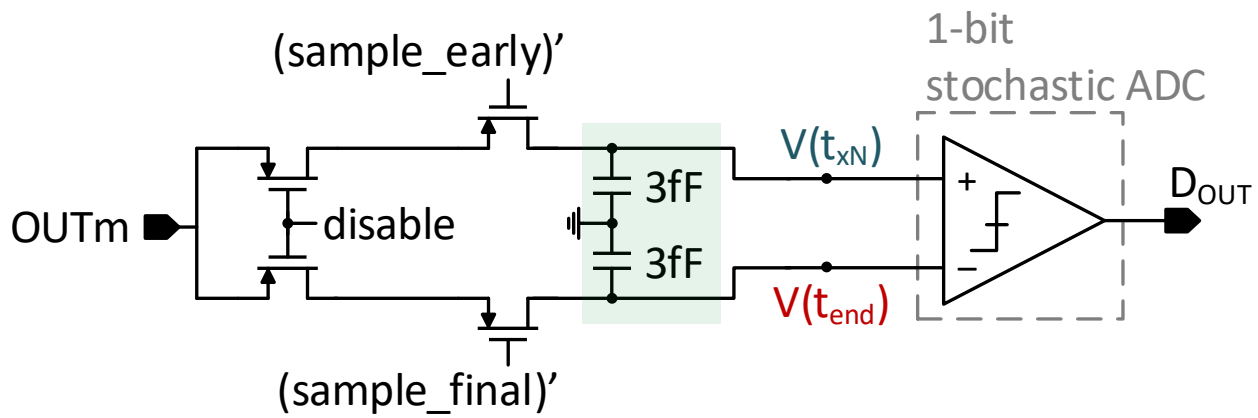
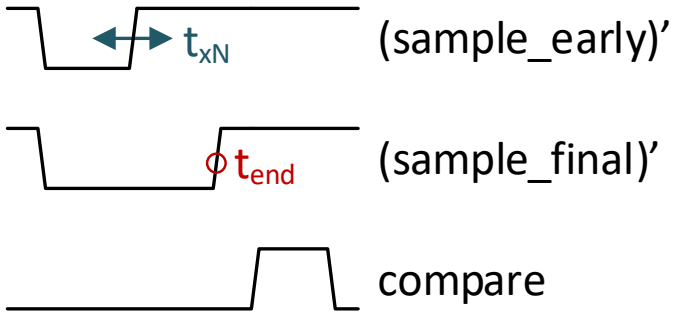
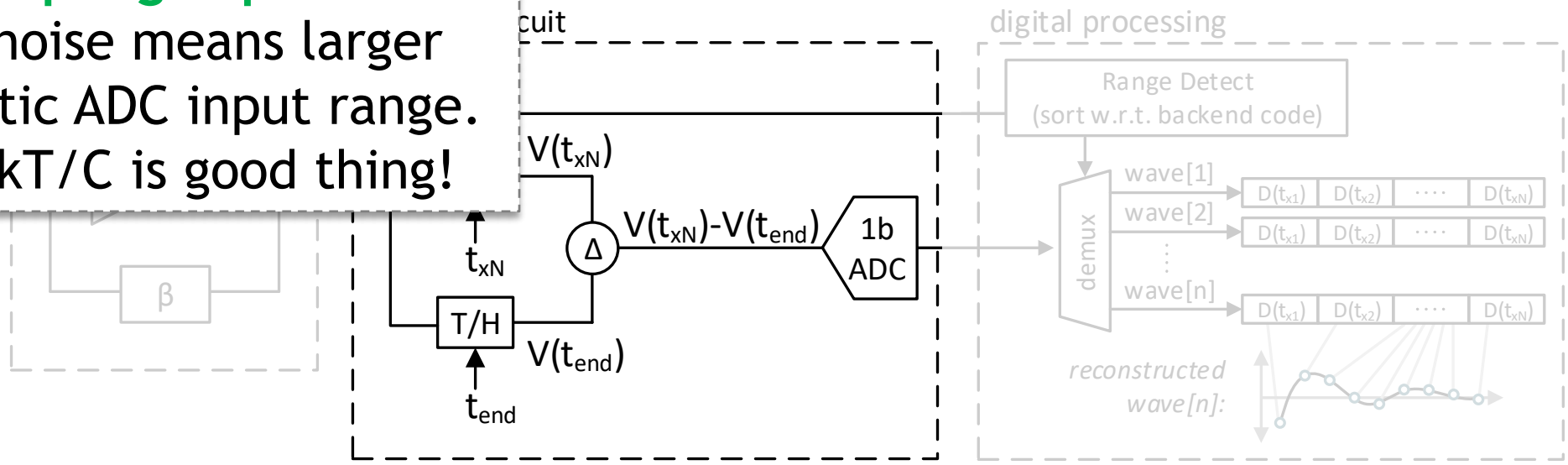




Tiny Sampling Capacitance

More noise means larger stochastic ADC input range. Here, kT/C is good thing!



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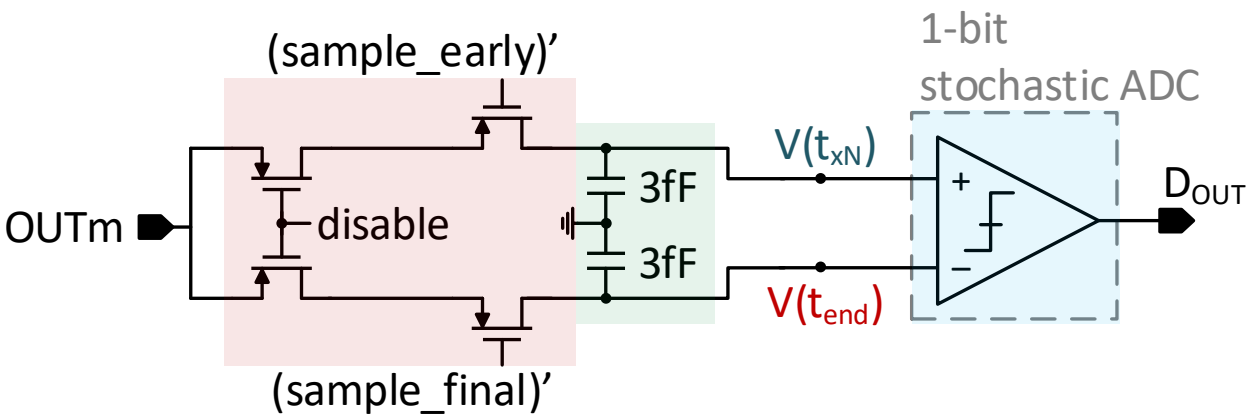
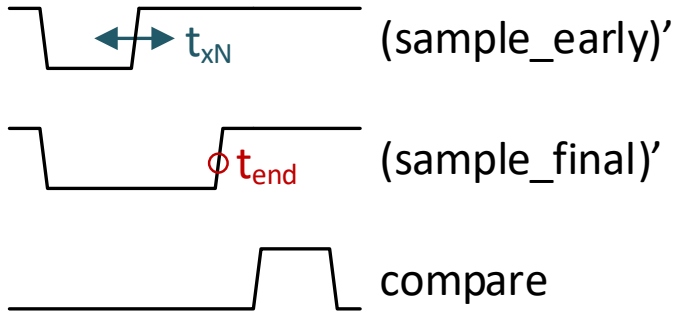
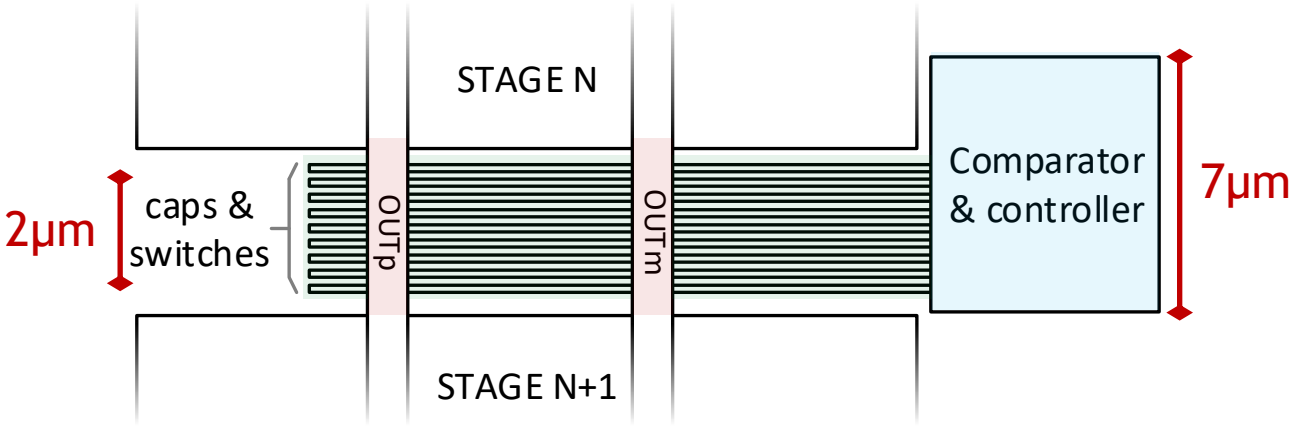
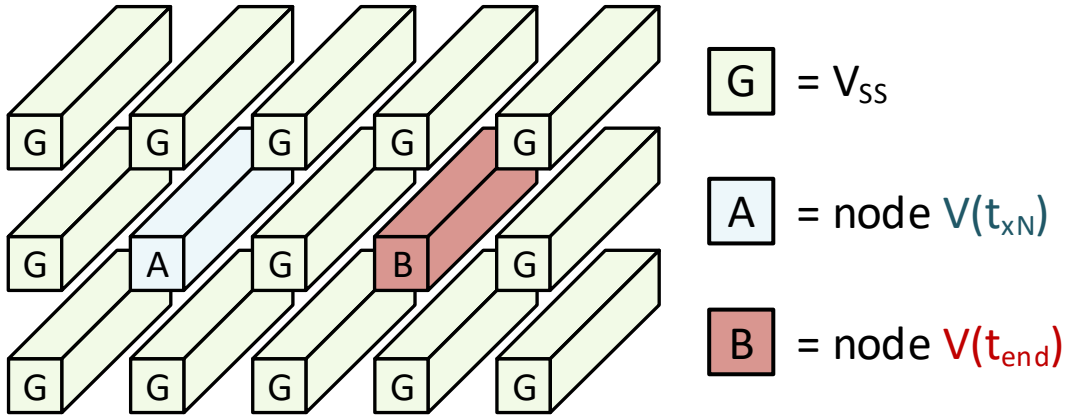






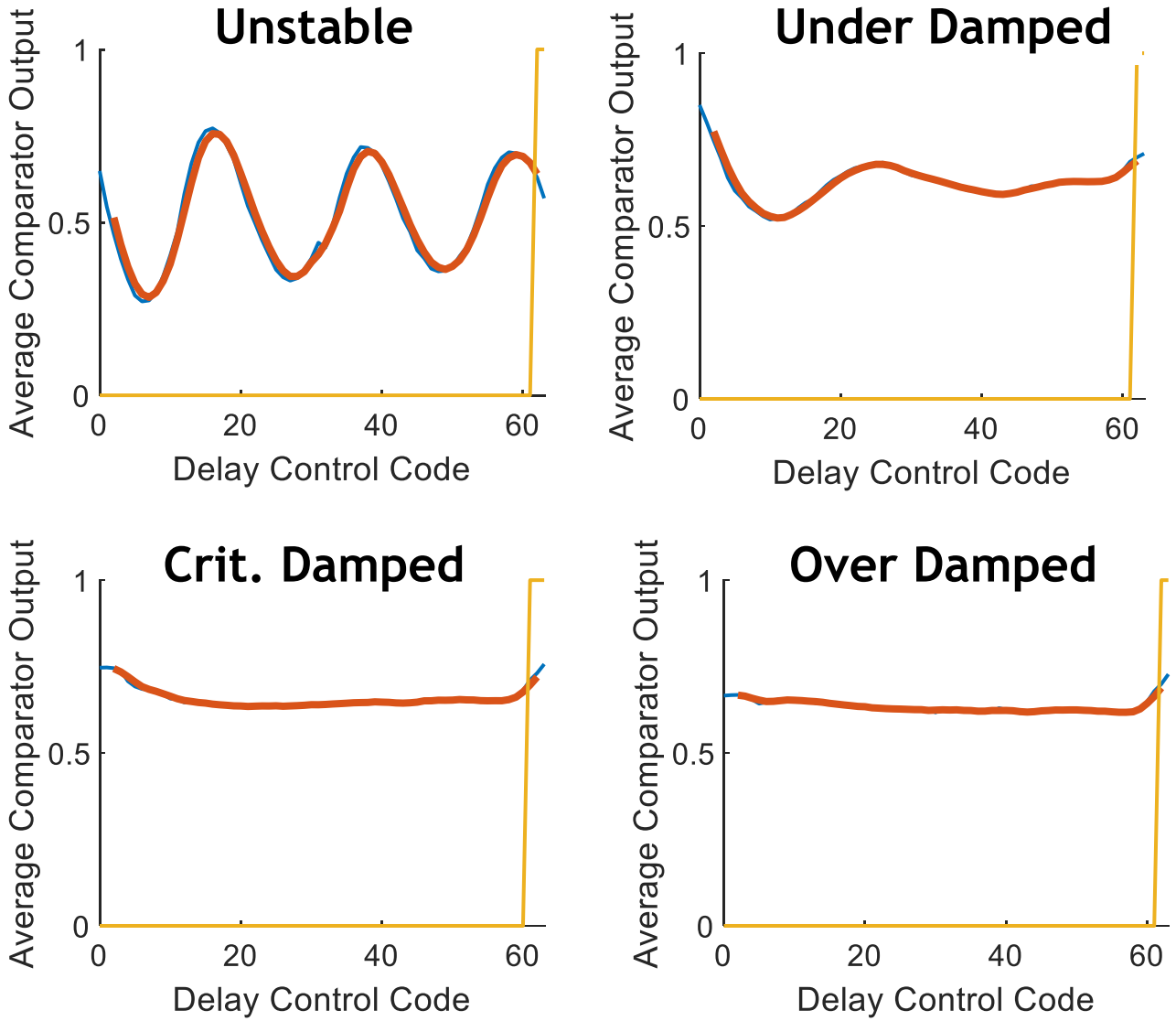
Compact layout between pipeline stages



Capacitors built from routing wires

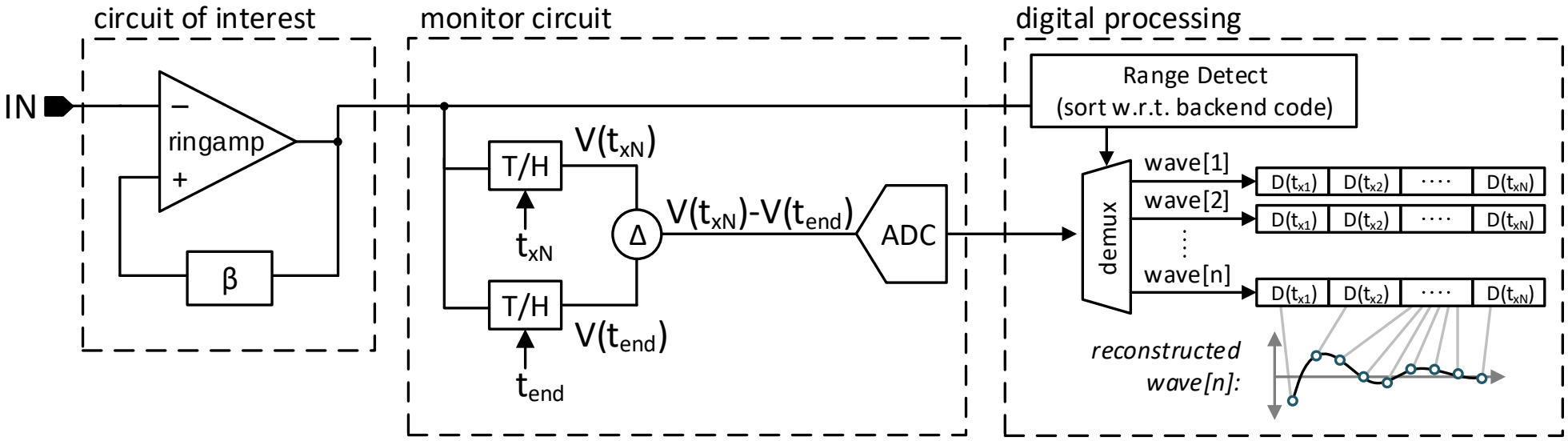
Measured Amplifier Settling Waveforms

- Provides direct insight into amplifier settling behavior!
  - Verification
  - Debug
  - Calibration?...



Ringamp Waveform Capture

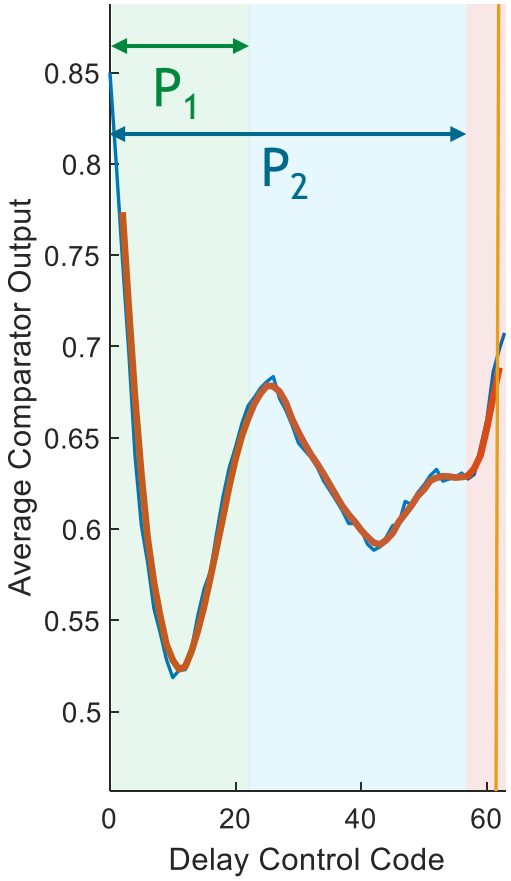
- Main goals:
  1. Background capture of amplifier settling waveform ✓
  2. Use this information to optimize ringamp biasing / performance



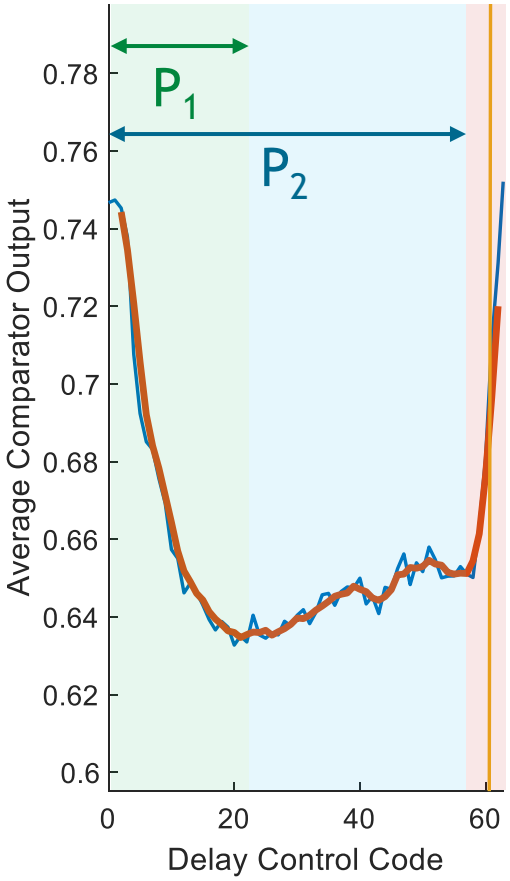
Defining an Objective Function for Bias Control

- **Observation:** only the Critically Damped case has:
  - Initial large amplitude
  - Final small amplitude
- Estimator = P_2 / P_1
- Other variations of this concept also work

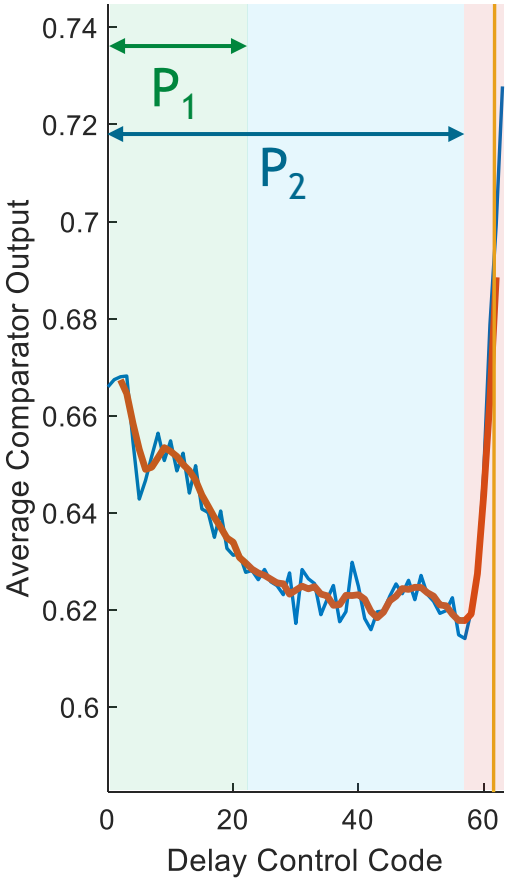
Under Damped (code 50)



Crit. Damped (code 100)

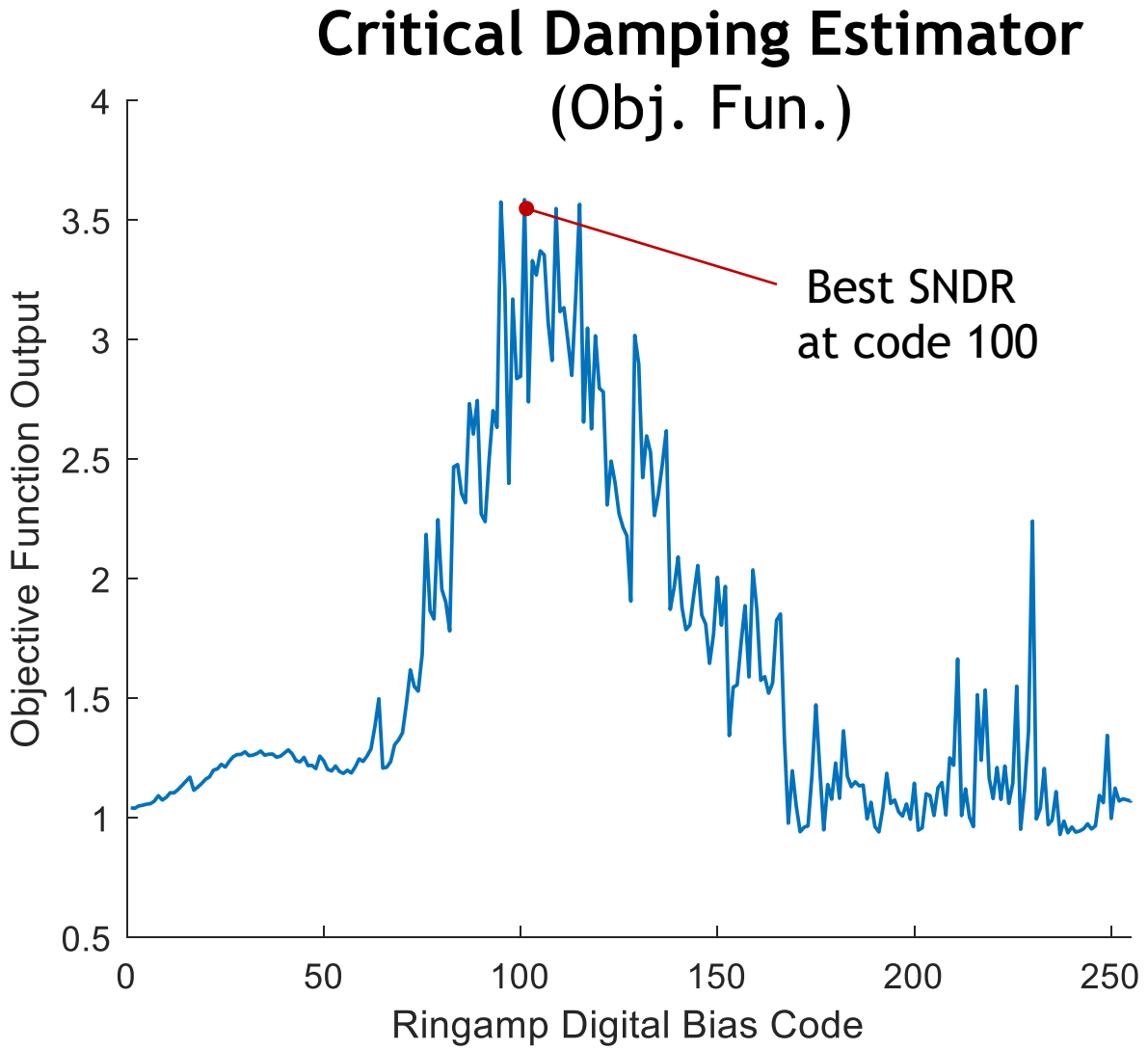


Over Damped (code 150)



Defining an Objective Function for Bias Control

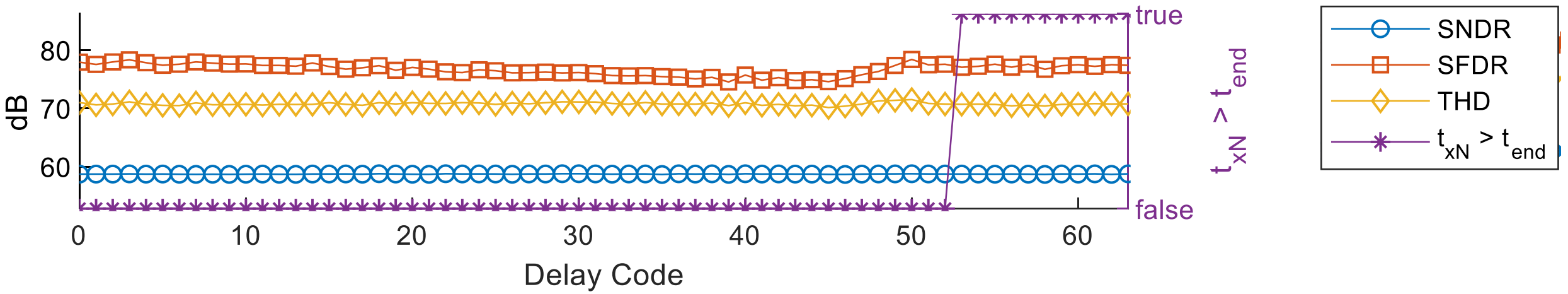
- Estimator = P_2 / P_1
- Accurately predicts the bias optimum (within certain margin) ✓
- PVT tracking loop possible
  - But not implemented



Background operation of Ringamp Monitor

- Monitor circuit samples during normal operation
  - Disturbs residue slightly

- Minimal performance impact ✓
  - SNDR: no loss
  - THD: no loss
  - SFDR: -3dB worst-case

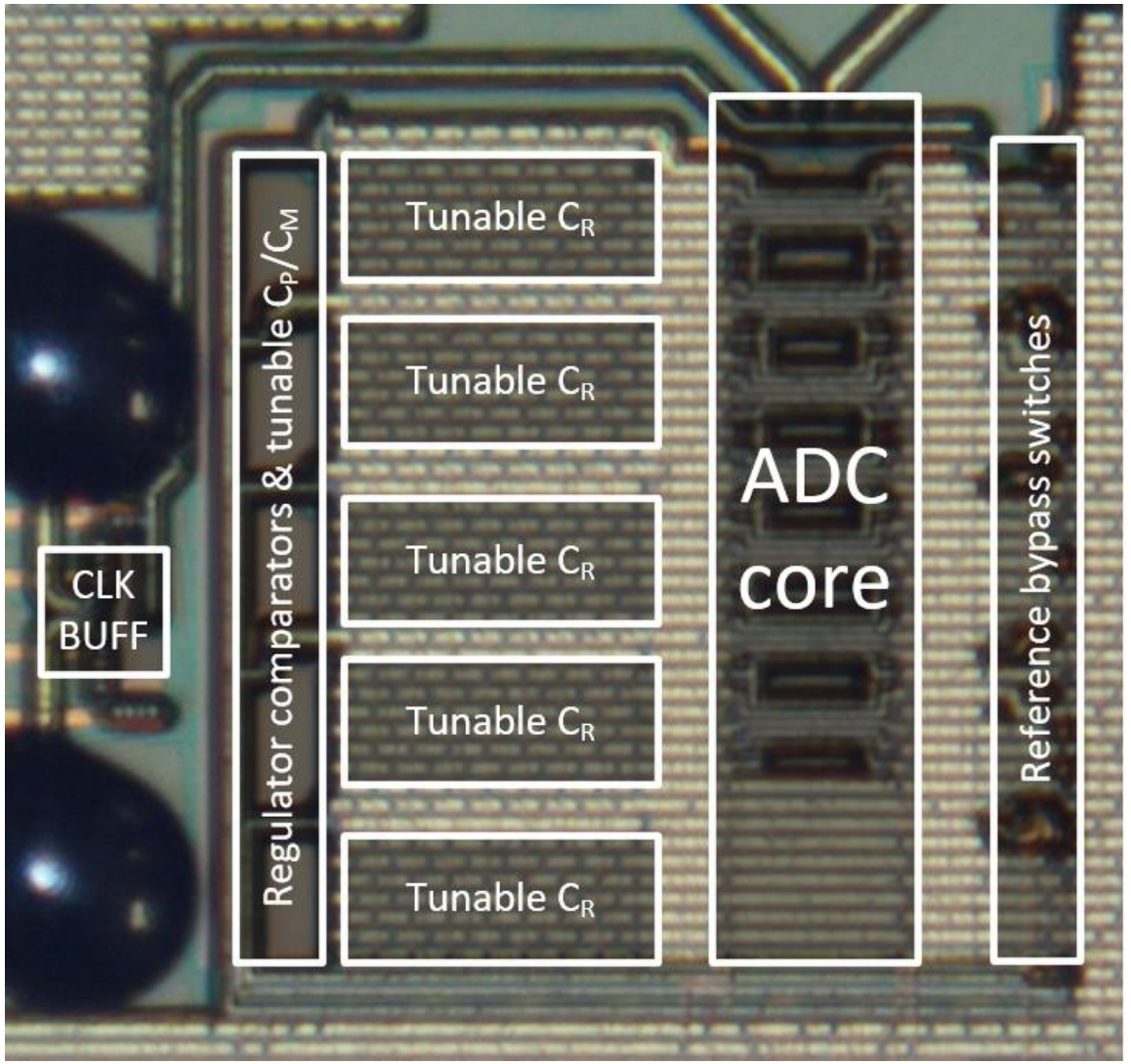


Outline

- Ringamp Topology
- Fully Dynamic Reference Regulation
- Scope-on-Chip Amplifier Settling Monitor
- Performance Summary & Conclusion

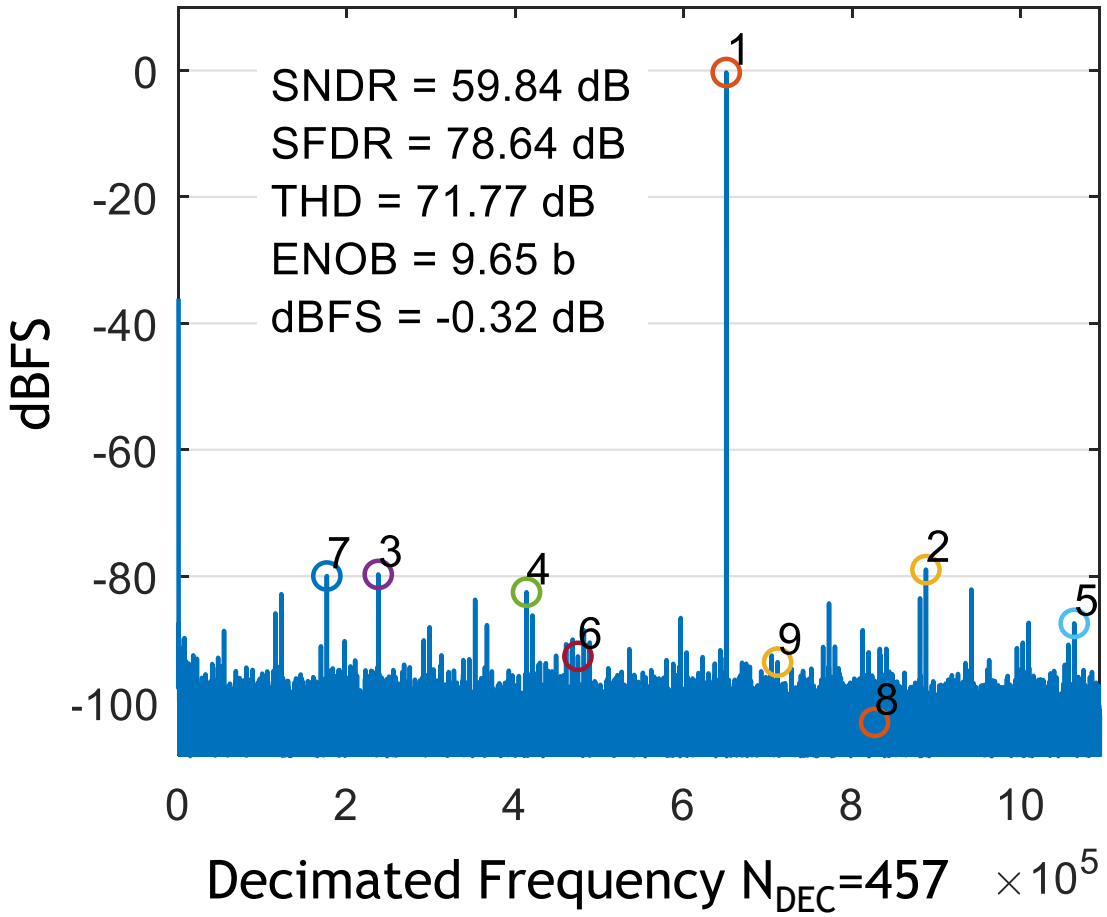
Measurement Results

- 16nm CMOS FinFET
- 0.095 mm^2

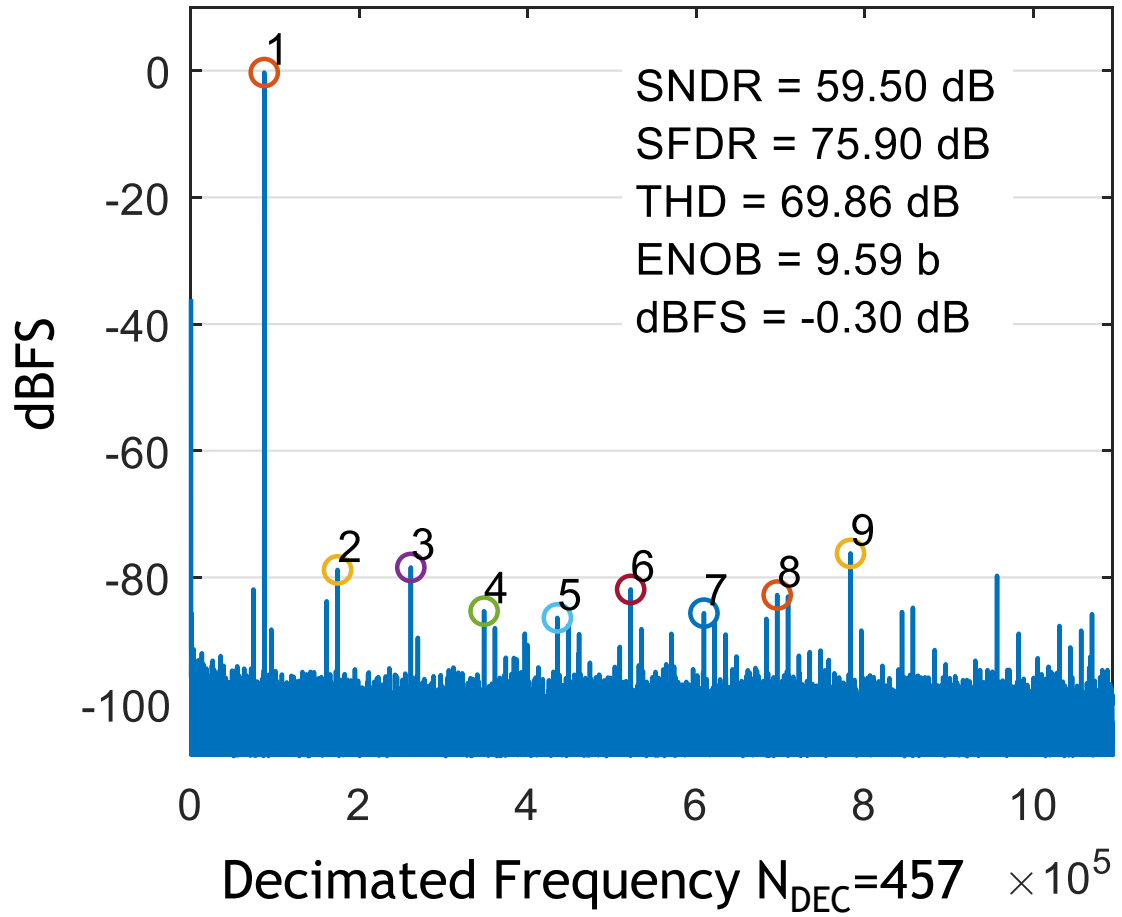


ADC Output Spectrum with Regulation

F_{IN} = 100MHz, F_{CLK} = 1GHz

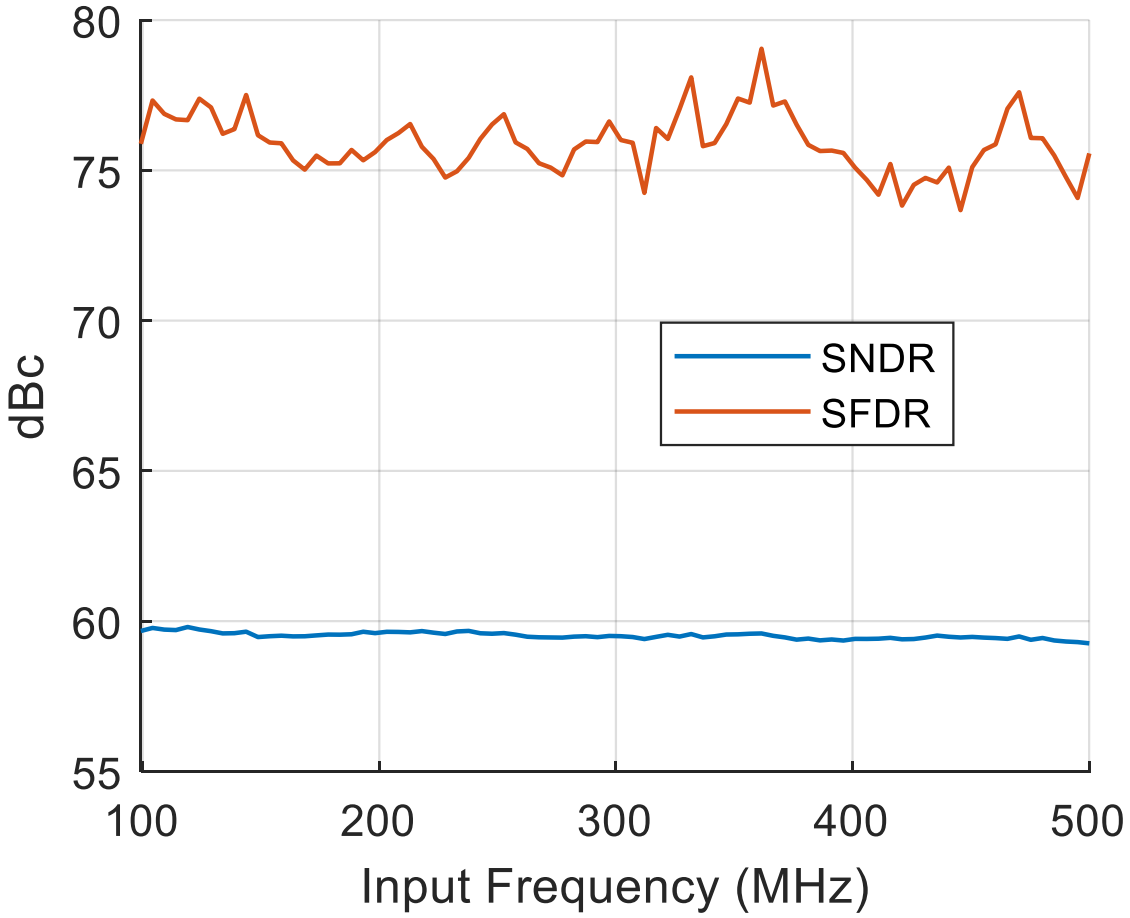


F_{IN} = 500MHz, F_{CLK} = 1GHz

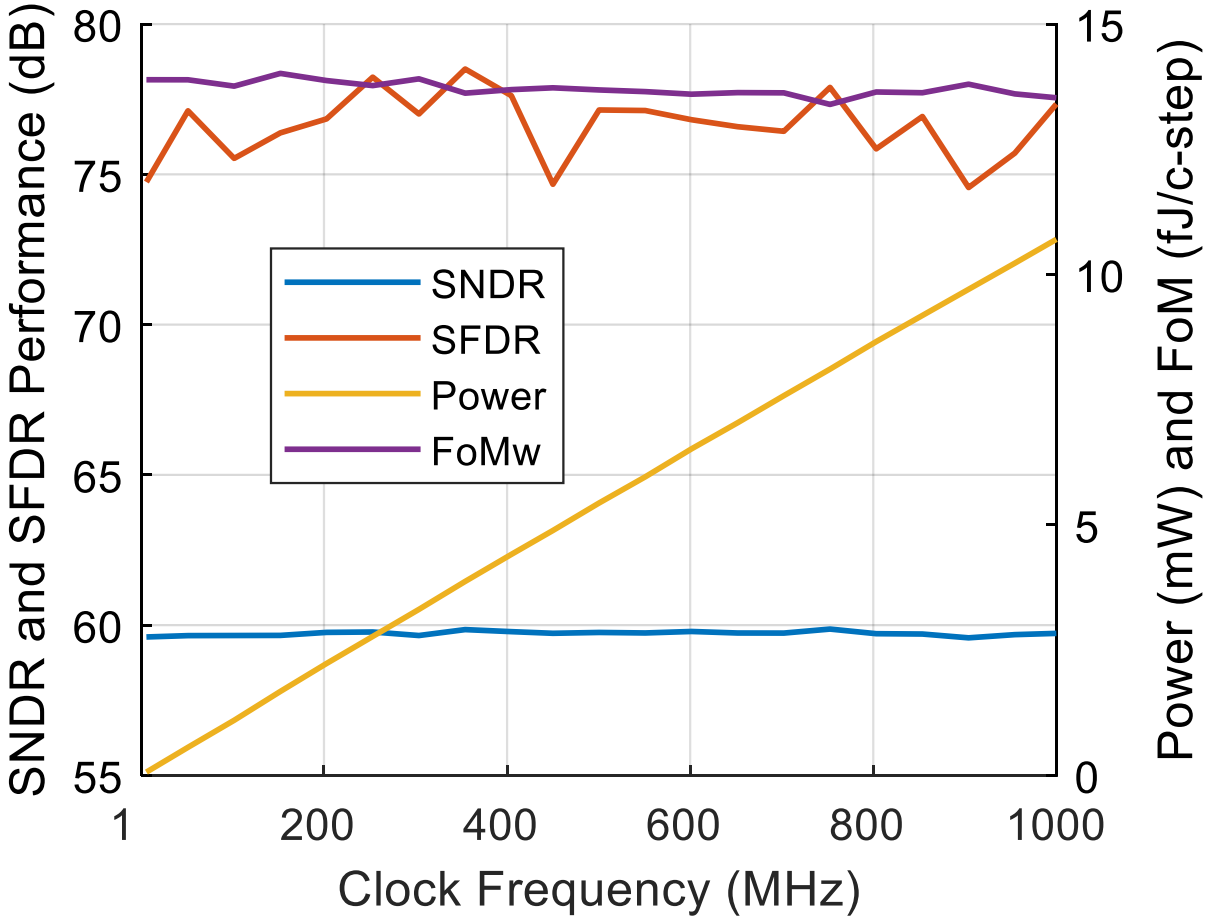


Frequency Sweeps

F_{IN} Sweep: 100MHz – 500MHz

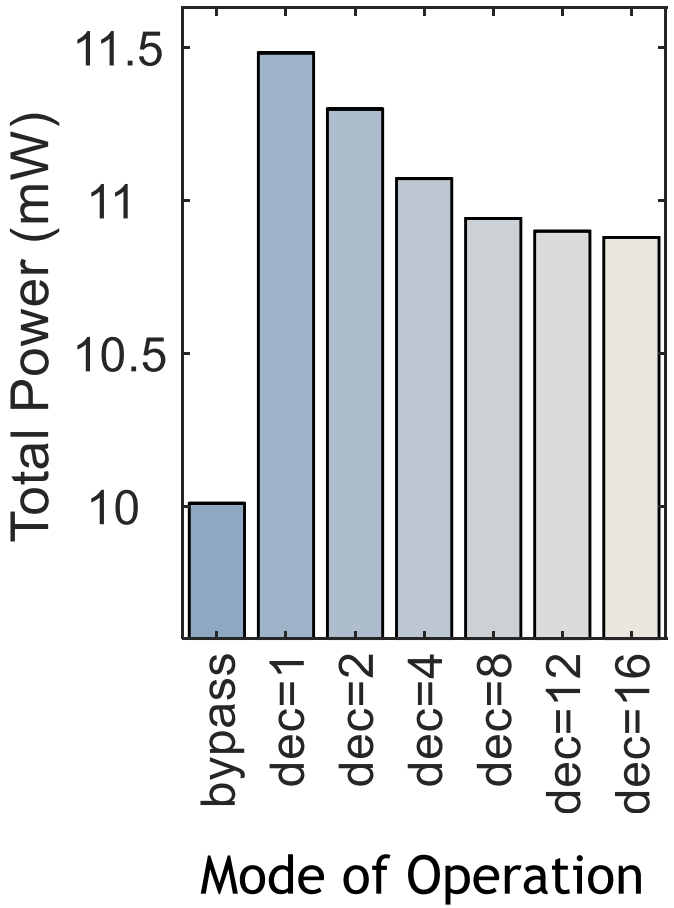


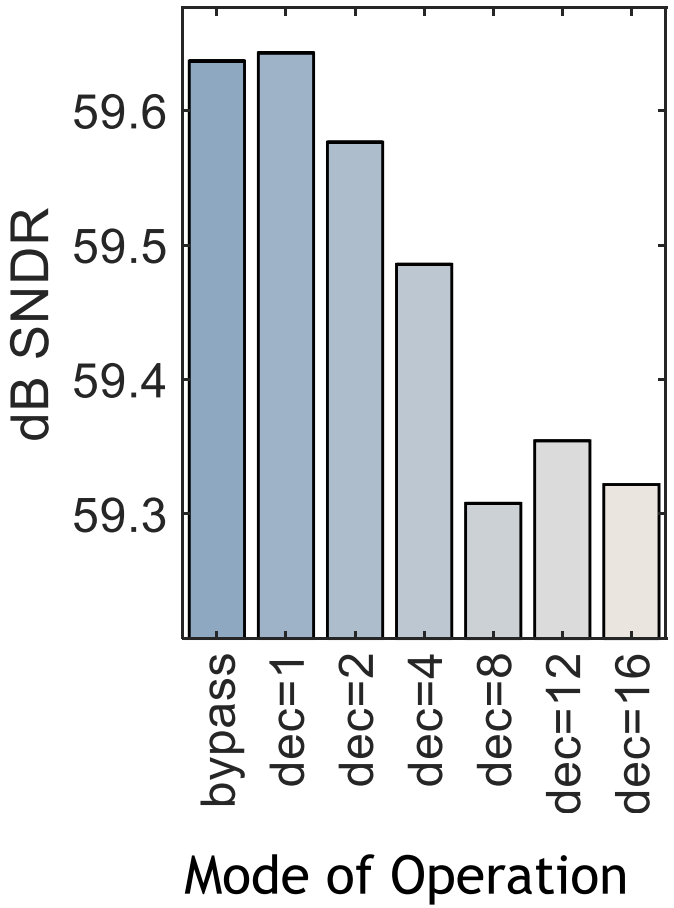
F_{CLK} Sweep: 1MHz – 1GHz



Regulator Performance

- Regulator only 8% of total ADC power
  - Majority of power delivered to load
  - High efficiency
- Decimation of clean regulators improves efficiency
- Minimal impact on noise & SNDR





Performance Summary

- 1GS/s single channel 9.6 ENOB
- Full dynamic reference regulation
- FoM_W 14fJ/c-step from 1MS/s – 1GS/s

Technology	16nm CMOS	
Supply	0.9 V	
Sampling Rate	1MS/s - 1 GS/s	
Resolution	11b	
Input Range	1.6 V pk-pk diff.	
Performance at 1GS/s:	*100 MHz input:*	*500 MHz input:*
ENOB	9.7 b	9.6 b
SNDR	59.8 dB	59.5 dB
SFDR	78.6 dB	75.9 dB
THD	71.8 dB	69.9 dB
Total Power	10.9 mW	
ADC	10.0 mW (92%)	
Regulator	0.9 mW (8%)	
Walden FoM	14.1 fJ/c-step	
Schreier FoM	166.1 dB	
Active Area	0.095 mm^2	

Contributions & Conclusions

- High-Speed Ringamp Topology
  - Elegant operation
- Fully-Dynamic Discrete-Time Reference Regulation
  - Many applications (pipeline, SAR, ...)
  - Any accuracy / noise requirement
- Stochastic ADC “Scope-on-Chip”
  - Small, simple, high resolution, background operation
  - Other interesting applications: e.g. supply and reference diagnostics

Thank you for your attention!