27.2 Ring Amplifiers for Switched-Capacitor Circuits

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To overcome the challenges that CMOS process scaling has imposed on the design of switched-capacitor amplification circuits, designers must consider a growing number of design tradeoffs and employ new circuit techniques in order to achieve required accuracies, often at a cost of added power and complexity. This amplification performance bottleneck has been highlighted in recent years by the disparity in achievable power efficiency between SAR ADCs versus ADC structures that require amplification [1]. In many analog and mixed-signal topics, a comparison like this doesn't even exist, simply because amplification is a necessity. Even SAR ADCs have their limitations, particularly at higher resolutions where matching and noise constraints begin to dominate capacitor sizing and comparator power requirements.

This paper introduces the concept of a Ring Amplifier (alternately: Ring Amp or RAMP), which is ideally suited to perform switched-capacitor amplification at low voltage. Shown in Fig. 27.2.1, the core structure is that of a ring oscillator that has been split into two separate signal paths. A different voltage offset is added to each path, creating an input "dead-zone" for which neither M_{CN} nor M_{CP} will conduct.

Although the basic structure of a ring amplifier is very simple, the mechanisms by which it works are more complex. The basic theory of operation is depicted in Fig. 27.2.2. With a dead-zone of 0mV, the ring amplifier is functionally identical to a 3-inverter ring oscillator. As the dead-zone is increased, plateaus form in the output waveform wherever the dead-zone is crossed and both M_{CN} and M_{CP} are off. During these plateaus, the effective gain (A_{eff}) through the oscillator is zero, and thus the average gain (and frequency of oscillation) is decreased. At some critical dead-zone size this effect reduces the unity-gain bandwidth of the oscillator to below the frequency corresponding to 180° phase delay. Now acting as an amplifier, the structure begins to settle. This settling occurs much faster than in a standard ring oscillator, because the dead-zone continues to provide gain-decreasing feedback by both decreasing the slope of the output slewing and also increasing the proportional time spent in the dead-zone. At some point A_{eff} drops to zero, and the amplifier remains locked into the dead-zone.

The ability to dynamically adjust its gain-bandwidth product enables the ring amplifier to both charge rapidly and then stabilize quickly. Its output stage transistors (M_{CN} and M_{CP}) use only dynamic power when charging the output load with a ramp, similar to the output waveform of a zero-crossing-based circuit [2]. M_{CN} and M_{CP} behave like complementary, digitally switched current sources, leading to a weak correlation between internal power use and dynamic output drive current. This enables high-efficiency charging, particularly for large capacitive loads. Whereas the open-loop nature of a zero-crossing-based circuit creates offset, linearity, noise, and variation issues, ring amplifiers operate in feedback, and do not suffer from these drawbacks, making them uniquely suited to operate in scaled, low-voltage environments. Furthermore, unlike traditional amplifiers, accuracy is determined by the input-referred value of the dead-zone and is independent of output linearity. This allows the ring amp to utilize the entire supply range for output swing, which reduces power on an architectural level by boosting SNR.

Due to the attributes discussed, the ring amplifier is a particularly good candidate to be used as the coarse charging device in the first phase of a Split-CLS amplification scheme [3]. To demonstrate the effectiveness of this pairing, the high-resolution pipelined ADC of Fig. 27.2.3 is presented. The pipeline resolves 15b with 6 MDAC stages and a 3b backend flash. The first four stages employ Split-CLS (and stages 5 and 6 use ring amplifiers only). Two single-ended ring amps are used as the coarse charging device and a telescopic opamp is used as the fine settling device. Due to the fact that the opamp common-mode feedback (CMFB) is applied at the opamp output (and not the stage output), the pseudo-differential ring amplifiers must control the stage output's common-mode voltage. The simple capacitive CMFB network depicted in Fig. 27.2.4 provides an effective solution. The CMFB gain must be several times smaller than the gain of the primary feedback paths, and can be configured by selecting the appropriate capacitor ratio between C_{SIG} and C_{CM}. To further relax the CMFB requirement, the stage 2-6 MDACs employ a 3b pseudo-differential MDAC similar to the 1.5b flip-around MDAC used in [4] (but with a fixed feedback capacitor), allowing the common-mode error to be passed down the pipeline with a gain of 1.

To save power, the ring amps and opamps are only switched on when in use. For the most part, the ring amps are only needed during the coarse charging phase and can be disabled otherwise. However, the voltages stored across capacitors C_{SIG}, C_{DZ1}, and C_{DZ2} of Fig. 27.2.4 must be refreshed periodically. To accomplish this while minimizing power, a digital counter asserts the control signals 'front_enable' and 'refresh' during a fraction of ϕ_S once every N cycles in addition to normal operation (explained in greater detail in Fig. 27.2.4). To reduce opamp power, the stage 1-4 opamps are shut off during ϕ_S and power up at the beginning of ϕ_A, utilizing the time when the ring amps are operating to reach steady state.

The prototype pipelined ADC is fabricated in a 1P4M 0.18µm CMOS process. At 20MHz sampling rate it achieves 76.8dB SNDR (12.5 ENOB), 77.2dB SNR and 95.4dB SFDR, consuming 5.1mW. The ERBW is found to be above 10MHz, which results in a Figure-of-Merit of 45fJ/conv-step. The MDAC references are set at 25mV and 1275mV, allowing the input signal to utilize 96% of the available supply range. Capacitor matching is good enough that no digital calibration is needed. When the sampling frequency is increased to the point that the opamps never have a chance to amplify, the contribution of the ring amps to overall accuracy can be measured, and is found to be 55dB SNDR at f_s = 80MHz.

All analog portions of the circuit operate at 1.3V. Due to an issue in the layout of the bootstrapped input switches, the digital and switch supply is operated above 1.3V, at a cost of additional power. Opamp switching is measured to reduce the total opamp power by 35%.

The ring amplifiers exhibit a high tolerance to variation, as shown in Fig 27.2.5. In the lower-right plot, the dead-zone bias of the ring amps in the 1st-stage MDAC is swept with everything else held constant. The roll-off above +50mV is due to the dead-zone becoming large and reducing accuracy and the roll-off below -50mV is due to the amplifier going unstable. The curve's peak has a systematic offset of roughly -100mV from that seen in simulation, but this does not affect performance. The opamp, via Split-CLS, helps to absorb small errors and further flattens the peak into a wide stable plateau. When the ring amplifier supply voltage is swept with all other voltages and biases held constant (lower-left plot of Fig. 27.2.5), SNDR is virtually unchanged. At 1275mV the supply voltage equals the positive MDAC reference, and explains the roll-off seen below that voltage.

Acknowledgment:
The authors would like to thank Asahi Kasei Microdevices (AKM) for supporting this work and providing fabrication.

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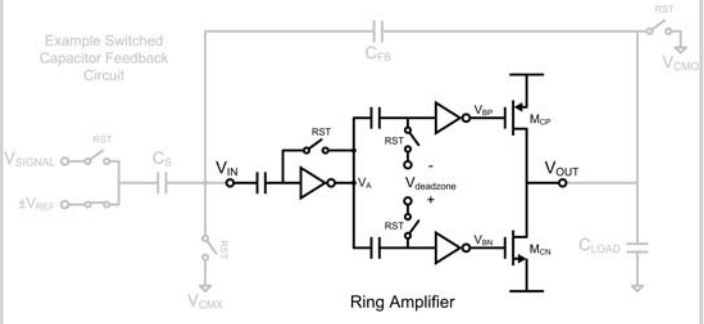

Figure 27.2.1: Fundamental structure of a ring amplifier.

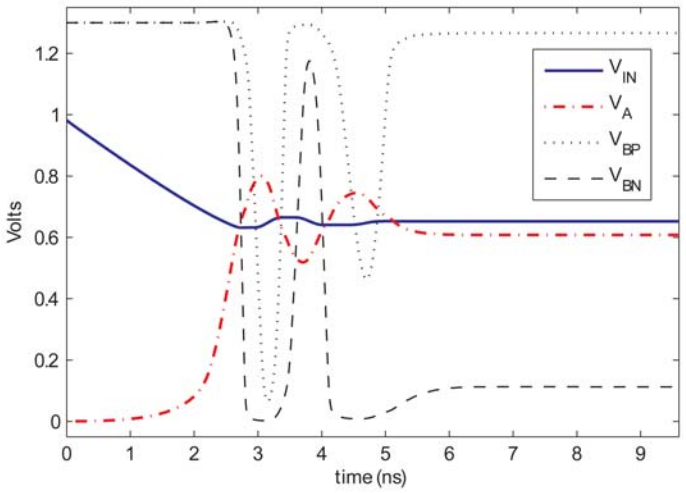

Figure 27.2.2: Settling behavior of Fig. 1 for a typical dead-zone size and charging condition.

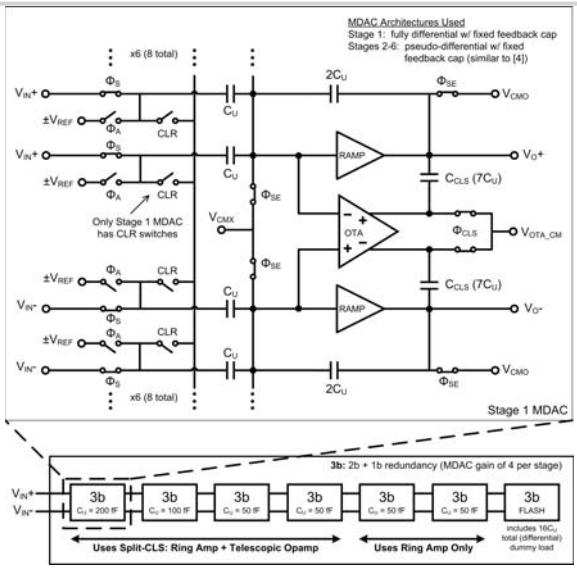

Figure 27.2.3: Split-CLS pipeline ADC structure and first stage MDAC.

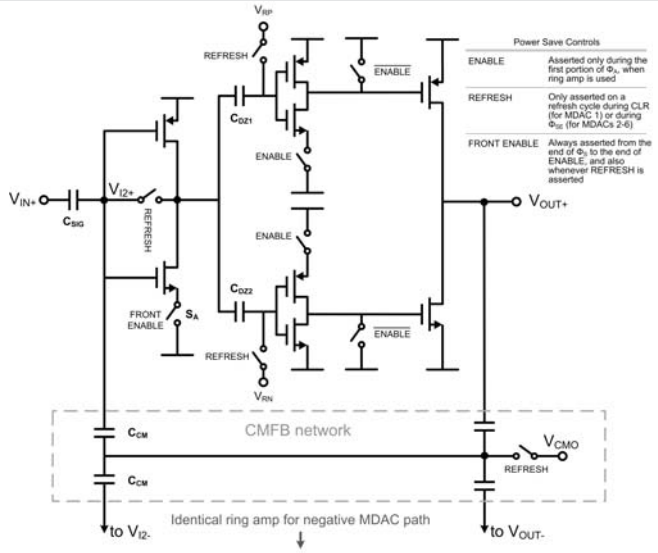

Figure 27.2.4: Ring amplifier with common-mode feedback and power-save features.

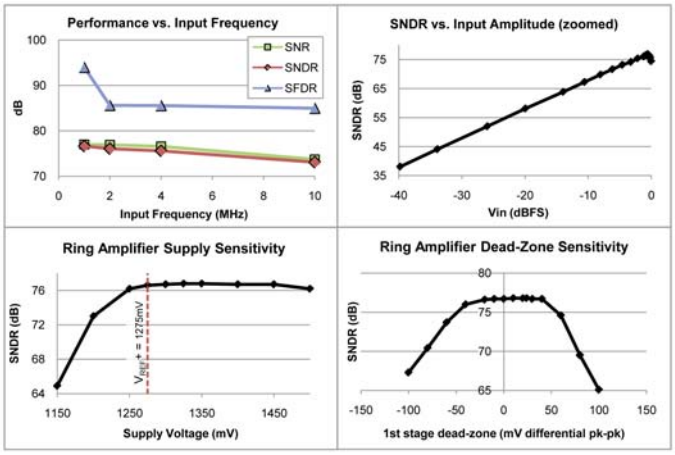

Figure 27.2.5: Input signal characteristics (top) and ring amplifier sensitivity (bottom).

Performance Summary

Resolution	15 bits	Input Range	2.5 V pk-pk diff.
Analog Supply	1.3 V	SNDR	76.8 dB
Sampling rate	20 Msps	SNR	77.2 dB
ERBW	10 MHz	SFDR	95.4 dB
Technology	0.18µm 1P4M CMOS	ENOB	12.5 bits
Active Area	1.98mm^2 (3.05mm x 0.65mm)	Total Power	5.1 mW
		FoM	45 fJ/c-step

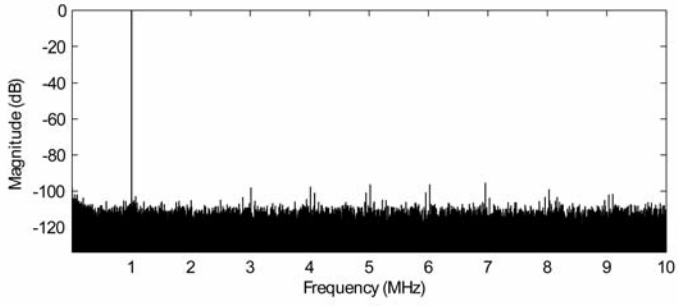

Figure 27.2.6: Summary of key performance metrics and measured output spectrum.

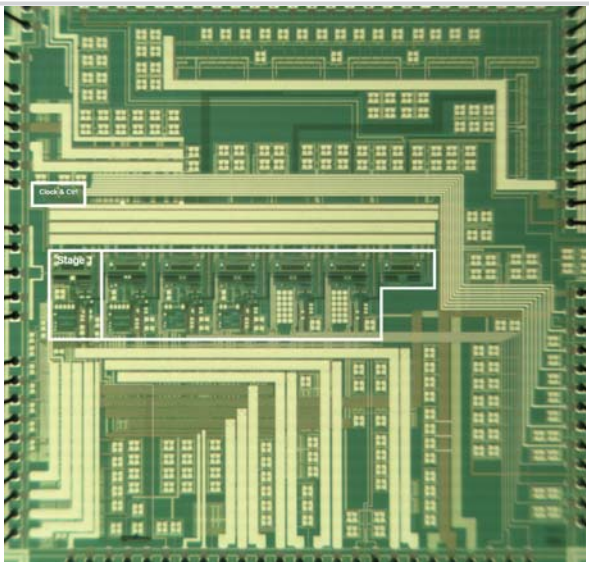

Figure 27.2.7: Chip Micrograph.

978-1-4673-0377-4/12/$31.00