9.7 A Self-Calibrated 10Mb/s Phase Modulator with -37.4dB EVM Based on a 10.1-to-12.4GHz, -246.6dB-FOM, Fractional-N Subsampling PLL

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The two-point injection scheme has proven to be an effective technique for overcoming the problem of PLL bandwidth limitations during wideband polar phase modulation [1]. The quality of the phase-modulated signal, typically expressed in terms of error-vector magnitude (EVM), still remains limited by the PLL phase-noise, gain mismatch between the two injection paths and linearity of the digital-to-modulated phase conversion. We present a phase modulator that makes use of an analog, fractional-N, digital-to-time-converter (DTC)-based subsampling PLL that achieves -37.4dB EVM around a 10.24GHz fractional carrier during 10Mb/s GMSK modulation. The subsampling PLL architecture uses no power-consuming divider and allows wide PLL bandwidth (because of its high phase-error detection gain) for optimal VCO noise suppression. The VCO has a secondary, digitally controlled capacitor bank (modulating DAC) used during two-point modulation. The gain errors and nonlinearities in the digital-to-modulated phase conversion are automatically background-calibrated in both injection points: in the phase-error detection path (where nonlinearity is dominated by the DTC INL) and in the VCO modulating capacitor bank (where nonlinearity is dominated by capacitor mismatch and nonlinear capacitance-to-frequency conversion).

Figure 9.7.1 depicts a block diagram of the presented phase modulator. The system operates as a fractional-N subsampling PLL when there is no modulation [2]. The high-frequency VCO output sinewave is subsampled at the reference rate (40 MHz). The Gm produces a current linearly proportional to the phase difference between reference and VCO phase. That current is steered to the lowpass filter during *Pulser* opening windows [3], which results in appropriate VCO control adjustment. A frequency acquisition loop [2] (not shown in the figure) is implemented for initial locking. A 10b, 0.4ps-step DTC (based on a simple digital delay cell) is transparent during integer multiplication of the input frequency, while, in fractional-N operation mode, it serves for fractional residue compensation i.e. it always forces near-to-zero voltage sampling by dynamically adjusting the delay (phase) of the reference signal [2]. During modulation, the input data is sent through a GMSK modulator that generates a frequency modulation signal for the VCO's modulating DAC (8b, 113 kHz/LSB), inducing appropriate instantaneous frequency shifts. The DTC receives the same modulation signal (expressed in phase) on top of the regular fractional residue compensation signal, to force VCO zero-crossing sampling, letting the unfiltered modulation signal through the loop.

Any kind of gain/nonlinearity presence in the DTC transfer function results in noise folding and fractional spurs during fractional synthesis [4], leading to performance degradation. To overcome this issue, we propose a DTC Gain/INL self-calibration algorithm that pre-distorts the original DTC code to compensate for the unwanted nonlinearities. A similar error-detection calibration structure is used for compensation of the nonlinear modulating DAC, in the second injection path. Notably, since there is no divider in the loop, the intrinsic time mismatch [1] between the two injection points is below 200ps (constant DTC delay), and hence it has negligible effect on the modulation performance.

Details of the INL calibration blocks are shown in Fig. 9.7.2. The calibration is based on *Error Sign* signal observation, which represents the sign of the Gm output current, corresponding to the sign of the instantaneous phase error. This 1b phase error is random and zero on average in a linear system, but in the presence of DTC/DAC INL it becomes "colored" by their respective nonlinearities. Essentially, we exploit the correlation between the *Error Sign* signal and the particular DTC/DAC input code that induced it, to restore the INL curves and pre-compensate for them. A look-up-table (LuT) with a set of coefficients *c(0:k-1)* is used to approximate the 10b DTC/8b DAC INL curve (where k is 32 for DTC and 16 for DAC). In every clock cycle, the input code addresses two neighboring LuT coefficients that piece-wise linearly approximate the expected, instantaneous INL error. The INL compensation value is simply subtracted from the original code, which ideally forces the DTC/DAC to produce no error (zero mean *Error Sign*) for the given code. The LuT correction coefficients are updated gradually, by integrating the scaled *Error Sign* value to the appropriate address (defined with the input code) in every cycle. When the calibration is initialized, the LuT is reset to zero. While the PLL operates, the coefficients *c(0:k-1)* slowly change towards their optimal calibrated values that cancel the INL error. At that moment, the coefficient updating can be disabled. The algorithm convergence speed is determined by the tap gain G, where a typical value of 2^{-15} results in 100ms approximate calibration time. Importantly, the DAC INL calibration uses an additional differentiator on the *Error Sign* (a=1 for DAC, but a=0 for DTC INL calibration) before the application to the LuT. This serves to compensate for the VCO phase integration, i.e. the integration of the error induced by the DAC.

The Gm current sign is extracted by a comparator (Fig. 9.7.1) that exhibits certain input offset. This results in an *Error Sign* signal that is not zero on average, even though the PLL settles into a zero phase-offset condition by definition. Consequently, the DTC INL calibration block receives a corrupted error signal that results in drift of the coefficients *c(0...k-1).* Rather than directing design effort into analog offset cancellation we propose digital calibration (Fig. 9.7.2) in front of the INL calibrations blocks. The operating principle is to periodically overrule the *Error Sign* bit with a fixed high or low value, to bring the average output back to zero. To determine this period, the *Error Sign* is brought to an integrator that ramps with direction related to the offset sign. Its output drives another, overflowing, integrator (after appropriate scaling by $\mu<<1$). The overflow flag is used to address a MUX, steering an artificial *Error Sign* value to the INL calibration algorithm. The value is determined with overflow direction, which is opposite to the offset sign. In this way, the second integrator overflows with frequency proportional to the comparator offset, pseudo-randomly modifying the original *Error Sign* signal, compensating on average for presence of offset.

The prototype IC was fabricated in TSMC 28nm bulk digital CMOS technology, and its size is 0.77mm^2 (excluding IO ring). A die micrograph is shown in Fig. 9.7.7. It operates on 0.9V and 1.8V supplies (IO interface and the Gm stage [2]). To quantify the system performance we report measurements related to both the frequency synthesizer and the phase modulator operation. In frequency-synthesizer mode, the measured power consumption is 5.64mW in total, of which 1.84mW is for the loop components, 2.7mW for the VCO, and 1.1mW for digital circuitry, The VCO tuning range is 10.1 to 12.4GHz**.** The measured in-band phase noise around a close-to-integer fractional 11.72GHz carrier is -107.9dBc/Hz (Fig. 9.7.3). The measured RMS jitter is 198fs after calibration is enabled, with an integration range from 10Hz to 40MHz and all spurs (worst fractional) included. The measured spurious performance is shown in Fig. 9.7.4. The worst fractional spur before calibration appears at -41dBc but drops by 15.6dB after calibration to -56.6dBc. The integer spur is at -69dBc. The PLL achieves a competitive -246.6dB FOM and it is compared to other recent designs in Fig. 9.7.6. During modulation we operate the VCO in high power mode (7.1mA) since the modulating DAC LSB step is then reduced to 113kHz (from the original 241kHz), such that the DAC quantization noise does not limit the EVM. Figure 9.7.5 shows the measured GMSK spectrum and constellation plot, around a fractional carrier close to 10.24GHz. The measured EVM RMS with DTC/DAC calibration is at -37.4dB, which is only 4dB above the total integrated phase noise. The improvement in performance (~4dB) is mainly due to the DTC INL calibration. A comparison to other recently published PLL-based phase modulators is given in Fig. 9.7.6, with a note that this work achieves the best measured EVM results to date.

Acknowledgements:
This work is part of imec's green radio research program sponsored by Hisilicon, Panasonic, Murata, Sony, Cadence and the Flemish HERCULES project VeRONICa. Authors thank IWT, Flanders, Belgium for support and acknowledge Jorgo Tsouhlarakis for valuable contributions with digital circuitry implementation.

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 978-1-4673-9467-3/16/$31.00

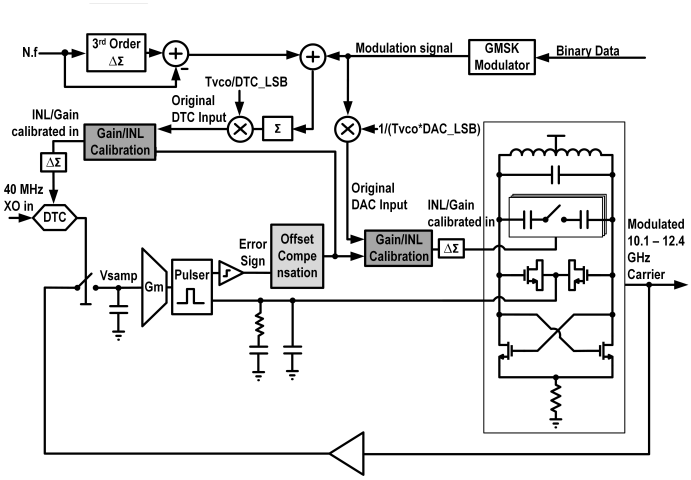

Figure 9.7.1: Complete system block diagram showing the Fractional-N subsampling PLL with modulation capabilities.

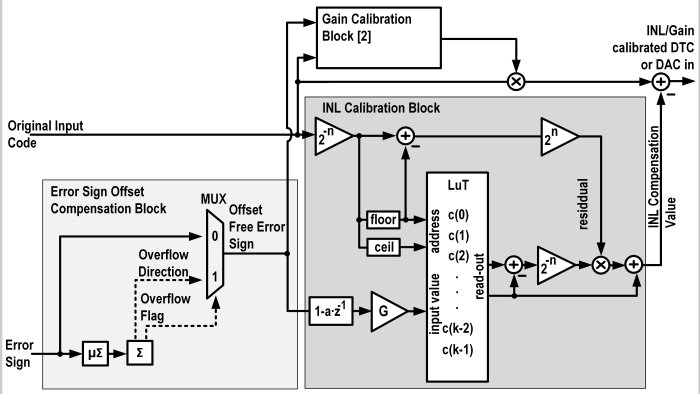

Figure 9.7.2: Details of the Offset Compensation and INL Calibration Block. The gain calibration block was reused from a previous design [2].

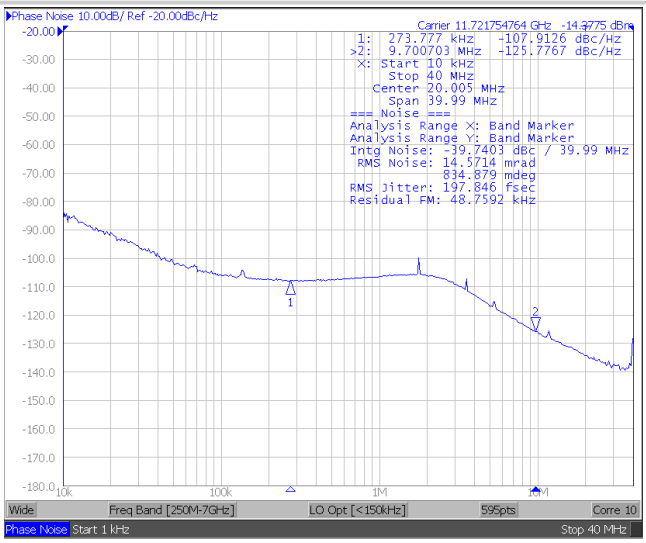

Figure 9.7.3: PLL output spectrum. The RMS jitter integration range is 10kHz to 40MHz and includes all spurs (worst fractional).

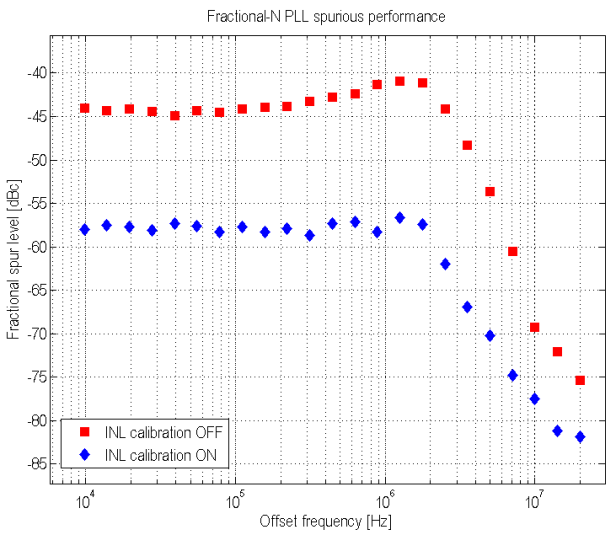

Figure 9.7.4: Fractional spur with and without calibration at different fractional offsets.

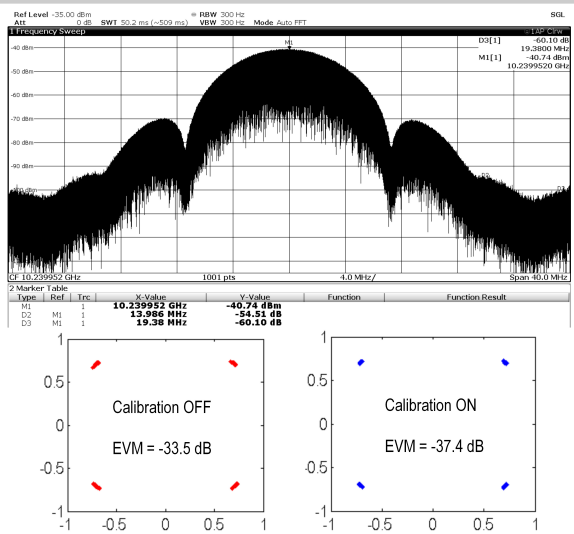

Figure 9.7.5: GMSK spectrum and EVM after DTC/DAC INL calibration (10Mb/s, close to a 10.24GHz fractional carrier).

PLL Comparison	This work	Chen ISSCC'15	Huang ISSCC'14	Gao ISSCC'15
Architecture	Subsamp. Analog	Subsamp. Digital	Subsamp. Analog	TDC-based Digital
Reference (MHz)	40	49.15	48	40
Output (GHz)	10.1-12.4	2.6-3.9	2.2-2.9	5.82 GHz
Tuning range (%)	20.4	40	27.4	N.A.
Bandwidth (kHz)	1800	700	500	500[3]
In-band PN[1] (dBc/Hz)	-107.9	-97.2	-97.9	-105.9
Ref. spur (dBc)	-69	-60	-55	-76
Frac. spur (dBc)	-56.6	-62	-53	N.A.
RMS jitter (fs)	176/198 (10k-40M)	226/240 (1k-100M)	400/266 (10k-30M)	174 (10k-10M)
Power (mW)	5.6	11.5	17.3	9.5
FoM[2] (dB)	-247.6/-246.6	-241.8	-235.6/-239.1	-245.5
Area (mm²)	0.77	0.23	0.75	0.3
Process (nm)	28	65	180	28

Modulator Comparison	This work	Marzin JSSC'12	Xu JSSC'14	Shanan ISSCC'09
Architecture	Direct-FM Two-point	Direct-FM Two-point	Direct-FM Two-point	Direct-FM Pre-distort.
Reference (MHz)	40	40	26	52
Output (GHz)	10.1-12.4	2.9-4.0	1.7-2.1	2.4
Modulation type	GMSK	GMSK	GMSK	GMSK
Max. data rate (Mb/s)	10	10	10.83	2
Energy/bit (nJ/bit)	0.81	0.5	0.64	8
EVM RMS (dB)[4]	-37.4	-26.9	-13.9	-5.4
Phase noise (dBc)[4]	-41.7	-29.9	N.A.	N.A.
Out of band emission (dBr)	-55	-56	N.A.	-57
Power	8.1	5	6.9	16
Area (mm²)	0.77	0.5	0.49	1.1
Process (nm)	28	65	65	180

[1] Scaled to 11.72 GHz.
[2] $\mathrm{FoM} = 10\log\left(\frac{\mathrm{jitter}^2}{1\mathrm{s}^2}\frac{\mathrm{power}}{1\mathrm{mW}}\right)$.
[3] Estimated from source analyzer measurement.
[4] Scaled to 10.24 GHz.

Figure 9.7.6: State-of-the-art comparison table with recently published PLLs (left) and PLL-based phase modulators (right).

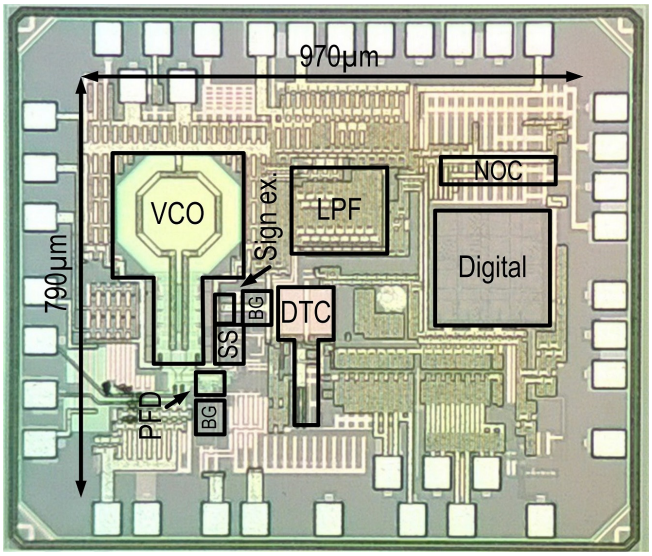

Figure 9.7.7: Die micrograph.

978-1-4673-9467-3/16/$31.00