A 1Gsps, 12-bit, Single-channel Pipelined ADC with Dead-zone-degenerated Ring Amplifiers

Jorge Lagos[1,2], Benjamin Hershberg[1], Ewout Martens[1], Piet Wambacq[1,2], and Jan Craninckx[1]
[1]imec, Leuven, Belgium
[2]Vrije Universiteit Brussel, Dept. of Electronics and Informatics, Brussels, Belgium

***Abstract*—The design of power-efficient ADCs able to achieve both high linearity and bandwidth in deep nanoscale CMOS processes becomes very challenging as the constraints of low-voltage operation and limited intrinsic gain often mandate the use of power-consuming analog circuits and digital calibration. This work introduces a pipelined ADC that leverages the low but very flat open-loop gain vs. output swing characteristic of the ring amplifier (ringamp) to address these problems. A 12-bit, 1Gsps, single-channel prototype is implemented in a 28nm planar CMOS process achieving 56.6dB SNDR and 73.1dB SFDR. Consuming 24.8mW from a single 0.9V supply, it achieves Schreier and Walden FoMs of 159.6dB and 45fJ/conv.-step, respectively.**

Keywords—Pipelined ADC, ring amplifier, ringamp, single-channel, dead-zone degeneration, gain calibration.

I. Introduction

In the context of high-linearity and high bandwidth ADCs, the use of pipelining is a popular choice, as it allows information to be broken down into smaller increments that can be processed faster, at the cost of added latency. However, the residue amplification step required by this technique often imposes a limit on the power efficiency that can be achieved, as tough speed and linearity specifications often translate into the use of power-hungry amplifiers operating at high supply voltages. Moreover, when the required speed exceeds what is achievable with a single channel, time interleaving must be used, which comes at the expense of calibration complexity and corresponding power efficiency. As illustrated in Fig. 1, most high-performance converters reported to date rely on pipelining and time interleaving, and only a few single channel implementations reach this performance region [1]. Moreover, approaching the upper boundary of speed, the power efficiency of these single channel ADCs tends to be heavily penalized. Thus, the maximization of per-channel speed and linearity, along with the minimization of power consumption, is of paramount importance for the implementation of power-efficient, high-performance ADCs that can meet the demanding specifications of next-generation communication applications.

In [2] it was shown that ring amplification [3] combined with 1st-order gain calibration can provide a power-effective solution for achieving high-speed and linearity in nanoscale CMOS by exploiting the flatness properties of the ringamp open-loop gain even when intrinsic device gain is severely limited. Here we extend this concept further by introducing a new ring amplifier with increased linearity and speed, based on the concepts of dead-zone degeneration and 2nd-stage bias enhancement. Using

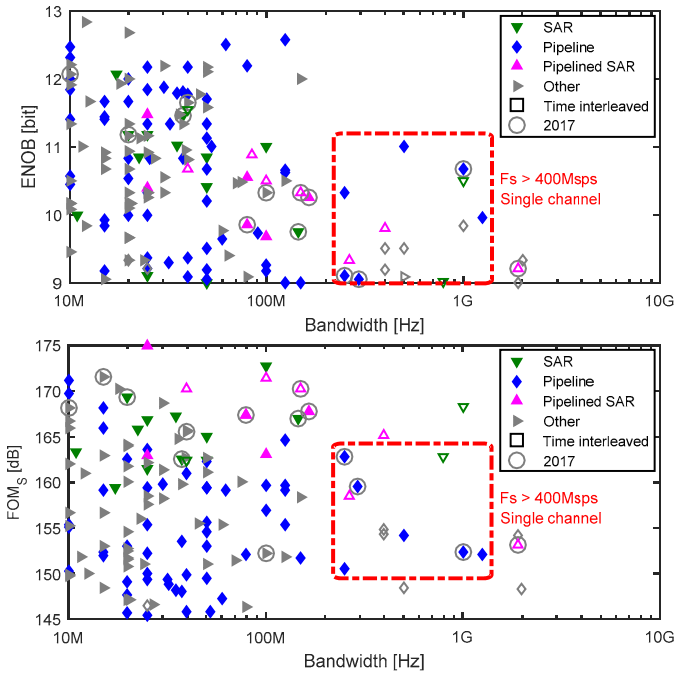

Fig. 1. Effective number of bits and Schreier FoM vs. bandwidth for ADCs published in the last 20 years (with ENOB>9bit) [1].

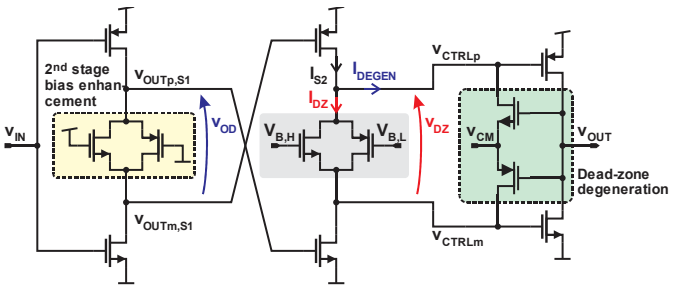

Fig. 2. Proposed ring amplifier featuring dead-zone degeneration and 2nd-stage bias enhancement.

these techniques, the implemented ADC achieves the highest speed reported to date for ringamp-based converters, and the best power efficiency reported to date among all single-channel ADCs with greater than 9ENOB and higher than 800Msps.

This paper is organized as follows. Section II introduces the proposed ringamp and its associated techniques. Section III describes the ADC implementation. The measured results are reported in Section IV. Finally, Section V concludes the paper.

978-1-5386-2483-8/18/$31.00 ©2018 IEEE

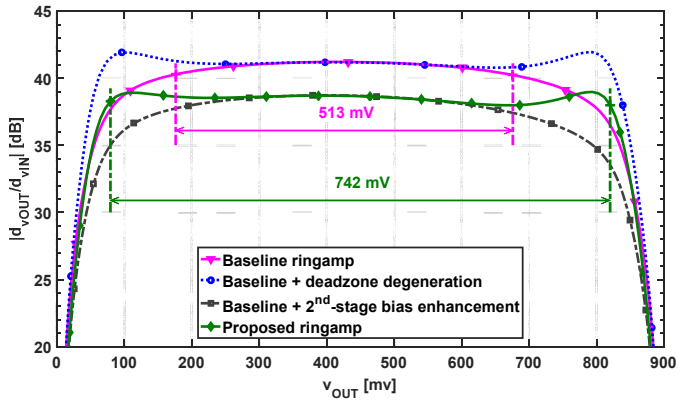

Fig. 3. Simulated effects of dead-zone degeneration and 2nd-stage bias enhancement in the open-loop gain vs. output swing characteristic.

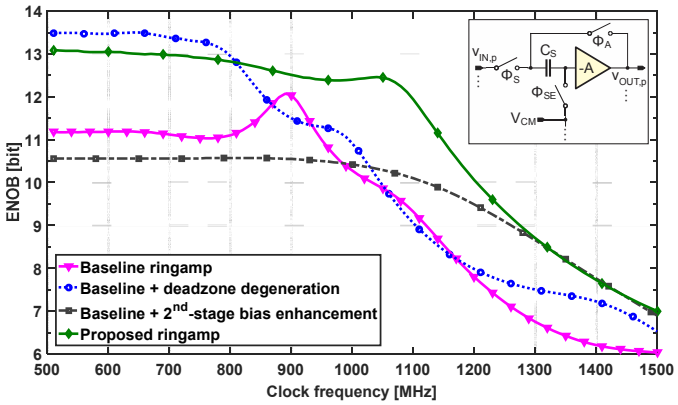

Fig. 4. Simulated linearity vs. clock frequency for a differential unity-gain SHA using the amplifiers showcased in Fig. 3 (1.6Vpp input signal).

II. Proposed Ring Amplifier

Fig. 2 shows the structure of the ringamp introduced in this work. It is based on the CMOS-resistor self-biased implementation of [2] (henceforth referred-to as the *baseline ringamp*) with two key modifications, as discussed below.

A. Open-loop gain flattening through dead-zone degeneration

In order to maximize the linearity that can be recovered from a residue amplifier through 1st-order gain calibration, it is desirable to have an open-loop gain vs. output swing profile that is as flat as possible [2]. To this end, the proposed ringamp introduces the concept of dead-zone degeneration, which is implemented by 2 feedback transistors between the 3rd and 2nd stages, as shown in Fig. 2. When the output voltage is close to mid-rail, these degeneration devices are off and the operation is as in the original baseline ringamp. However, whenever the output departs towards the supply boundaries, the degeneration devices start to turn on, drawing a current I_{DEGEN} from the 2nd stage. As a result, the current $I_{DZ}=I_{S2}-I_{DEGEN}$ flowing through the 2nd stage CMOS resistor is decreased and this reduces the magnitude of the dead-zone voltage V_{DZ}. Crucially, this dead-zone collapse happens in an asymmetric manner: when the output is high the upper portion of the dead-zone collapses, and when the output is low the lower portion collapses. This introduces an output-voltage dependent offset into the ringamp that the feedback loop will suppress by adding a small offset at the ringamp input. The sign of this offset will be opposite with respect to the sign of the error due to both finite gain and gain compression. That is to say,

$$V_{IN} = \frac{V_{OUT}}{A_{OL}} + f_{\varepsilon\_cmpr}(V_{OUT}) - f_{\varepsilon\_dz}(V_{OUT})$$

where V_{IN} and V_{OUT} are the input and output voltages of the ringamp in feedback, A_{OL} is the nominal ringamp open loop gain, $f_{\varepsilon\_cmpr}(V_{OUT})$ is the input referred error due to signal dependent gain variation and $f_{\varepsilon\_dz}(V_{OUT})$ is the intentionally created input referred error term due to dead-zone degeneration. Clearly, when $f_{\varepsilon\_cmpr}(V_{OUT}) = f_{\varepsilon\_dz}(V_{OUT})$, the two terms cancel and the finite gain in the system becomes entirely 1st order. Interestingly, even though $f_{\varepsilon\_cmpr}(V_{OUT})$ is related to an AC small signal gain whereas $f_{\varepsilon\_dz}(V_{OUT})$ is related to an embedded DC offset mechanism, due to the fact that both are a function of V_{OUT} and ultimately manifest as voltage errors in the system, one can be used to cancel the other. Although such perfect cancellation is not practical to realize, when sized properly, the degeneration devices can be used to partially cancel the gain compression error function in this manner, resulting in a much flatter gain vs. output swing characteristic. This is illustrated in Fig. 3. The top two traces in the figure show the simulated open-loop gain vs. output swing characteristic for the baseline ringamp with and without dead-zone degeneration. The output swing range lying within the 1dB compression points is expanded by more than 200mV.

In Fig. 4, the ringamp is simulated in an ideal SC unity-gain SHA and the linearity is analyzed with respect to operating frequency. Although dead-zone degeneration has little effect on speed, it significantly improves linearity. At lower frequencies, we can see that compression cancellation boosts linearity by more than 14dB and rolls off at higher frequencies due to incomplete settling in a manner similar to the baseline case.

B. 2nd-stage bias enhancement

Within the context of pipelined ADCs, the maximum operating frequency is often limited by incomplete settling errors of the residue amplifiers. In ringamps, as was independently discovered in [4], this speed limitation can be improved by boosting the overdrive of the 2nd stage. As shown in Fig. 2, in the proposed implementation this is done by adding an additional CMOS resistor in the 1st stage to create a voltage drop V_{OD} which is used to drive the 2nd stage devices with higher V_{GS} and thus higher overdrive. Consequentially, the poles at the output of the 2nd stage are shifted towards higher frequencies. This results in a higher overall phase margin due to the increased separation between these non-dominant poles and the dominant pole at the output. This, however, comes at the expense of a slightly lower gain in the 1st and 2nd stages of the ringamp. These effects are clearly seen in Fig. 4: the peak linearity of the baseline ringamp with 2nd-stage bias enhancement is extended to higher frequencies, despite an overall 3dB degradation in peak linearity. As shown in Fig. 3, this degradation is constant across output swing, and the gain profile with 2nd-stage bias enhancement exhibits the same 1dB compression behavior as the baseline ringamp. Fig. 3 shows that this is also true if 2nd-stage bias enhancement is applied to a ringamp with dead-zone degeneration, as is the case in the proposed ringamp.

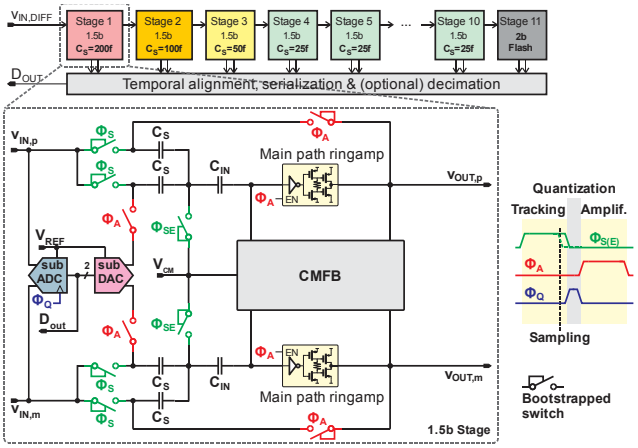

Fig. 5. ADC architecture and structure of each 1.5bit pipeline stage.

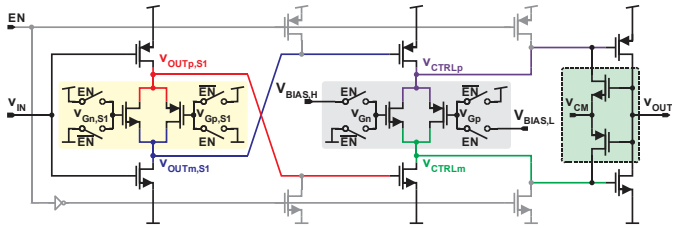

Fig. 6. Detailed structure of the proposed ringamp.

C. *Combined effects of dead-zone degeneration and 2nd-stage bias enhancement*

The two previously described techniques can be combined to simultaneously achieve high speed and linearity. As seen in Fig. 4, when using both techniques, a 2.5dB loss in linearity due to bias enhancement subtracts from the 14dB boost due to degeneration, resulting in a net improvement of 11.5dB in linearity while at the same time improving speed significantly. When used together, in conjunction with 1st-order gain calibration, the proposed ringamp can achieve greater than 12b linearity and beyond 1Gsps in 28nm CMOS. Considering that 28nm planar CMOS is one of the most challenging technologies for achieving high gain and linearity, this work demonstrates the capability of ringamps to cover a broad range of design targets for speed and linearity in any nanoscale technology.

III. ADC Implementation

The architecture of the ADC is depicted in Fig. 5. It is a pipeline composed of 10 1.5-bit stages (to maximize speed) followed by a 2-bit back-end flash. The digital reconstruction and gain calibration are implemented off-chip. The stages are scaled down three times by a factor of 2 to save power. The structure of each stage is also shown in Fig. 5. It is based on the flip-around MDAC with ringamp-based CMFB described in [2]. The actual implementation of the proposed ring amplifier used in the signal path is detailed in Fig. 6. The CMOS resistors implementing the dead-zone degeneration and the 2nd stage bias enhancement are gated so that the full ringamp can be easily powered-down, providing a signal-independent idle state when the ringamp is not used. In order to maximize overdrives and slewing power, and to minimize parasitics, all the transistors are ultra-low-VT devices with minimum channel length.

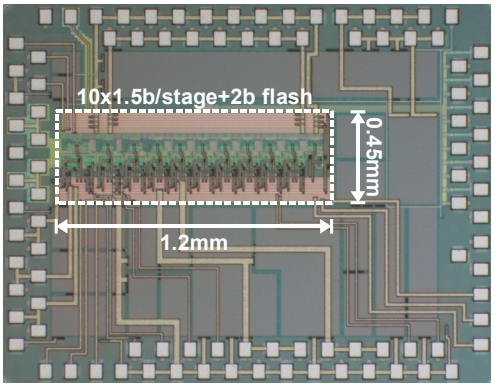

Fig. 7. Chip micrograph.

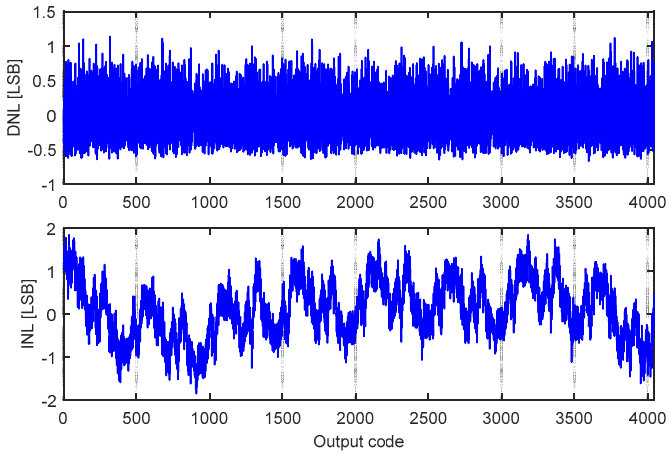

Fig. 8. Measured differential and integral non-linearities (12b quantization).

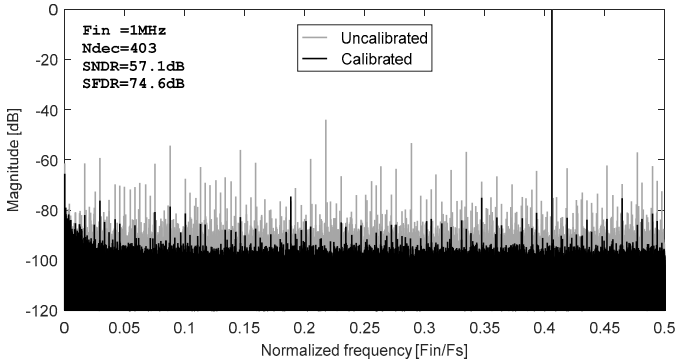

Fig. 9. Measured output spectrum for a 1MHz input at 1Gsps (32Kpts FFT).

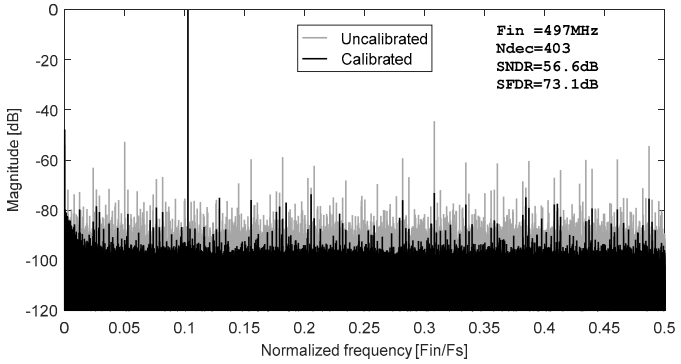

Fig. 10. Measured output spectrum for a Nyquist input at 1Gsps (32Kpts FFT).

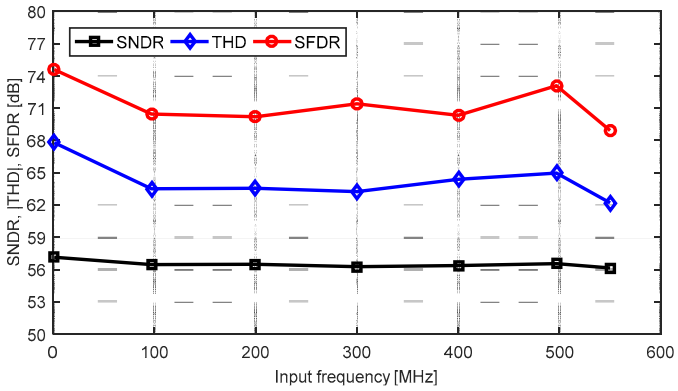

Fig. 11. Measured performance at 1Gsps for variable input signal frequency.

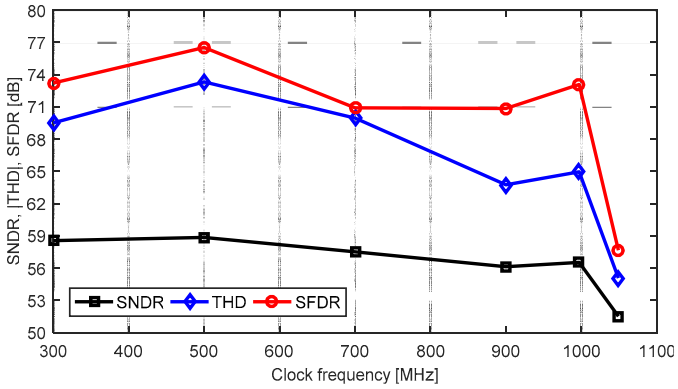

Fig. 12. Measured performance for variable clock frequency and Nyquist input.

IV. Measurement Results

A prototype ADC was fabricated in a 1P9M 28nm standard CMOS process, occupying a core active area of 1.2x0.45mm^2, shown in Fig. 7. The measured static linearity is detailed in Fig. 8. The achieved DNL and INL are 1.85LSB and 1.14LSB with a full-scale input of 1.6Vpp. Figures 9 and 10 show the measured decimated spectrums at 1Gsps with low- and Nyquist frequency inputs, respectively. The effectiveness of the ringamp gain linearization is apparent from these figures, where a SFDR in excess of 70dB is achieved after a simple 1st-order stage gain calibration. The dynamic behavior with respect to input signal and clock frequencies is reported in Figures 11 and 12, respectively. The ADC exhibits greater than 500MHz ERBW and operates up to 1Gsps, after which the performance degrades due to incomplete settling.

At 1Gsps the ADC consumes 24.8mW operating entirely on a 0.9V supply, which translates into Schreier and Walden FoMs of 159.6dB and 45fJ/conv.-step, respectively. Table I summarizes the measured performance and compares it against other state-of-the-art single-channel ADCs. As illustrated by the FoM plots in Fig. 13, this work constitutes not only the highest-speed ringamp-based ADC reported to date but also the most power efficient implementation among all single-channel ADCs of any architecture with at least 800Msps and greater than 9ENOB, showing the potential for extending this work to achieve power-efficient multi-Gsps implementations using time interleaving techniques.

TABLE I. Peformance summary & state of the art Comparison

		This work	VLSIC'17 J. Lagos	VLSI'17 K.-J. Moon	ISSCC'17 H. Shibata	VLSIC'16 A.M. Ali	ISSCC'15 El-Chammas	ISSCC'14 A.M. Ali
Architecture		**Pipeline**	Pipeline	Pipe-SAR	CT Pipe.	Pipeline	Pipeline	Pipeline
Residue amplifier		**Ringamp**	Ringamp	Gm cell	Opamp	Opamp	Opamp	Opamp
Resolution [bit]		**12**	12	10	-	14	14	14
Technology [m]		**28n**	28n	28n	28n	28n	180n SiGe	65n
Supplies [V]		**0.9**	0.9	1.0	1.8/±1.0	2.5/1.8/0.9	3.3/1.8	3.3/2.5/1.2
Input range [Vpp]		**1.6**	1.6	-	2.0	1.3	2.5	2.0
Sampling rate [sps]		**1G**	**600M**	**500M**	**9G**	**2.5G**	**500M**	**1G**
ERBW [Hz]		**>500M**	350M	-	1.125G	1.5G	700M	1G
ENOB [bit]	LF input	**9.2**	9.4	9.1	-	10.3	10.5	11.2
	Nyquist	**9.1**	9.1	9.1	10.7	10.0	10.3	11.0
SNDR [dB]	LF input	**57.1**	58.1	56.7	-	64	64.8	69
	Nyquist	**56.6**	56.3	56.6	66	61.7	64	68
SFDR [dB]	**LF input**	**74.6**	**67.5**	**73**	**79**	**80**	**93**	**86**
	Nyquist	**73.1**	**69.2**	**69.2**	**79**	**73**	**82**	**82**
Power [W]		**24.8m**	**14.2m**	**6m**	**2330m**	**1150m**	**550m**	**1200m**
FoM_{Walden} [J/c.step]		**45f**	44.3f	22f	715f	463f	849f	585f
$FoM_{Schreier}$ [dB]		**159.6**	159.5	162.8	152.3	152.1	150.6	154.2
Core area [mm2]		**0.54**	0.62	0.015	5.1	-	2.5	18
Gain calibration		**1st order**	1st order	1st order	>1st order	>1st order	No	>1st order

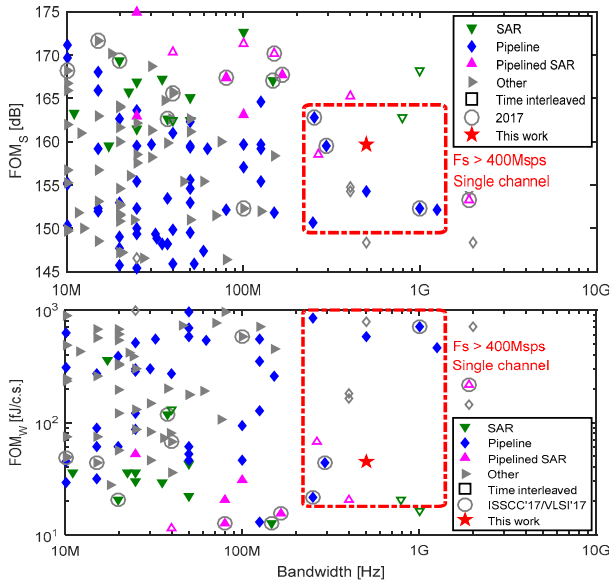

Fig. 13. Schreier & Walden FoM comparison for ADCs with >9ENOB [1].

V. Conclusion

The effectiveness of a new ringamp architecture that exploits dead-zone degeneration and 2nd-stage bias enhancement for simultaneously achieving high linearity and bandwidth with high power efficiency has been demonstrated. These two techniques can be combined with little interdependence effects to either improve linearity or bandwidth. A combination of both allowed the implemented design to push the power-efficiency state-of-the-art for high-performance, single-channel ADCs.

VI. References

[1] B. Murmann, "ADC Performance Survey 1997-2017," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

[2] J. Lagos, et al., "A single-channel, 600msps, 12bit, ringamp-based pipelined adc in 28nm cmos," in IEEE Symp. VLSI Circuits Dig. Tech.

[3] B. Hershberg et al., "Ring amplifiers for switched capacitor circuits," IEEE J. Solid-State Circuits, vol. 47, no. 12, pp. 2928–2942, Dec 2012.

[4] Y. Chen et al., "A 200ms/s, 11 bit sar-assisted pipeline adc with biasenhanced ring amplifier," in 2017 IEEE International Symposium on Circuits and Systems (ISCAS), May 2017, pp. 1–4.