A 69-dB SNDR 300-MS/s Two-Time Interleaved Pipelined SAR ADC in 16-nm CMOS FinFET With Capacitive Reference Stabilization

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***Abstract*— A two-time interleaved pipelined SAR ADC in 16-nm CMOS achieving 11.2-bit ENOB at 300 MS/s is presented. To cancel the signal-dependent voltage ripple on the reference node due to DAC switching, it employs a stabilization scheme based on the use of auxiliary DACs. The charge drawn from the reference becomes signal-independent, greatly reducing the requirements for the reference decoupling capacitance and/or buffers. The technique improves the linearity to levels better than 76-dB harmonic distortion. Power consumption is only 3.6 mW resulting in peak FoMs of 175.5 dB and 5.1 fJ/conv.step.**

***Index Terms*— ADC, FinFET technology, pipelined SAR ADC, reference pre-charging, reference ripple, reference stabilization.**

I. Introduction

NEW wireless applications, like Internet-of-Things, autonomous cars, massive machine communication, or augmented reality, continuously demand higher data rates requiring wireless receivers capable of processing channels with high bandwidths. Even for smaller channel bandwidths, technology scaling dictates that it is beneficial to digitize the signal early in the receive chain. These trends drive the interest in low-power ADCs with speeds of a few hundreds of MHz and accuracies of 10–12 effective number of bits. For these specifications, a hybrid solution based on a capacitive SAR architecture combined with pipelining and interleaving is an efficient choice [1].

This efficiency, however, comes at the cost of strict requirements for the surrounding circuitry like the input driver and the reference voltage. During tracking and sampling, the input driver should deliver a linear amount of charge to the capacitive DAC. To generate the residues during the SAR conversion, the DAC draws a *signal-dependent* charge from the reference node on which a stable voltage must be maintained [2]. Any signal-dependent variation of the voltage on this node modulates the reference voltage, which appears as harmonic distortion at the output of the ADC [3].

This paper explores a technique based on the use of auxiliary DACs to stabilize the voltage on the reference node without sacrificing the power efficiency of the interleaved pipelined SAR architecture, or a significant increase of the area cost. The technique has been implemented in a 16-nm ADC achieving 11.2-bit ENOB at 300 MS/s [4]. Whereas this accuracy is similar to the work presented in [5], it avoids the use of large on-chip decoupling capacitance.

This paper is organized as follows. Section II gives a brief overview of conventional reference stabilization techniques found in the literature. In Section III, the capacitive reference stabilization technique used in this paper is analyzed. The architecture of the ADC and details about its subcircuits are presented in Section IV. An overview of the calibration techniques applied in this design is given in Section V. Measurement results of our prototype are summarized in Section VI. Finally, conclusions are drawn in Section VII.

II. Reference Stabilization Techniques

SAR-based ADCs are most vulnerable to errors due to non-ideal reference voltages when combining high speed with high accuracy. With a low conversion speed, there is enough time to wait for the reference voltage to settle back to its nominal value after switching the DAC before comparison or amplification. An ADC of limited accuracy only needs a small DAC which consequently draws not much charge from the reference node, and larger errors can be tolerated. In this paper, we target more than 11-bit ENOB for sampling speeds up to 300 MS/s, and a technique to reduce the ripple on the reference node becomes imperative.

To stabilize the reference voltage, several techniques have been developed. A first conventional approach is adding a large decoupling capacitance at the cost of a large area. For example, 1 nF (taking up an area more than twice the area of the core ADC) is needed for the interleaved pipelined SAR ADC of [5] to achieve more than 11 ENOB at 200 MS/s.

Another typical approach is to use a reference buffer. This buffer needs a low output impedance to be able to provide high-frequency currents to charge the DAC when a residue is generated. These requirements typically result in a considerable power consumption [6], [7], e.g., 3.2 mW in [8] for 10 ENOB at 800 MS/s, 6.6 mW in [9] for 9.9 ENOB at 600 MS/s, and 7.3 mW in [10] for 12.7 ENOB at 40 MS/s.

Alternative DAC switching schemes can be adopted to relax the requirements on the reference buffer. For example, a sub-radix-2 adds redundancy allowing the buffer to recover from settling errors of the reference voltage [3]. However, this requires extra SAR cycles, which reduce the conversion speed.

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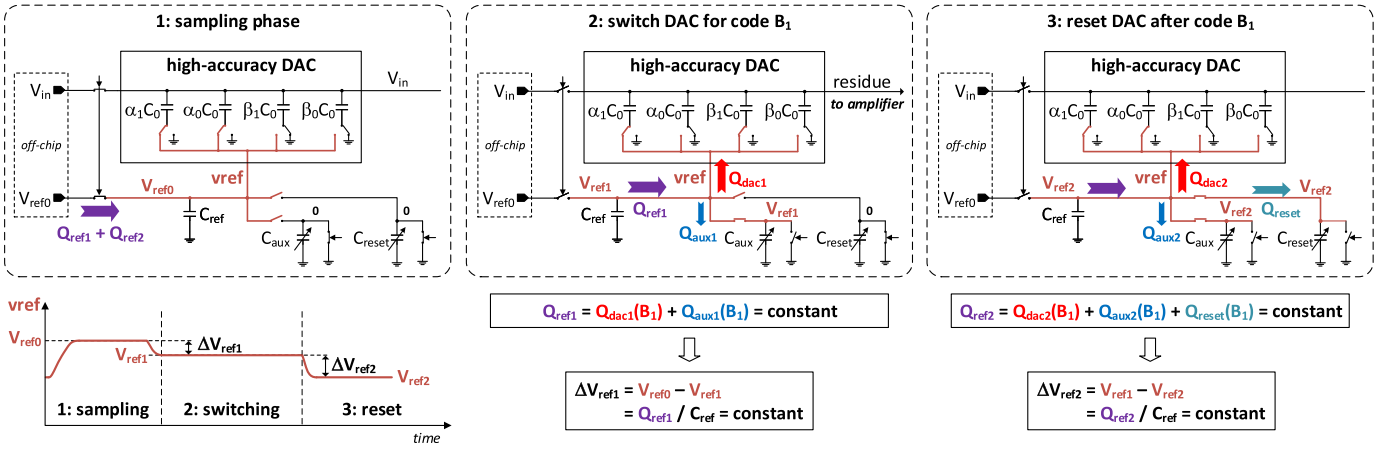

Fig. 1. Basic principle for canceling voltage ripple on reference node using the auxiliary capacitors C_{aux} and C_{reset} during switching the DAC for generating a residue and resetting the DAC back to its sampling state.

Switching schemes that reduce the signal-dependent charge drawn by the DAC can be adopted [11], [12], but they increase the design complexity.

Another approach is to pre-charge a charge reservoir, so that all charge needed for the conversion is acquired before the conversion begins, which makes the ADC more immune to ripple on the reference node [13]. Charge-sharing architectures use different pre-charged reference capacitors and reconnect them to the DAC to generate the residues making these architectures more immune to ripple on the reference node. Examples are [14] for 7.8 ENOB at 20 MS/s, [15] for 9.8 ENOB at 600 MS/s, and [16] for 13.2 ENOB at 1 MS/s. By resetting the reference capacitors before pre-charging, reference pre-charging becomes signal-independent [6]. Compared with the conventional charge-redistribution DAC, most of these architectures suffer from extra signal attenuation and are more vulnerable to non-idealities of the switches, e.g., signal-dependent charge injection and leakage.

Digital correction of analog reference errors is also a possibility. By adjusting the weights used to combine the ADC's output bits, errors can be compensated in the digital domain similar to capacitor mismatch [17]. However, reference errors due to incomplete settling are more sensitive to PVT variations than capacitor mismatches. In [18], reference errors are detected in extra comparison cycles, and a signal-dependent offset is compensated in digital domain achieving 9.7 ENOB at 100 MS/s.

In this paper, we follow yet another approach, whereby the charge drawn from the reference is directly replenished by an auxiliary charge source. In [19], it is shown how a properly sized auxiliary DAC can be switched concurrently with the main DAC to do an approximate cancellation of charge drawn from a buffered reference, thereby reducing the buffer's requirements. This charge neutralization technique achieves 8.8 ENOB at 1.6 GS/s. In this paper, we take the concept a step further and introduce a solution that fully neutralizes the charge to high precision so that the buffer's requirements are even further reduced. Background calibration allows it to maintain high accuracy at high sampling speeds independent of parasitics, mismatches, and slow-varying PVT conditions.

III. Capacitive Reference Stabilization

A. Basic Principle

The basic concept of the capacitive reference stabilization technique used in this paper is to cancel the signal-dependent ripple on the reference voltage due to DAC switching by ensuring that the charge drawn from the reference becomes code-independent. This principle is shown in Fig. 1, where a high-accuracy DAC is used to generate the residue corresponding to a digital code B_1.

First, the nominal reference voltage V_{ref0} is sampled onto a charge reservoir C_{ref} [13], while the input signal V_{in} is sampled onto the top plate of the DAC. The operation of a general charge-redistribution DAC can be described by defining four groups of DAC units, as shown in Fig. 1. The α_1 and α_0 units are connected via their bottoms plates to the reference node and the β_1 and β_0 units are grounded in the sampling phase. Only the units α_0 and β_1 will be switched to generate the residue. Note that the DAC code determines how many units are in each of the groups. Our implementation splits the DAC in two sub-DACs α and β corresponding to the positive and negative parts of the input ranges. Also, in the sampling phase, the auxiliary capacitors C_{aux} and C_{reset} are completely discharged.

In the second phase, the bottom plates of the DAC units are switched ($\alpha_0 C_0$ to ground and $\beta_1 C_0$ to the reference node), which require a charge Q_{dac1}. Meanwhile, C_{aux} is also connected to the reference node so that an extra charge Q_{aux1} is drawn from C_{ref}. As a result, the voltage on the reference node drops to a level V_{ref1}, as shown by the voltage diagram of Fig. 1, with

$$V_{\text{ref1}} = V_{\text{ref0}} - \frac{Q_{\text{dac1}}(B_1) + Q_{\text{aux1}}(B_1)}{C_{\text{ref}}}. \tag{1}$$

By selecting the appropriate value for C_{aux} per code B_1, the sum of the charge drawn by the DAC and Q_{aux1} is made constant over all DAC codes. As a result, the reference voltage drops to V_{ref1} independent of the DAC code B_1, eliminating any signal-dependent ripple on the reference voltage and greatly improving the harmonic distortion.

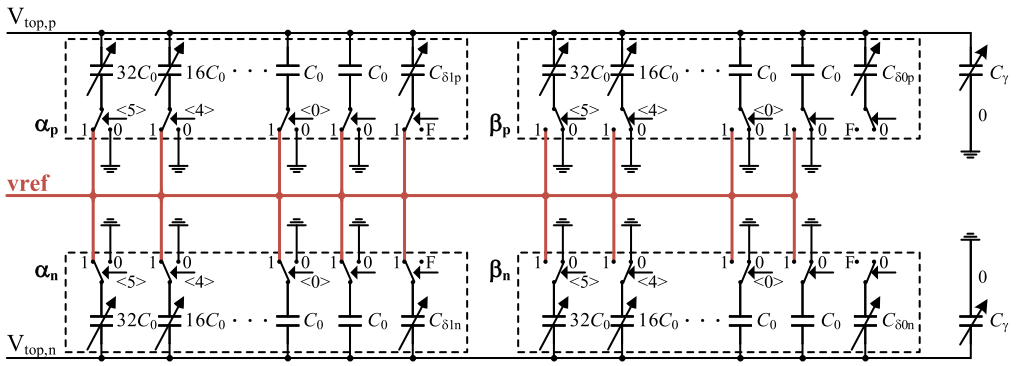

Fig. 2. Simplified schematic of the high-accuracy DAC. The bottom plate switches are set as during the sampling phase.

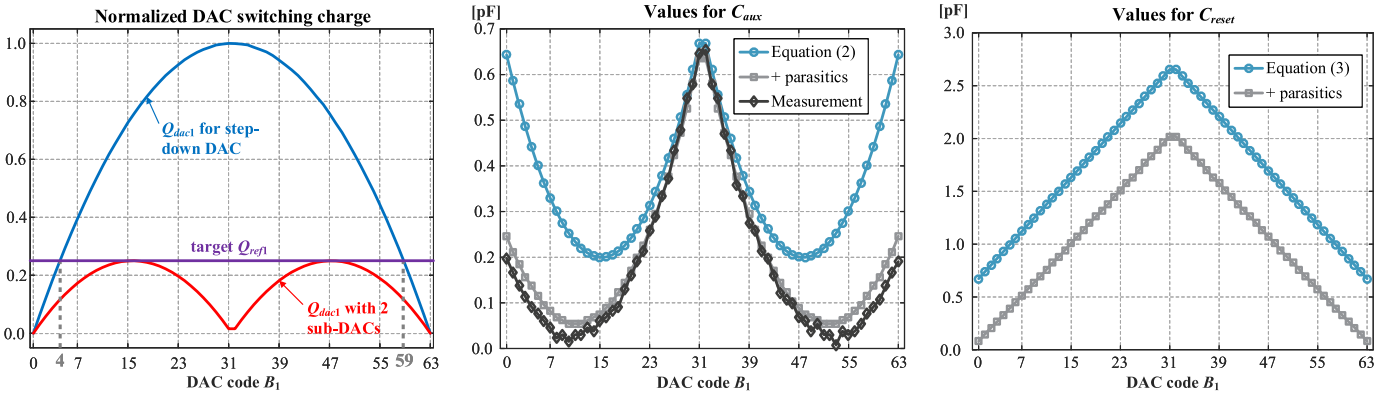

Fig. 3. Switching charge of the high-accuracy DAC (left) and the corresponding values for auxiliary capacitors C_{aux} (center) and C_{reset} (right).

The ideal value for C_{aux} can be derived by solving charge conservation equations. In the first order with parasitics neglected, it can be written as

$$C_{\text{aux}} = C_{\text{ref}}\frac{\Delta V_{\text{ref1}}}{V_{\text{ref1}}} - \frac{\alpha_1\alpha_0 + 2\alpha_0\beta_1 + \beta_1\beta_0}{N_{\text{dac}}}C_0 + \frac{\alpha_1\beta_0 - \alpha_0\beta_1}{N_{\text{dac}}}C_0\frac{\Delta V_{\text{ref1}}}{V_{\text{ref1}}} \quad (2)$$

with $N_{\text{dac}} = \alpha_1 + \alpha_0 + \beta_1 + \beta_0$ the relative total DAC size and $\Delta V_{\text{ref1}} = V_{\text{ref0}} - V_{\text{ref1}}$ the voltage drop on the reference node. The first term corresponds to the charge drawn from the charge reservoir from which the charge taken by the high-accuracy DAC is subtracted. The last term arises due to the voltage drop on the reference node. With a constant small value for ΔV_{ref1}, the second term dominates and it follows the shape of the switching charge of the high-accuracy DAC.

After processing the residue, the DAC needs to be reset to its initial state. The amount of charge required for this operation also depends on the code B_1 for which the residue has been generated. By connecting a second auxiliary capacitor C_{reset} to the reference node during reset, the charge Q_{ref2} taken from the charge reservoir becomes code-independent. Hence, during the sampling phase, a signal-independent and constant amount of charge $Q_{\text{ref1}} + Q_{\text{ref2}}$ should now be provided, which greatly simplifies the circuit providing the nominal reference.

The ideal value for C_{reset} can be written as follows:

$$C_{\text{reset}} = (C_{\text{ref}} + C_{\text{aux}})\frac{\Delta V_{\text{ref2}}}{V_{\text{ref2}}} - \frac{(\alpha_1 + \alpha_0)(\beta_1 + \beta_0)}{N_{\text{dac}}}C_0 + \frac{\alpha_1\beta_0 - \alpha_0\beta_1}{N_{\text{dac}}}C_0\frac{V_{\text{ref1}}}{V_{\text{ref2}}} \quad (3)$$

with $\Delta V_{\text{ref2}} = V_{\text{ref1}} - V_{\text{ref2}}$ the second drop of the reference voltage. Whereas the amount of units in $\alpha_1 C_0$ and $\alpha_0 C_0$ (or $\beta_1 C_0$ and $\beta_0 C_0$) is code-dependent, their *sum* is constant and determined by the sampling state. So, the second term in (3) is constant. Since C_{ref} is usually much larger than C_{aux}, the last term defines the profile of C_{reset}.

B. Implementation

Fig. 2 shows the schematic of the high-accuracy DAC for which the reference voltage is stabilized in this paper. By splitting it up in two sub-DACs α and β for the positive and negative parts of the input range, the switching energy is reduced compared with a DAC with a monotonic switching scheme [20], which is often used in a pipelined SAR ADC [5]. A comparison is shown in Fig. 3 (left). Since the sum of the charge drawn by the DAC and C_{aux} cannot be smaller than the largest value of Q_{dac1}, this implementation saves switching energy for the major part of the DAC codes B_1 (from 4 to 59, as shown in Fig. 3) compared with the step-down DAC. Furthermore, there is no big transition when the MSB toggles.

For this DAC, the coefficients used in previous analysis are as follows:

$$\alpha_1 = \{2B_1 + 1, 64\}, \quad \alpha_0 = \{65 - 2B_1, 0\},$$
$$\beta_1 = \{2B_1 - 63, 0\}, \quad \beta_0 = \{127 - 2B_1, 64\}.$$

The number of units in each sub-DAC scales linearly with the code B_1, and the two parts of each sub-DAC switch together to ensure the common mode stays around mid-supply.

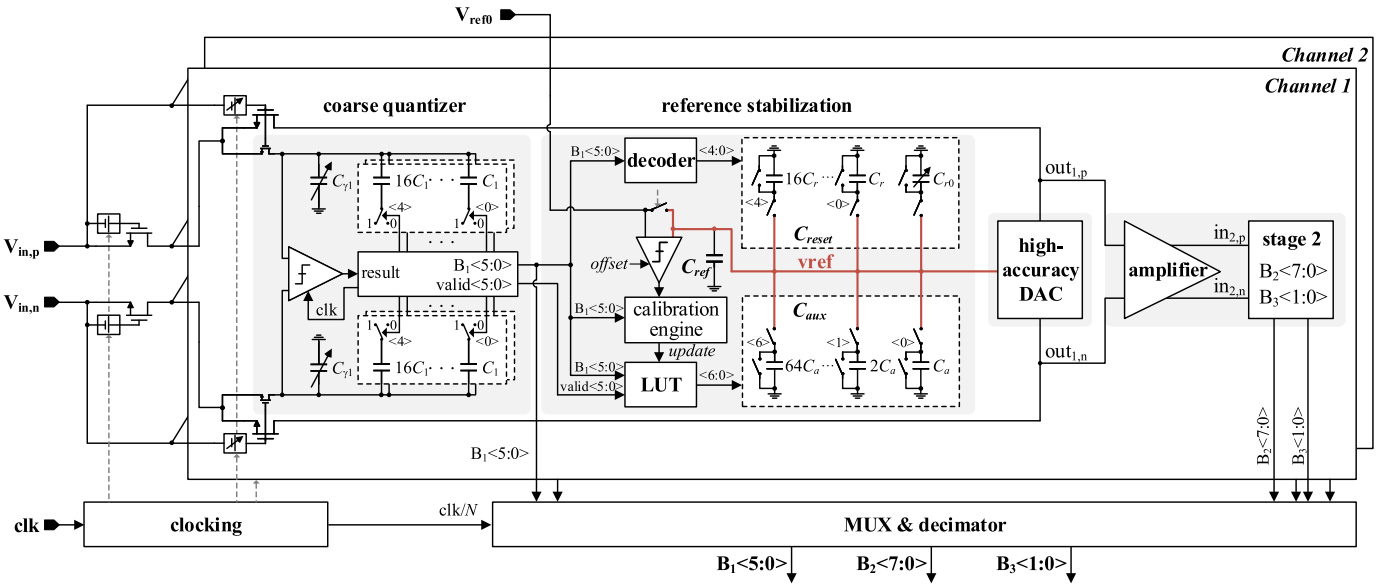

Fig. 4. Block diagram of the ADC. The technique of Fig. 1 is used in one high-accuracy DAC per channel using the full 6-bit code B_1 generated by the coarse quantizer to select the correct values for C_{aux} and C_{reset}.

This common-mode level is preferred for the dynamic residue amplifier with a complementary input pair, as discussed in Section IV-D.

With a DAC size of 4 pF (single-ended) and a charge reservoir of 50 pF, the values for C_{aux} and C_{reset} obtained using (2) and (3) are shown in Fig. 3. Also shown are the results when layout parasitics are considered, as well as the values obtained from background calibration in measurements as explained in Section V-C.

The values for C_{aux} follow a very nonlinear curve corresponding to the switching energy of the high-accuracy DAC. They are also very susceptible to parasitics, more specifically near the edges of the input range. To create this shape, C_{aux} is constructed as a 7-bit DAC with a unit size of 1/4th of C_0 with C_0 the unit size of the high-accuracy DAC. Behavioral simulations have shown that in the first order, the linearity scales linearly with the ratio of C_{ref} to the unit size of C_{aux}. With the chosen sizes of capacitances, this ratio is about 6500 which linearizes the DAC to better than 13-bit levels.

For C_{reset}, a piecewise linear curve is obtained. Parasitics mainly result in an offset of the curve, which only changes the absolute level V_{ref2} without making it signal-dependent. Hence, a fixed decoder can be used and no calibration is required for C_{reset}.

C. Decoupling Capacitance and Reference Buffers

In the proposed scheme, the signal-dependent ripple on the reference voltage is replaced by a signal-independent voltage drop. From (1), the ratio of $C_{\text{ref}}/C_{\text{dac}}$ determines the drop and there is a tradeoff between C_{ref} and the amount of signal attenuation. A *constant* drop of several LSBs can be tolerated, but the signal-dependent ripple should be kept within an LSB. Whereas a conventional decoupling capacitance should be large enough to fulfill the latter condition, our C_{ref} can be an order of magnitude smaller, since it only needs to limit the signal-independent voltage drop. For example, [5] uses 1 nF of decoupling capacitance, whereas this design uses two reference capacitors of 50 pF, which limit the voltage drop according to simulations within 1% or 8 mV.

Although reference buffers are not implemented in our design, we expect that the requirements are greatly relaxed by the presented technique. In a typical SAR, the reference voltage needs to be re-settled within the time allocated for each DAC settling step, which is often as short as possible by-design. Here, we use an architecture that only requires one reference compensation per conversion, and thus C_{ref} can be recharged during the ADC's much longer track time window. In our design, this is six to ten times larger, which reduces the bandwidth requirements of reference buffers. Furthermore, a much larger error on the settling to the nominal reference voltage can be tolerated. Indeed, the capacitive stabilization scheme always takes the same amount of charge from C_{ref}, so every error now becomes a signal-independent voltage drop of the reference voltage. These properties result in power savings in the reference buffers.

IV. ADC Design

A. Overview

An overview of the architecture of the two-time interleaved pipelined SAR ADC is shown in Fig. 4. A Nyquist-rate bootstrapped front-end sampler [21] minimizes the clock skew between the channels [22]. Each channel contains a first SAR stage, which resolves 6-bits B_1, a dynamic residue amplifier, and a second SAR stage, which first resolves 8-bits B_2 and then uses low-noise comparisons to generate two extra bits B_3. Considering the redundancy between the different phases, the total quantization level is 13.5 bit.

Due to the redundancy, only the last residue generated by the SAR algorithm in the first stage is critical for the overall ADC linearity. So, only this residue is generated

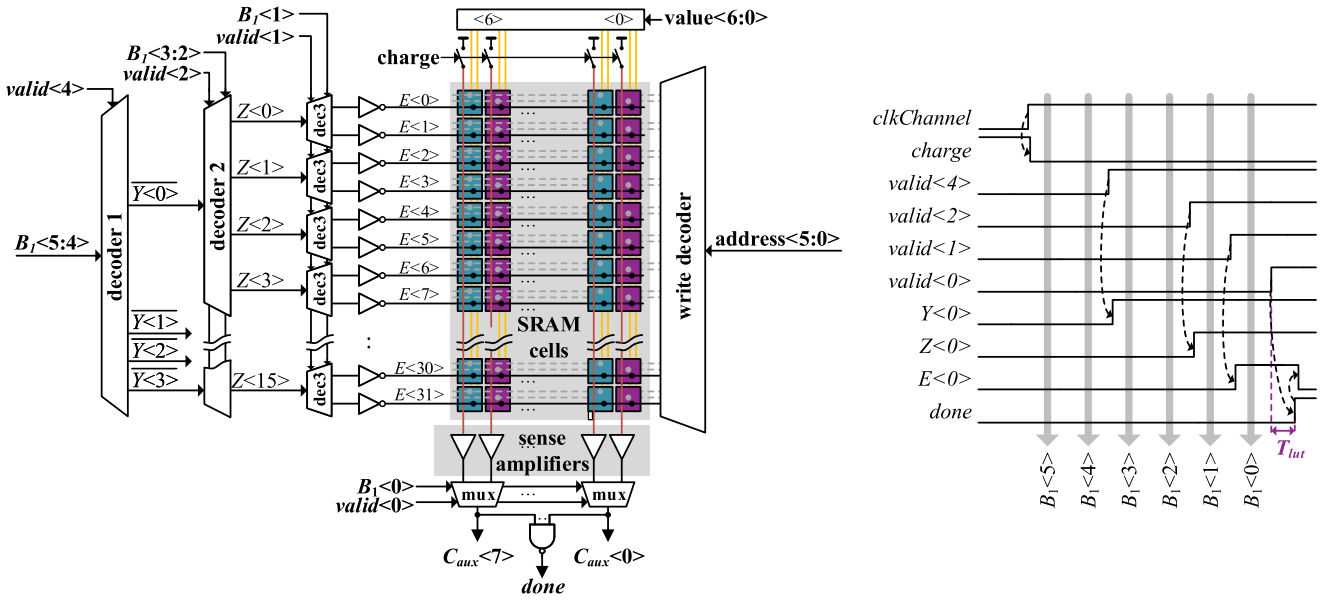

Fig. 5. Architecture and signal diagram of the LUT used to map code $B_1\langle 5{:}0\rangle$ generated by the coarse quantizer onto the 7-bit setting for C_{aux}.

with the high-accuracy DAC with stabilized reference and a fast coarse SAR quantizer is used to find the code B_1 to within 6-bit accuracy [23]. Each channel contains the reference stabilization circuitry shown in Fig. 4. The bottom plates in the coarse quantizer and second stage are just switched between ground and supply as in [24].

The ADC is driven by a clock up to 300 MS/s. Clocking circuitry generates two half-speed channel clocks with a nominal track time equal to 1/4th of the channel clock. For our test chip, the data bits are decimated and combined off-chip.

Sections IV-B–IV-D discuss the design details of the building blocks of the ADC.

B. Sampler and Coarse Quantizer

Parallel switches sample the signal onto the coarse and high-accuracy DACs. To minimize mismatches between the two samples, these switches use a common control signal and are scaled to match the input-path time constants of the coarse and high-accuracy paths to within 6-bit accuracy. They are bootstrapped with a programmable bootstrap voltage to calibrate bandwidth mismatches between the high-accuracy paths of the two channels [5]. The bootstrap circuits use the original input rather than the signal at the source of the sampling switch inside the channels to avoid charge injection from the front-end switch to the bootstrap capacitor. Dummy switches (not shown in Fig. 4) cancel coupling between channels during the SAR operation.

The coarse quantizer uses a DAC of 200 fF (single-ended) configured as a symmetrical split-capacitor DAC [25] resulting in a constant common mode. A single comparator implemented as in [26] is used within an asynchronous SAR loop [27]. From post-layout simulations, the conversion time is about 1.8 ns limited by transistor parasitics and interconnection parasitics due to non-optimized layout. This leaves about 3.2 ns for residue generation, amplification, and reset to achieve an overall clock speed of 300 MS/s.

C. Lookup Table

As stated in Section III-B, a lookup table (LUT) is used to map the B_1 code generated by the coarse quantizer onto a 7-bit word, which selects the right setting for the auxiliary DAC C_{aux}. To keep the access time of this LUT from becoming a speed bottleneck, a custom approach is adopted [28].

Since the SAR algorithm of the coarse quantizer determines the bits sequentially, the read operation from the LUT can be parallelized with the SAR quantizer as soon as the MSB bit is known. To this end, the coarse quantizer generates the signals $valid\langle 5{:}0\rangle$ to indicate the state of the SAR algorithm, as shown in Fig. 4. They are used to decode the address B_1 concurrently with the SAR operation as shown in Fig. 5.

The decoder operates in three levels. When the MSB and MSB-1 bits are valid, the first sub-decoder generates a signal Y that activates one out of four sub-decoders of the next level. Then, the same happens after the next two bits. When the LSB$+1$ bit is known, a read pulse E is generated on the correct word line to read out the memory cells. The 64 8T SRAM cells [29] are arranged in two columns depending on their LSB, as indicated in Fig. 5 by different colors. The bit lines are charged to V_{DD} when tracking the input signal, as shown in the signal diagram in Fig. 5. The read pulse E conditionally discharges the bit lines of all columns depending on the value stored in the memory cells. After amplification, two values are now fetched from the memory and the LSB bit selects via a multiplexer the correct one.

The sub-decoders are built using dynamic logic [30] with the *valid* signals acting as the clock signals. The sense amplifier is shown in Fig. 6. It is basically an inverter with increased threshold level followed by a latch with improved toggling speed in one direction when the voltage of the bitline has dropped by about 150 mV as tradeoff between speed and sensitivity.

For asynchronous operation, a *done* signal is generated by a simple NAND gate. This rules out a setting of all ones which

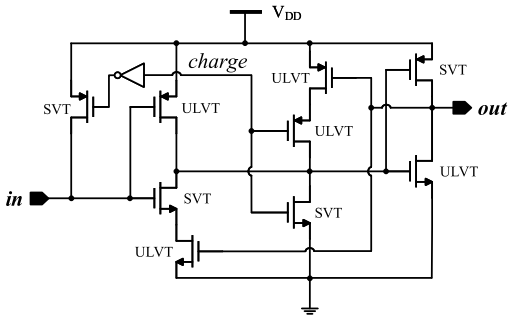

Fig. 6. Sense amplifier used in the LUT of Fig. 5.

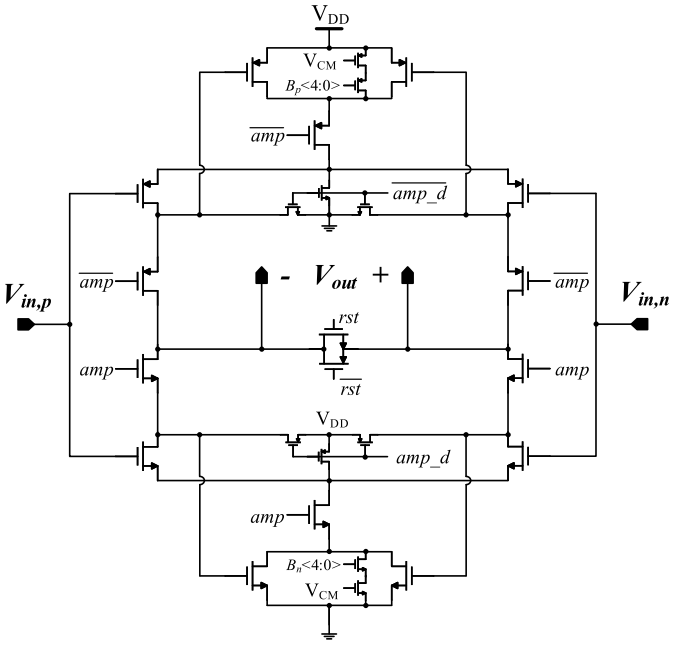

Fig. 7. Schematic of a dynamic residue amplifier.

only slightly decreases the range of C_{aux}. The delay in the logic is sufficient to deal with skew between the different bit lines. Post-layout simulations show an average read delay T_{lut} of 250 ps limited by the interconnection parasitics.

D. Dynamic Amplifier and Second Stage

The dynamic amplifier (DA) of Fig. 7 amplifies the residue of stage 1 and passes it on to stage 2. The input is connected to the top plates of the stage 1 high accuracy DAC, and the output is connected to the inputs of stage 2 (in_p and in_n of Fig. 9). The timing of the residue transfer is shown in Fig. 8. Initially, during stage 1's SAR conversion, the DA is held in a state where both the source and drain nodes of the complementary input pair transistors are shorted to V_{DD} or ground. This ensures that kickback from stage 2's operation will not influence stage 1.

After the stage 1 conversion is finished and a residue is available on stage 1's high accuracy DAC, the DA begins amplification by integrating a current proportional to the residue onto the load presented by stage 2. The gain of the DA is determined by the open-loop integration time, which is controlled with a 13-bit digitally controlled delay line.

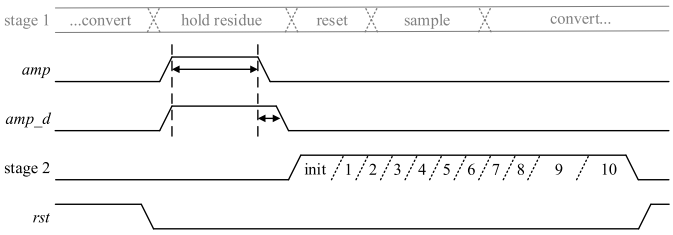

Fig. 8. Timing diagram of the amplifier and second stage.

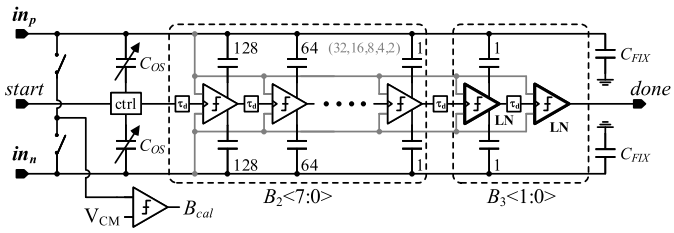

Fig. 9. Simplified schematic of the second stage.

Its nominal gain value is 8, which requires 900 ps in simulation.

At the end of the amplification period, the switches connecting the DA to stage 2 open first (amp in Figs. 7 and 8). Immediately after these switches are opened, the internal nodes are reset back to V_{DD} and ground (amp_d). Simulations indicate that THD is improved by more than 5 dB when disconnecting with these two sequential steps versus in a single step, since any potential overlap is avoided. The dc common-mode output voltage of the DA can be adjusted using the complementary 5-bit tuning DACs shown in parallel with the main CMFB current source transistors in Fig. 7. Despite the limited voltage headroom of this 16-nm technology, it is possible to bias the CMFB transistors in saturation and obtain 18-dB CMRR (simulation). By contrast, the CMFB transistors in [5] were biased in triode and achieved only 1-dB CMRR as a result (from simulation).

Fig. 9 shows a simplified schematic of the second stage. The SAR ADC is similar to that of [24] with bottom plates switching between ground and supply. It consists of a chain of ten asynchronously clocked comparators, with each comparator driving one unit of a capacitive step-down DAC. The first eight comparators determine $B_2\langle 7{:}0\rangle$. The last two comparators are specially designed for low noise and find the code $B_3\langle 1{:}0\rangle$. There is 1-bit redundancy between B_2 and B_3, thereby relaxing the comparator noise and DAC settling requirements of the earlier comparisons.

V. Calibration Techniques

To enhance performance, the ADC uses both redundancy and calibration techniques [31]. The offsets of each comparator are removed through calibration using a foreground calibration [24] for our test chip, but background calibration, as in [32], is also possible. Inter-channel offset is digitally corrected like in [24] while time constant mismatch in the sampling network is tuned via programmable bootstrap voltages [5]. Other calibration techniques are summarized in the following sections.

A. Calibration of High-Accuracy DACs

The high-accuracy DAC of Fig. 2 (4 pF) is sized according to noise requirements, not linearity. Thus, to ensure sufficient linearity, the 3 MSB capacitor units of each sub-DAC are calibrated in an off-line procedure like in [5]. This suppresses odd-order distortion.

Gain mismatch between the two sub-DACs of Fig. 2 results in even-order distortion. To correct this error, four 7-bit tunable capacitors C_δ with unit size 200 aF are added. During sampling, their bottom plates are connected to the reference or ground. When generating the residue, one pair stays connected while the bottom plates of the other ones are left floating. This configuration prevents the voltages on the floating nodes from going above supply or below ground during conversion.

Calibration of the sub-DAC gain happens off-line by first sampling the common-mode voltage $V_{\rm cm}$, then switching all DAC units to ground, and finally switching the α sub-DAC back with the appropriate tunable capacitors left floating. The top plates then carry a voltage near $V_{\rm cm}$ and the difference is detected via the amplifier and the second stage. Repeating the procedure but switching the β sub-DAC back results in a second digitized voltage, and the difference between the two results is used to tune C_δ.

Finally, the top plate parasitics are tuned via C_γ to compensate inter-channel gain mismatches like in [24].

B. Calibration of Coarse Quantizer

Besides comparator offset, the gain mismatch between the coarse and high-accuracy DACs is tuned via the top plate parasitic of the coarse quantizer ($C_{\gamma 1}$ in Fig. 4). This happens by monitoring the average result of the second stage for the positive and negative sides of the input range and adjusting $C_{\gamma 1}$ when the difference is too large.

Due to higher than expected layout parasitics in the coarse quantizer, the reference voltage $V_{\rm ref0}$ has been lowered to 610 from 800 mV to match the input ranges of the two DACs within the calibration range.

C. Filling the Lookup Table

As shown in Fig. 3 (center), the exact setting for $C_{\rm aux}$ is susceptible to layout parasitics and DAC mismatches, including mismatch of $C_{\rm aux}$ itself. A background calibration procedure is used to update the values of the LUT. From (2), the values are mainly determined by capacitor ratios, which are not expected to vary a lot with PVT, so the coefficients can be frozen after settling to their final values.

The voltage $V_{\rm ref1}$ on the reference node *vref* is monitored, as shown in Fig. 4. After amplifying the residue to the second stage, a comparator is activated that compares $V_{\rm ref1}$ with the nominal reference voltage $V_{\rm ref0}$. The comparator has a tunable offset to compensate for the voltage drop $\Delta V_{\rm ref1}$. The result of the comparator increases or decreases a counter per code B_1. When it achieves its maximum or minimum value, the counter is reset to its center value and the value in the LUT for that B_1 is updated by increasing or decreasing it with one via the write decoder of Fig. 5 when the LUT is not active at the beginning of the track time.

The offset of the comparator is first set in a foreground calibration step by switching the high-accuracy DAC using the code B_1 where a minimum is expected and a fixed low setting for $C_{\rm aux}$. It is updated online when any of the $C_{\rm aux}$ settings become too low.

D. Calibration of Residue Amplifier

The offset of the residue amplifier is compensated by switching $C_{\rm OS}$ in Fig. 9 differentially. This adjustment is done during the init phase of the stage 2 operation (see Fig. 8). Any remaining differential offset present after this coarse cancellation is removed by the comparators themselves during their own offset cancellation procedure. Also, the common mode can be adjusted during this time to optimize the speed of the comparators.

A special comparator circuit is added in Fig. 9 for the purpose of sensing the DA's common-mode output level, and then using this information $B_{\rm cal}$ to tune the programmable common-mode adjustment circuits in Fig. 7 during foreground calibration with shorted DA outputs. The target common-mode level $V_{\rm cm}$ is locally generated.

The gain of the residue amplifier is set like in [24] by using the high-accuracy DAC to apply a ± 0.5 LSB at the input of of the amplifier during foreground calibration.

E. Calibration Time and Hardware

All foreground calibration routines adopt a binary search algorithm requiring maximum $N + 3$ steps (to allow a non-binary radix) to determine N-bit calibration words. With 2k clock cycles per step used for averaging, it requires about 350k clock cycles in total. Note that all the comparators in the second stage are calibrated simultaneously to reduce the required calibration time with a factor 2. Since all calibration routines are similar, hardware optimization by reusing dedicated hardware for the different routines should be possible.

Simulations show settling of all coefficients in the LUT after 250k clock cycles with a full-scale sine wave input signal starting from zero for all codes, and using 4-bit counters per code B_1. Due to the histogram of a sine wave and the shape of the calibration curve shown in the center of Fig. 3, the mid-range codes take the most cycles. The hardware required for this calibration corresponds to an extra comparator, and a counter per DAC code. Note that it is also possible to use a single counter and calibrate the DAC codes in series, which would then require about 9M cycles.

VI. Measurement Results

The ADC prototype has been fabricated in a 1P11M 16-nm digital CMOS FinFET process and has a core area of $350\times325\ \mu{\rm m}^2$, as shown in Fig. 10. The complete reference stabilization block of Fig. 4, including the charge reservoir $C_{\rm ref}$ of 50 pF, occupies about 16% of the core area. The total area is limited by the pad ring, and filled with mainly decoupling for the output buffers and the single supply voltage of 800 mV used for the ADC.

For the reference voltage, there is only a low ohmic connection without extra decoupling capacitance. The resistance

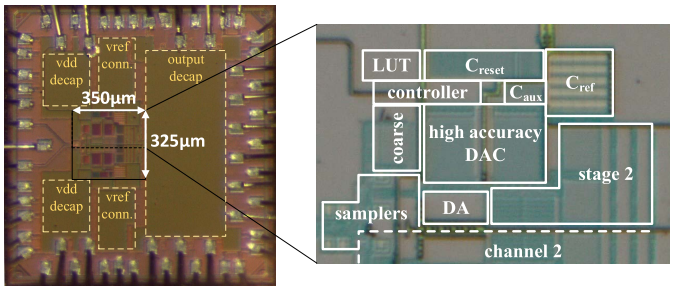

Fig. 10. Chip micrograph with details of the layout of a channel.

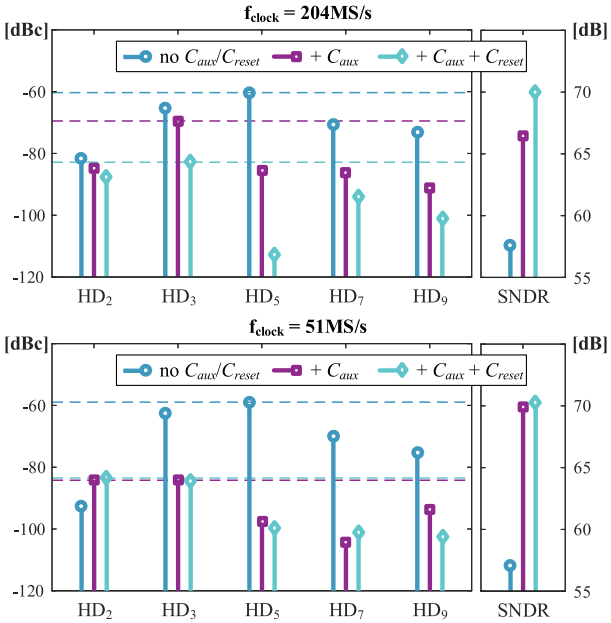

Fig. 11. Effect of C_{aux} and C_{reset} on harmonic spurs and SNDR for f_{in} = 30 MHz (decimated by 6 to isolate one channel) and two different clock speeds.

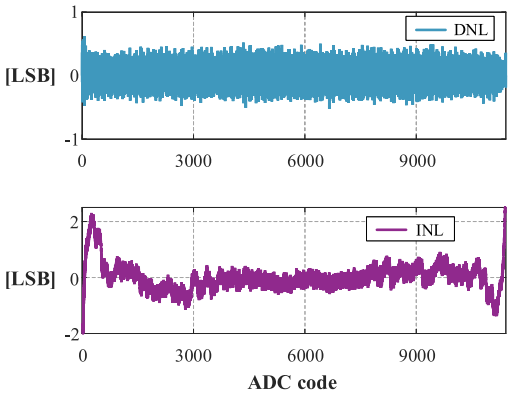

Fig. 12. DNL and INL of ADC measured with f_{clock} = 50 MS/s.

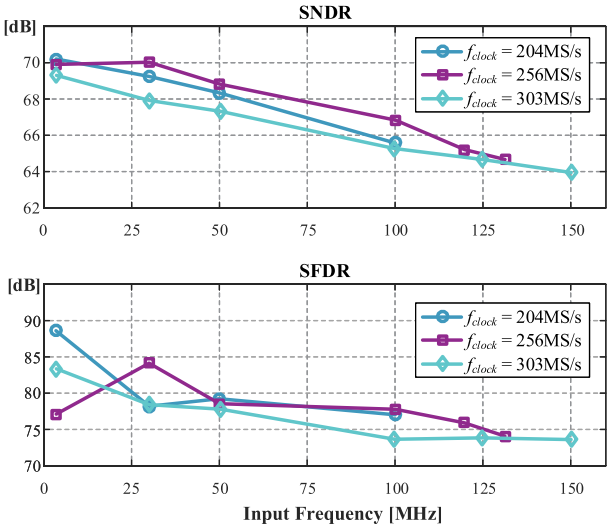

Fig. 13. Measured SNDR and SFDR for different input and clock frequencies.

of this connection adds to the resistance of the switch used to recharge the charge reservoir C_{ref} and might result in incomplete settling. However, since the ADC always takes the same amount of charge from C_{ref}, any incomplete settling is signal-independent and does not degrade the ADC performance as discussed in Section III-C.

The test setup is similar to [5] with the reference voltage V_{ref0} itself generated by an external dc source (Keithley 2400 SourceMeter). It is brought on-chip via a bondwire resulting in an equivalent circuit as in [13].

After running the calibration routines described in Section V, the settings for C_{aux} shown in Fig. 3 are obtained and frozen. The effect of the auxiliary DACs on the harmonic spurs and corresponding SNDR is shown in Fig. 11 with one channel isolated. For a high clock speed, the use of C_{reset} suppresses the spurs below −80 dBc as indicated by the dashed lines in Fig. 11. At 51 MS/s, the reset time is long enough for complete settling of the voltage of the charge reservoir C_{ref} to V_{ref0}.

The linearity measured as DNL and INL of the ADC is shown in Fig. 12. DNL is within −0.52/+0.62 LSB and minimum and maximum INL is −1.38/+2.31 LSB near the edges of the valid code range corresponding to signals within the input range of the ADC, and −1.98/+2.31 LSB when including also invalid codes.

The maximum clock speed where the ADC is still functional is 311 MS/s after which the second stage becomes too slow. With a low input frequency of 3.6 MHz, the SNDR is 70.2, 69.9, and 69.3 dB with a sampling speed of 204, 256, and 303 MS/s, respectively. As reported in Fig. 13, this reduces to 65.6, 64.7, and 63.9 dB with Nyquist inputs. Fig. 14 shows the output spectrum measured with the low and a high input frequency while sampling at 303 MS/s. Whereas the SFDR in the first case is more than 83 dB, it is limited by non-harmonic spurs around the input signal to 73.6 dB. The ENOB is also degraded due to jitter.

The conversion energy of the ADC is 12 pJ and without clock signal, it has 200-μW dc power due to leakage and V_{cm} generation. At 303 MS/s, the power consumption is then 3.6 mW. Fig. 15 shows the power breakdown of the ADC as obtained from simulations. The second-stage comparators, switching energy of the high-accuracy DAC in the first stage, and the residue amplifier are the dominant sources. The reference stabilization scheme requires less than 5% of the total power budget. Input or reference buffers are not included in this prototype.

A summary of the performance of the ADC and a comparison with pipelined SAR ADCs with comparable

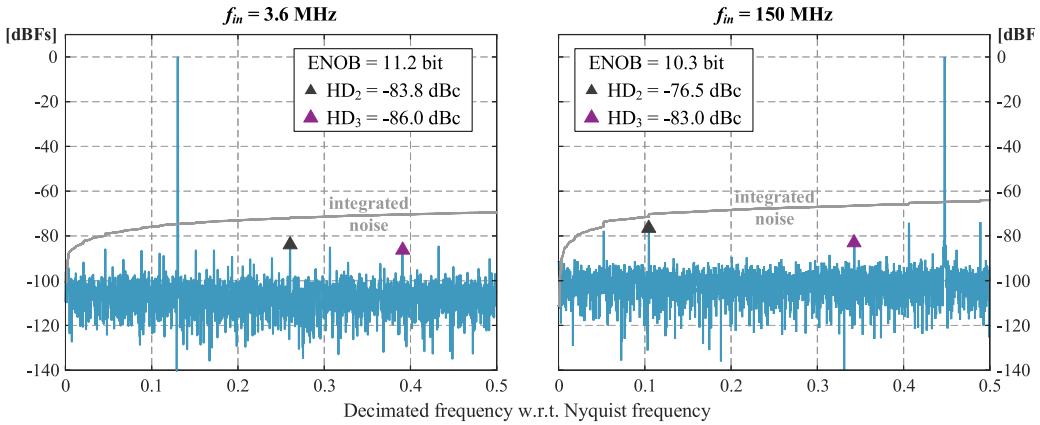

Fig. 14. Measured PSD with a low (left) and high (right) input frequency with $f_{\text{clock}} = 303$ MS/s. Output is decimated with factor 11.

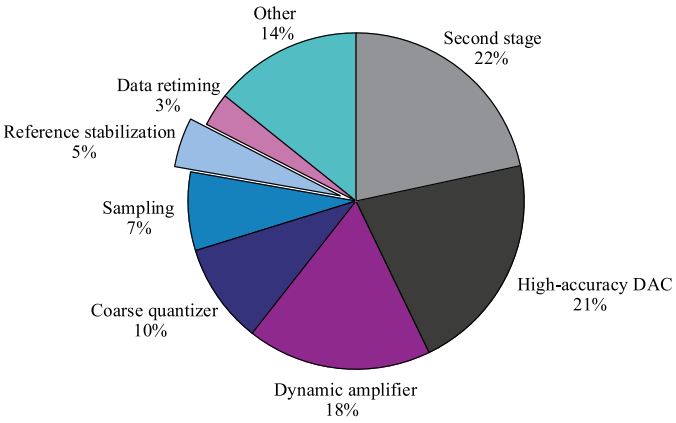

Fig. 15. Simulated power breakdown of the ADC at 303 MS/s.

TABLE I
COMPARISON OF THE STATE-OF-THE-ART PIPELINED SAR ADCS

	[5]	[33]	[34]	[8]	[35]	[36]	This work	*unit*
Technology	28	65	65	28	65	28	**16**	nm
$\mathbf{f_{sample}}$	200	210	450	800	330	160	**303**	MS/s
$\mathbf{ENOB_{lf}}$	11.33	10.25	9.81	10.04	10.95	9.96	**11.22**	bit
$\mathbf{ENOB_{hf}}$	10.50	9.69	9.04	9.81	10.26	9.86	**10.33**	bit
$\mathbf{SFDR_{hf}}$	73	75	70	76	76	73	**74**	dB
$\mathbf{Area_{core}}$	0.10	0.48	0.07	0.093	0.08	—	**0.11**	mm^2
$\mathbf{Area_{total}}$	0.35	—	0.10	—	—	0.10	**0.27**	mm^2
Power	2.3	5.3	7.4	14.6	6.23	1.9	**3.6**	mW
$\mathbf{FoM_{W,lf}}$	4.5	20.7	18.4	17.3	9.5	11.9	**5.1**	fJ/c.s.
$\mathbf{FoM_{W,hf}}$	7.9	30.5	31.2	20.3	15.4	12.8	**9.2**	fJ/c.s.
$\mathbf{FoM_{S,lf}}$	176.4	166.4	165.6	166.6	171.9	167.9	**175.5**	dB
$\mathbf{FoM_{S,hf}}$	171.4	163.1	161.0	165.2	167.7	167.3	**170.2**	dB

speed/accuracy specs is shown in Table I. With a Nyquist Schreier FoM of 170.2 dB, this paper achieves excellent performance. Compared with [5], a similar accuracy with 50% higher speed has been realized. The core area is also comparable, but it contains a complete reference stabilization scheme, whereas [5] needs 1-nF on-chip decoupling capacitance.

VII. CONCLUSION

Whereas capacitive SAR architectures in combination with pipelining and interleaving are an attractive solution for realizing power-efficient ADCs with medium to high accuracies and speeds, they are vulnerable to ripple on the reference voltage. Traditional solutions, like on-chip decoupling capacitance or reference buffers, are area- or power-hungry solutions. This paper shows that the reference voltage can be stabilized by using auxiliary DACs which remove the signal-dependent drop of the reference voltage due to DAC switching. Furthermore, by using the same technique when resetting the DAC, the load on the reference node is also made signal-independent.

The technique has been implemented in an interleaved pipelined SAR in 16-nm FinFET technology. Measurement results demonstrate the efficiency of the capacitive stabilization technique for reducing distortion with only a small area and power penalty making it an attractive solution for high-performance SAR-based ADCs.

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REFERENCES

[1] B. Murmann. (2017). *ADC Performance Surveu 1997–2017*. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

[2] J. Zhong, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "Thermal and reference noise analysis of time-interleaving SAR and partial-interleaving pipelined-SAR ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2196–2206, Sep. 2015.

[3] F. van der Goes *et al.*, "A 1.5 mW 68 dB SNDR 80 MS/s 2× interleaved pipelined SAR ADC in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2835–2845, Dec. 2014.

[4] E. Martens, B. Hershberg, and J. Craninckx, "A 16 nm 69 dB SNDR 300 MSps ADC with capacitive reference stabilization," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2017, pp. 92–93.

[5] B. Verbruggen, K. Deguchi, B. Malki, and J. Craninckx, "A 70 dB SNDR 200 MS/s 2.3 mW dynamic pipelined SAR ADC in 28 nm digital CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 242–243.

[6] J. Kuppambatti and P. R. Kinget, "Current reference pre-charging techniques for low-power zero-crossing pipeline-SAR ADCs," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 683–694, Mar. 2014.

[7] C.-H. Chan *et al.*, "60-dB SNDR 100-MS/s SAR ADCs with threshold reconfigurable reference error calibration," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2576–2588, Oct. 2017.

[8] Y.-C. Lien, "A 14.6 mW 12b 800 MS/s 4x time-interleaved pipelined SAR ADC achieving 60.8 dB SNDR with Nyquist input and sampling timing skew of 60 fs_{rms} without calibration," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 156–157.

[9] A. Kumar *et al.*, "A 0.065 mm^2 19.8 mW single channel calibration-free 12b 600 MS/s ADC in 28 nm UTBB FDSOI using FBB," in *IEEE Eur. Solid-State Circuits Conf. (ESSCIRC) Dig. Tech. Papers*, Sep. 2016, pp. 165–168.

[10] H. Xu *et al.*, "A 78.5 dB-SNDR radiation- and metastability-tolerant two-step split SAR ADC operating up to 75 MS/s with 24.9 mW power consumption in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 476–477.

[11] S.-H. Wan *et al.*, "A 10-bit 50-MS/s SAR ADC with techniques for relaxing the requirement on driving capability of reference voltage buffers," in *IEEE Asian Solid-State Circuits Conf. (A-SSCC) Dig. Tech. Papers*, Nov. 2013, pp. 293–296.

[12] J. Zhong, Y. Zhu, C.-H. Chan, S.-W. Sin, S.-P. U, and R. P. Martins, "A 12 b 180 MS/s 0.068 mm^2 pipelined-SAR ADC with merged-residue DAC for noise reduction," in *IEEE Eur. Solid-State Circuits Conf. (ESSCIRC) Dig. Tech. Papers*, Sep. 2016, pp. 169–172.

[13] R. Kapusta, J. Shen, S. Decker, H. Li, E. Ibaragi, and H. Zhu, "A 14b 80 MS/s SAR ADC With 73.6 dB SNDR in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3059–3066, Dec. 2013.

[14] J. Craninckx and G. van der Plas, "A 65 fJ/conversion-step 0-to-50 MS/s 0-to-0.7 mW 9b charge-sharing SAR ADC in 90 nm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 246–247.

[15] A. Venca, N. Ghittori, A. Bosi, and C. Nani, "A 0.076 mm^2 12 b 26.5 mW 600 MS/s 4-way interleaved subranging SAR-$\Delta\Sigma$ ADC with on-chip buffer in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2951–2962, Dec. 2016.

[16] M. Maddox, B. Chen, M. Coln, R. Kapusta, J. Shen, and L. Fernando, "A 16 bit linear passive-charge-sharing SAR ADC in 55 nm CMOS," in *IEEE Asian Solid-State Circuits Conf. (A-SSCC) Dig. Tech. Papers*, Nov. 2016, pp. 153–156.

[17] W.-H. Tseng, W.-L. Lee, C.-Y. Huang, and P.-C. Chiu, "A 12-bit 104-MS/s SAR ADC in 28 nm CMOS for digitally-assisted wireless transmitters," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2222–2231, Oct. 2016.

[18] C.-H. Chan *et al.*, "A 0.011 mm^2 60 dB SNDR 100 MS/s reference error calibrated SAR ADC with 3 pF decoupling capacitance for reference voltages," in *IEEE Asian Solid-State Circuits Conf. (A-SSCC) Dig. Tech. Papers*, Nov. 2016, pp. 145–148.

[19] Y.-Z. Lin, C.-H. Tsai, S.-C. Tsou, and C.-H. Lu, "A 8.2-mW 10-b 1.6-GS/s 4× TI SAR ADC with fast reference charge neutralization and background timing-skew calibration in 16-nm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 204–205.

[20] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[21] A. M. Abo and P. R. Gary, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[22] S. K. Gupta, M. A. Inerfield, and J. Wang, "A 1-GS/s 11-bit ADC with 55-dB SNDR, 250-mW power realized by a high bandwidth scalable time-interleaved architecture," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2650–2657, Dec. 2006.

[23] V. Tripathi and B. Murmann, "A 160 MS/s, 11.1 mW, single-channel pipelined SAR ADC with 68.3 dB SNDR," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2014, pp. 1–4.

[24] B. Verbruggen, M. Iriguchi, and J. Craninckx, "A 1.7 mW 11b 250 MS/s 2-times interleaved fully dynamic pipelined SAR ADC in 40 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2880–2887, Dec. 2012.

[25] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 739–747, Apr. 2007.

[26] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE ASSCC*, Nov. 2008, pp. 269–272.

[27] S.-W. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 12, no. 12, pp. 2669–2680, Dec. 2006.

[28] B. Hershberg, S. Weaver, S. Takeuchi, K. Hamashita, and U.-K. Moon, "Binary access memory: An optimized lookup table for successive approximation applications," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, May 2011, pp. 1620–1623.

[29] L. Chang *et al.*, "Stable SRAM cell design for the 32 nm node and beyond," in *IEEE Symp. VLSI Technol., Dig. Tech. Papers*, Jun. 2005, pp. 128–129.

[30] R. H. Krambeck, C. M. Lee, and H. F. S. Law, "High-speed compact circuits with CMOS," *IEEE J. Solid-State Circuits*, vol. SSC-17, no. 3, pp. 614–619, Jun. 1982.

[31] B. Murmann, "Digitally assisted data converter design," in *Proc. ESSCIRC*, Sep. 2013, pp. 24–31.

[32] B. Verbruggen *et al.*, "A 2.1 mW 11b 410 MS/s dynamic pipelined SAR ADC with background calibration in 28 nm digital CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2013, pp. 268–269.

[33] C.-Y. Lin and T.-C. Lee, "A 12-bit 210-MS/s 5.3-mW pipelined-SAR ADC with a passive residue transfer technique," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 244–245.

[34] Y. Zhu, C.-H. Chan, S.-P. U, and R. P. Martins, "An 11 b 450 MS/s three-way time-interleaved subranging pipelined-SAR ADC in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1223–1234, May 2016.

[35] H. Huang, S. Sarkar, B. Elies, and Y. Chiu, "4 A 12b 330 MS/s pipelined-SAR ADC with PVT-stabilized dynamic amplifier achieving <1dB SNDR variation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 472–473.

[36] K. Yoshioka *et al.*, "A 0.7V 12b 160 MS/s 12.8 fJ/conv-step pipelined-SAR ADC in 28 nm CMOS with digital amplifier technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 478–479.

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