A 1-GS/s, 12-b, Single-Channel Pipelined ADC With Dead-Zone-Degenerated Ring Amplifiers

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***Abstract*— Ring amplification has recently been shown capable of simultaneously achieving high linearity and high bandwidth (BW) in low-voltage, deep nanoscale CMOS processes, while retaining good power efficiency. In these processes, the low but very flat open-loop (OL) gain versus output voltage characteristic of the ring amplifier can be exploited, together with its high BW, to overcome the low intrinsic gain limitations that otherwise mandate the use of power-consuming analog circuits and complex digital calibration. Within this context, this paper introduces the techniques of dead-zone degeneration (DZD) and second-stage bias enhancement to further extend the linearity and speed limits of the ring amplifier, respectively. These techniques are applied to a 12-b, 1-GS/s, single-channel pipelined ADC implemented in a 28-nm planar CMOS process, which achieves 56.6-dB SNDR and 73.1-dB SFDR while consuming 24.8 mW from a single 0.9-V supply, resulting in Schreier and Walden figure-of-merit (FoM) values of 159.6 dB and 45 fJ/conv.-step, respectively.**

***Index Terms*— Bias enhancement, gain boosting, pipelined ADC, ring amplifier, ringamp, single-channel.**

I. Introduction

IN THE context of high-linearity and high-bandwidth ADCs, the use of pipelining is a popular choice, as it allows information to be broken down into smaller increments that can be processed faster, at the cost of added latency. However, the residue amplification step required by this technique often imposes a limit on the power efficiency that can be achieved, as tough speed and linearity specifications usually necessitate power-hungry amplifiers [1]–[7]. At the upper boundary of high-speed designs, it becomes even more difficult to satisfy both BW and biasing headroom constraints, and to deal with this the residue amplifiers are often placed on a dedicated high-voltage supply, drastically reducing efficiency [3]–[5]. Moreover, when the required speed exceeds what is achievable with a single channel, time interleaving must be used, which comes at the expense of calibration complexity and its associated power efficiency penalty [1], [3], [4], [7]–[12]. A review of the state of the art reveals that most high-linearity and high-BW converters[1] reported to date rely on pipelining and time interleaving, and only a few single-channel implementations reach this performance region [13]. Moreover, approaching the upper boundary of speed, the power efficiency of these single-channel ADCs tends to be heavily penalized. Thus, the maximization of *per-channel* speed and linearity, along with the minimization of power consumption, is of paramount importance for the implementation of power-efficient, high-performance ADCs that can meet the demanding specifications of next-generation communication applications [14], [15].

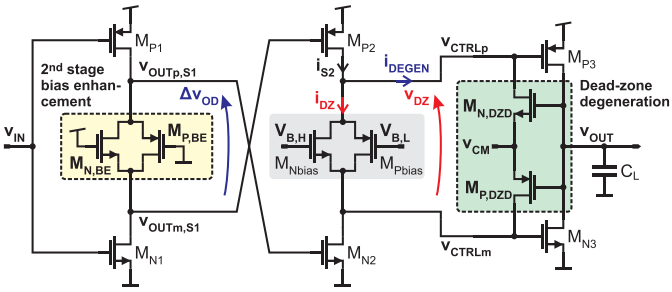

Fig. 1. Proposed enhanced-linearity-and-BW ringamp featuring DZD and second-stage bias enhancement.

Ring amplification [16] has been recently introduced as a solution for implementing high-efficiency scalable amplifiers in switched-capacitor circuits, with early embodiments focusing on high-linearity and low-to-medium speed implementations [17]–[20]. More recently, in [21] and [22] it was shown that ring amplification combined with first-order gain calibration can provide a power-effective solution for achieving high-speed and linearity in nanoscale CMOS by exploiting the flatness properties of the ringamp open-loop (OL) gain, even when intrinsic device gain is severely limited. In this paper we extend this concept further by introducing a new ring amplifier with increased linearity and speed, shown in Fig. 1, based on the techniques of *DZD* and *second-stage bias enhancement* [23]. Using these techniques, the implemented ADC achieves the highest speed reported to date for ringamp-based converters, and the best power efficiency among single-channel ADCs with greater than 9 ENOB and higher than 800 MS/s.

This paper is organized as follows. Section II reviews the operation and properties of the baseline ringamp which this

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[1] In the remainder of this paper, we denote as high-linearity, high-BW converters those achieving ≥ 400 MS/s and ≥ 9 ENOB with a Nyquist input.

work builds upon. Section III discusses the new ringamp proposed in this paper and the techniques it leverages for enhancing linearity and speed, demonstrating their effects and process, supply voltage, and temperature (PVT) sensitivity through circuit simulation. Section IV describes the implementation of these ideas in a prototype pipelined ADC, and the measurement results obtained are reported in Section V. Finally, Section VI concludes this paper.

II. Baseline Ringamp Operation

Fig. 2(a) shows the core schematic and main parameters of the ringamp introduced in [22]. As this structure constitutes the baseline architecture from which the ringamp introduced in this paper builds upon, its most relevant properties are reviewed in this section, along with useful definitions that will aid the discussion in Section III.

Briefly summarized, the ringamp in Fig. 2(a) is a three-stage inverter-based amplifier which uses an *anti-parallel CMOS (AP-CMOS) arrangement* [22] in the second stage for inducing the so-called dead-zone (DZ) voltage to under-drive the output devices and thus achieve stabilization when working in feedback. The DZ voltage $V_{\rm DZ}$, defined as the voltage difference between the output stage control nodes $v_{{\rm CTRL}p}$ and $v_{{\rm CTRL}m}$, plays a major role in defining the static and dynamic properties of the ringamp [22].

A. Static Properties

Since the second stage of the baseline ringamp is a single-input, multiple-output system, the overall ringamp OL gain is better expressed in terms of the first-stage gain, A_{S1}, and the gain of the second and third stages combined, $A_{S2,S3}$:

$$A_{\rm OL} \triangleq A_{S1,S2,S3} \triangleq A_{S1}A_{S2,S3} \tag{1}$$

where

$$A_{S1} = \left(g_{m1}^{P} + g_{m1}^{N}\right)\left(r_{o1}^{P} || r_{o1}^{N}\right) \tag{2}$$

and it can be shown that

$$A_{S2,S3} = \frac{\left(g_{m2}^{P} + g_{m2}^{N}\right)\left(g_{m3}^{P'} + g_{m3}^{N'}\right) + g_{m3}^{P} g_{m2}^{P} \frac{r_o^B}{r_{o2}^N} + g_{m3}^{N} g_{m2}^{N} \frac{r_o^B}{r_{o2}^P}}{\frac{r_{o2}^{P'} + r_o^B + r_{o2}^{P'}}{r_{o2}^P \cdot r_{o2}^N \cdot r_{o3}}} \tag{3}$$

where the following definitions hold ($i = \{1, 2, 3\}$, $j = \{\rm P, N\}$):

$$\begin{aligned} g_{mi}^{j}, r_{oi}^{j} &= \text{transconductance and output resistance of } M_{ji} \\ g_{m}^{Bj}, r_{o}^{Bj} &= \text{transconductance and output resistance of } M_{j,\rm bias} \\ r_o^B &\triangleq r_o^{\rm BP} || r_o^{\rm BN}, \quad r_{o3} \triangleq r_{o3}^{P} || r_{o3}^{N} \\ r_{o2}^{P'} &\triangleq r_{o2}^{P}\left(g_m^{\rm BP} r_o^B + 1\right), \quad r_{o2}^{N'} \triangleq r_{o2}^{N}\left(g_m^{\rm BN} r_o^B + 1\right) \\ g_{m3}^{P'} &\triangleq g_{m3}^{P}\left(g_m^{\rm BN} r_o^B + 1\right), \quad g_{m3}^{N'} \triangleq g_{m3}^{N}\left(g_m^{\rm BP} r_o^B + 1\right). \end{aligned}$$

Likewise, the composite partial gains $A_{S1,S2}^{P}$ and $A_{S1,S2}^{N}$ of the first and second stages can be expressed as

$$\begin{aligned} A_{S1,S2}^{P(N)} &\triangleq \frac{v_{{\rm ctrl},p(m)}}{v_{\rm in}} = \frac{v_{{\rm out},S1}}{v_{\rm in}} \frac{v_{{\rm ctrl},p(m)}}{v_{{\rm out},S1}} \triangleq A_{S1} A_{S2}^{P(N)} \\ &= A_{S1} \frac{-r_{o2}^{P(N)} \left[g_{m2}^{P(N)} r_o^B + \left(g_{m2}^{P} + g_{m2}^{N}\right) r_{o2}^{N(P)'}\right]}{r_{o2}^{P'} + r_o^B + r_{o2}^{N'}}. \end{aligned} \tag{4}$$

The gains corresponding to (2)–(4) are obtained from simulation (dc sweep of $V_{\rm IN}$) and plotted in Fig. 2(c) versus output voltage for various $V_{\rm DZ}$ values. It can be seen that the OL gain decreases as $V_{\rm DZ}$ increases, mainly due to an ensuing gain drop in the second stage (cf. $A_{S1,S2}^{P}$ and $A_{S1,S2}^{N}$). The decrease in gain is, however, reasonably small (<2 dB for the 100-mV $V_{\rm DZ}$ variation considered), and the flatness of the gain curves is preserved such that the static linearity of the ringamp, which is defined by flatness of the OL gain versus output voltage characteristic, is not significantly affected [22].

B. Dynamic Properties

An important characteristic of the ringamp is its improved speed with respect to OTA-based multistage amplifiers, due to the absence of internal dominant poles. Indeed, in ringamps the dominant pole is located at the output and is defined by the load capacitance C_L:

$$f_{dp} = \frac{1}{2\pi\left(r_{o3}^{P} || r_{o3}^{N}\right) C_L}. \tag{5}$$

The value of f_{dp} is tightly linked to $V_{\rm DZ}$ through the impact of the latter on the resistance of the output stage devices [22]. The same holds true for the gain–BW (GBW) product, which depends on the transconductance of the output stage devices and is, thus, a function of variations in $V_{\rm DZ}$ [22]:

$$f_{\rm GBW} \approx \frac{1}{2\pi} A_{S1} A_{S2} \frac{g_{m3}^{P} + g_{m3}^{N}}{C_L}. \tag{6}$$

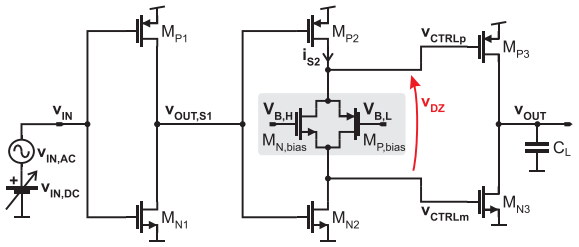
In order to illustrate these dependencies, Fig. 2(d) shows the ringamp frequency response at a large settled output voltage ($V_{\rm OUT} = 800$ mV) for varying $V_{\rm DZ}$. It can be seen that although the gain reduction for increasing $V_{\rm DZ}$ is not large, the corresponding reductions in BW and GBW are more pronounced, which have an important effect on the ringamp speed due to the resulting increase in phase margin (PM). This is readily seen in the transient response in unity-gain feedback shown in Fig. 2(e): despite exhibiting the same overshoot in all three cases, the settling behavior is progressively damped better for larger $V_{\rm DZ}$. Thus, despite the GBW of the ringamp actually *decreasing*, an *increase* of operating speed can be achieved for larger $V_{\rm DZ}$ due to the resulting increase in PM and the ensuing improved settling.

III. Proposed High-Linearity and High-BW Ringamp

Fig. 1 shows the ringamp introduced in this paper. It builds upon the baseline implementation discussed in Section II, with two key modifications, as discussed in what follows.

A. OL-Gain Flattening Through Dead-Zone Degeneration

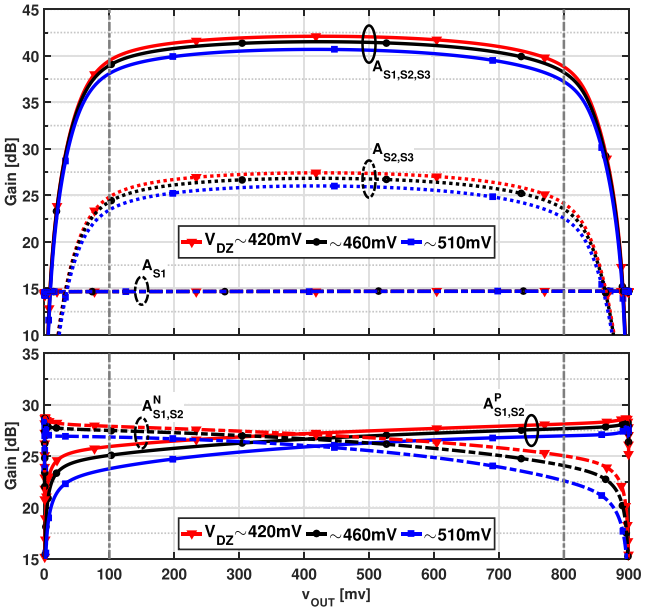
In order to maximize the linearity that can be recovered from a residue amplifier through first-order gain calibration, it is desirable to have an OL gain versus output voltage profile that is as flat as possible [22]. To this end, the proposed ringamp introduces the concept of DZD, which, as shown



(a)

	Stage 1		Stage 2		Stage 3	
$W_{M_{P(N)1}}$	16 µm		8 µm		8 µm	
$W_{M_{P(N),bias}}$	–		1.2 µm		–	
	$V_{OUT}=V_{CM}=450$ mV			$V_{OUT}=V_{OUT,max}=800$ mV		
V_{DZ}	∼430 mV	∼480 mV	∼530 mV	∼420 mV	∼460 mV	∼510 mV
$I_{DC,S1}$	1.65 mA	1.65 mA	1.65 mA	1.64 mA	1.64 mA	1.64 mA
$I_{DC,S2}$	507.8 µA	476.5 µA	441.1 µA	515.6 µA	483.1 µA	445.5 µA
$I_{DC,S3}$	38.8 µA	25 µA	15.1 µA	31.9 µA	21 µA	13.1 µA
I_{TOTAL}	2.2 mA	2.15 mA	2.11 mA	2.19 mA	2.15 mA	2.1 mA
$A_{OL,DC}$	42.1 dB	41.5 dB	40.7 dB	38.9 dB	38.3 dB	37.3 dB
GBW	9.1 GHz	6.6 GHz	4.3 GHz	7.7 GHz	5.5 GHz	3.4 GHz
PM	20.6°	32.2°	46.4°	27.6°	39.7°	53.7°

(b)



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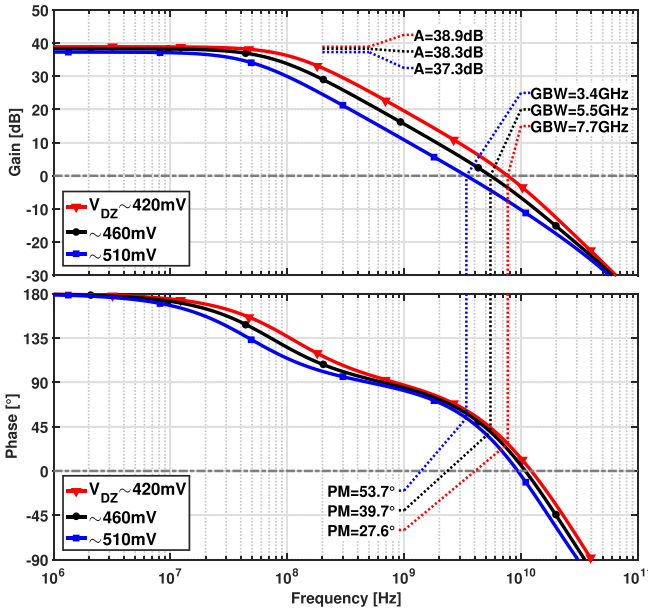
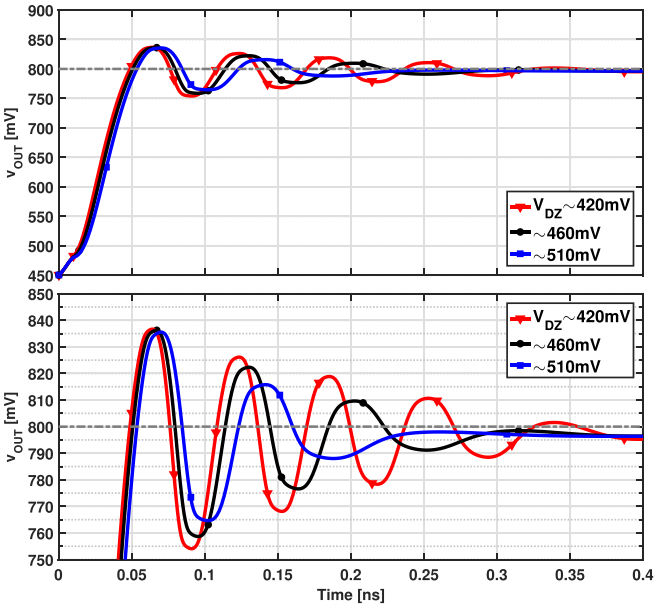


(d)



(e)

Fig. 2. Simulated performance of the baseline ringamp for varying DZ voltage ($V_{DZ} \approx \{420, 460, 510\}$ mV, $V_{DD} = 0.9$ V, and $C_L = 400$ fF). (a) Simulated circuit. (b) Design parameters and performance metrics. (c) OL gain (and its components) versus output voltage (from dc sweep). (d) OL gain versus frequency for $V_{OUT} = 0.8$ V (from ac sweep). (e) Transient response to a 350-mV step applied at $t = 0$ ns in unity-gain feedback configuration.

in Fig. 1, is implemented by two feedback devices $M_{N,DZD}$ and $M_{P,DZD}$ between the third and second stages. As we will show next, the operation of this technique can be explained in terms of large- and small-signal considerations.

1) Large-Signal Analysis: When the output voltage is close to mid-rail, the degeneration devices are off and the operation is the same as in the baseline ringamp. However, whenever the output departs toward the supply rails, the degeneration devices start to turn on, drawing a current i_{DEGEN} from the second stage. As a result, the current i_{DZ} flowing through the AP-CMOS arrangement is perturbed or *degenerated*, which modulates the DZ voltage and introduces an output-voltage-dependent offset $v_{DZD} = v_{DZD}(v_{OUT})$ into the ringamp. The sign of i_{DEGEN} is chosen so that the polarity of this offset will be opposite to the errors due to both finite gain and gain nonlinearity. Under these circumstances, the settled voltage at the input of the ringamp, when placed in feedback, can be expressed as

$$v_{IN} = v_{OUT}/A_1 + v_{NL}(v_{OUT}) - v_{DZD}(v_{OUT}) \tag{7}$$

where v_{IN} and v_{OUT} are the input and output voltages of the ringamp, A_1 is the linear term of the ringamp OL gain, $v_{NL}(v_{OUT})$ is the input-referred offset due to signal-dependent gain variation and $v_{DZD}(v_{OUT})$ is the intentionally created input-referred offset due to DZD. Clearly, when $v_{NL}(v_{OUT}) = v_{DZD}(v_{OUT})$, the two terms cancel out and the finite gain in the system becomes entirely first-order. Although such perfect cancellation is not practical to realize, when sized properly,

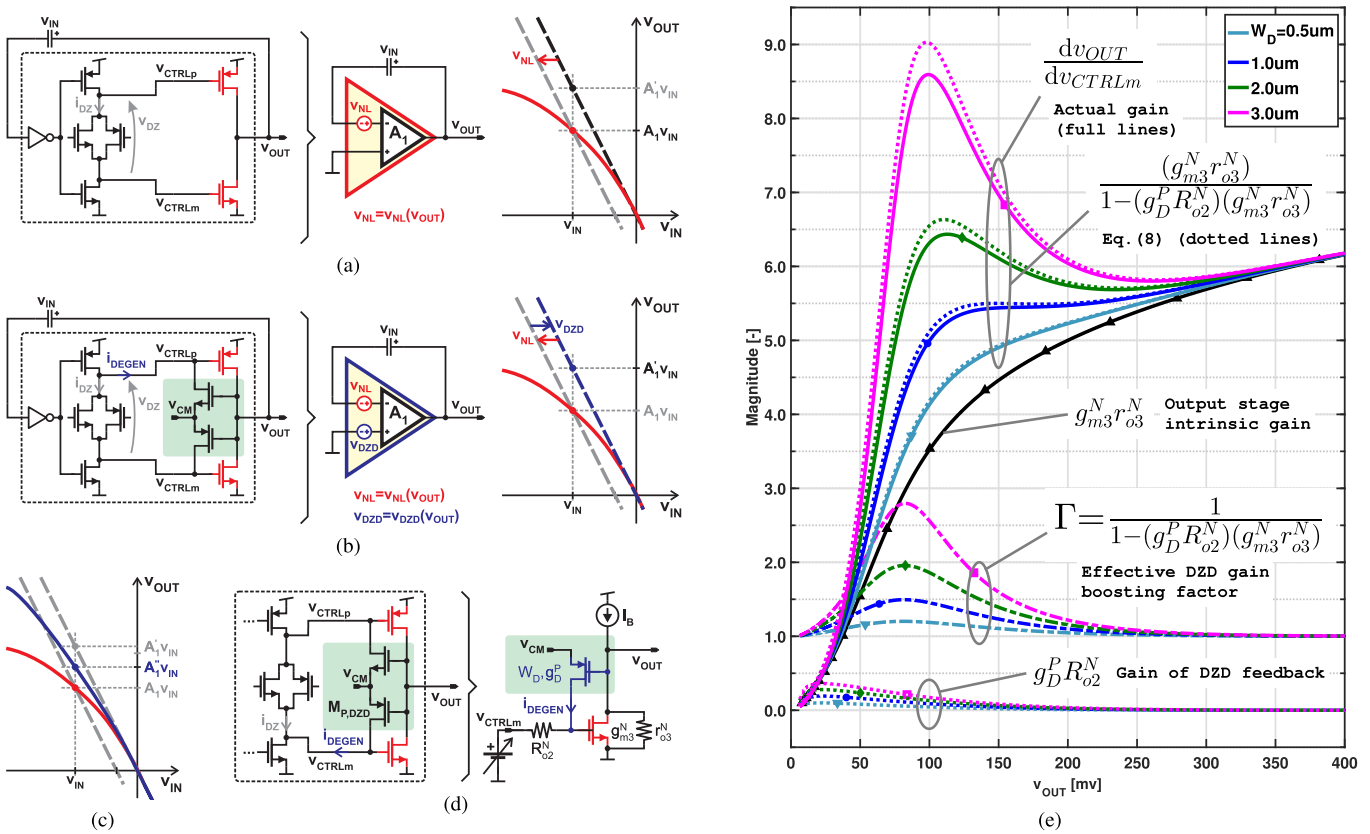


Fig. 3. Principle of DZD. (a) Nonlinear ringamp represented as a linear gain A_1 in series with a signal-dependent offset $v_{\rm NL}$. (b) Ideal linearization by DZD inducing a signal-dependent offset $v_{\rm DZD}$ to perfectly cancel $v_{\rm NL}$. (c) Practical linearization with $v_{\rm DZD}$ only partially cancelling $v_{\rm NL}$. (d) Circuit model for DZD analysis. (e) Simulated OL gain of the model (colored full lines) and prediction from (8) (colored dotted lines), along with the components of the latter.

the degeneration devices can be used to partially cancel the gain compression error in this manner, resulting in a much flatter OL gain versus output voltage characteristic that will yield an improved static linearity and wider output swing.

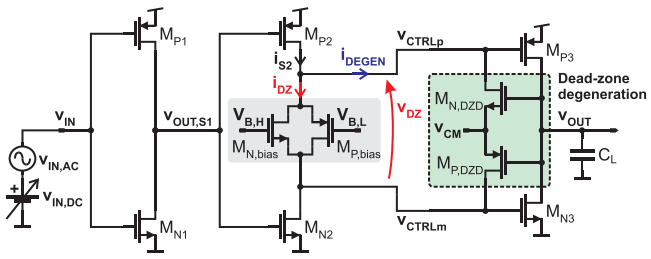
The foregoing discussion can be intuitively explained through a graphical representation. Fig. 3(a) shows the baseline ringamp and its representation as a linear gain A_1 in series with the signal-dependent offset $v_{\rm NL}$, along with a sketch of the OL input–output characteristic. As shown in the latter, the nonlinear gain (red) can be thought of as being generated by an ideally linear gain (black) that is shifted by the signal-dependent offset $v_{\rm NL}$. In Fig. 3(b), an ideal DZD is added to the ringamp, which introduces a signal-dependent compensation offset $v_{\rm DZD}$ that completely cancels the nonlinear-gain offset $v_{\rm NL}$ according to (7), thus yielding a perfectly linear gain characteristic (blue). Finally, Fig. 3(c) shows the input–output characteristic for the case of a practical DZD implementation: despite the offset cancellation not being perfect, the linearity of the compensated gain characteristic (blue) is significantly improved with respect to the baseline ringamp (red).

2) Small-Signal Analysis: To gain further insight into the DZD operation, a small-signal analysis can be performed. To this purpose, the bottom half of the proposed ringamp output stage is modeled using the circuit in Fig. 3(d), where R_{o2}^N represents the Thévenin resistance looking into the second-stage $v_{{\rm CTRL}m}$ node, the output PMOS device is replaced by an ideal current source I_B, and the degenerating device $M_{P,{\rm DZD}}$ of width W_D is modeled by its transconductance g_D^P. The gain and output resistance of this model are given by

$$\frac{v_{\rm OUT}}{v_{{\rm CTRL}m}} = \frac{-\left(g_{m3}^N r_{o3}^N\right)}{1-\left(g_D^P R_{o2}^N\right)\left(g_{m3}^N r_{o3}^N\right)} = -\Gamma\cdot\left(g_{m3}^N r_{o3}^N\right) \quad (8)$$

$$r_o = \frac{r_{o3}^N}{1-\left(g_D^P R_{o2}^N\right)\left(g_{m3}^N r_{o3}^N\right)} = \Gamma\cdot r_{o3}^N \quad (9)$$

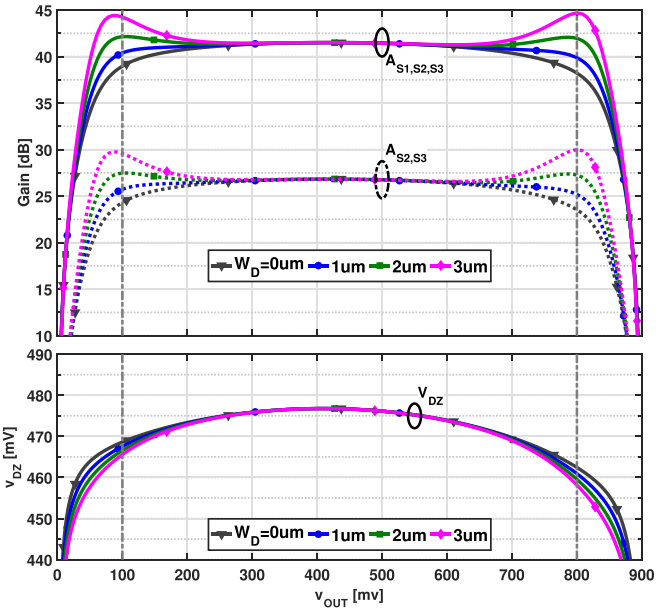
where $\Gamma \triangleq [1-(g_D^P R_{o2}^N)(g_{m3}^N r_{o3}^N)]^{-1}$ is a gain-boosting term resulting from the positive-feedback action of the degenerating device, whose magnitude changes as the output voltage moves closer to the supply rails as a result of the change in large-signal device biasing. This model is verified in Fig. 3(e), which shows the actual simulated gain ($\mathrm{d}v_{\rm OUT}/\mathrm{d}v_{{\rm CTRL}m}$) for parametric W_D and the values obtained from (8) (using the device parameters provided by the simulator at each dc bias point), along with the output stage intrinsic gain $g_{m3}^N r_{o3}^N$, the DZD feedback gain $g_D^P R_{o2}^N$, and the gain-boost factor Γ. Close to mid-rail (i.e., $v_{\rm OUT}\approx 400$ mV) $\Gamma\approx 1$ as g_D^P is null, but it increases as the output voltage approaches the supply rail, progressively turning on $M_{P,{\rm DZD}}$ and increasing g_D^P. Below the maximum boosting point, this feedback effect is outpowered by the reduction in the direct-gain term $g_{m3}^N r_{o3}^N$ for voltages too close to the rail. This model shows that with proper sizing of the DZD devices, the gain compression of the output stage close to the rails can be significantly counteracted, effectively extending the output swing. It should be noted that this extension stems from using the DZD-induced gain boost



(a)

$W_D = W_{M_{P(N),DZD}}$	–	1 µm	2 µm	3 µm
I_{DEGEN} @V_{OUTmax}	0 µA	∼8 µA	∼16 µA	∼24 µA
$I_{DC,S1}$ @V_{OUTmax}	1.64 mA	1.64 mA	1.64 mA	1.65 mA
$I_{DC,S2}$ @V_{OUTmax}	483.1 µA	488.3 µA	493.5 µA	498.7 µA
V_{DZ} @V_{OUTmax}	462.4 mV	460.9 mV	459.5 mV	458.1 mV
$I_{DC,S3}$ @V_{OUTmax}	21.0 µA	21.4 µA	21.7 µA	22.0 µA
I_{TOTAL} @V_{OUTmax}	2.15 mA	2.15 mA	2.16 mA	2.17 mA
$A_{OL,DC}$ @V_{OUTmax}	38.3 dB	39.9 dB	42 dB	44.7 dB
GBW @V_{OUTmax}	5.48 GHz	5.46 GHz	5.47 GHz	5.47 GHz
PM @V_{OUTmax}	39.7°	39.5°	39.1°	38.7°
ΔV_{OUT} @ −1 dB ΔA_{OL}	466 mV	632 mV	685 mV	544 mV
ΔA_{OL} @ 0.7 V ΔV_{OUT}	3.38 dB	1.63 dB	1.01 dB	3.38 dB

(b)



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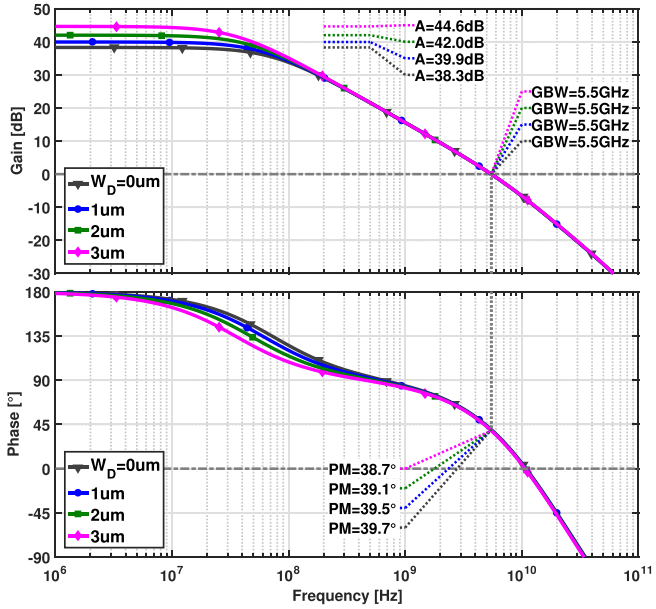

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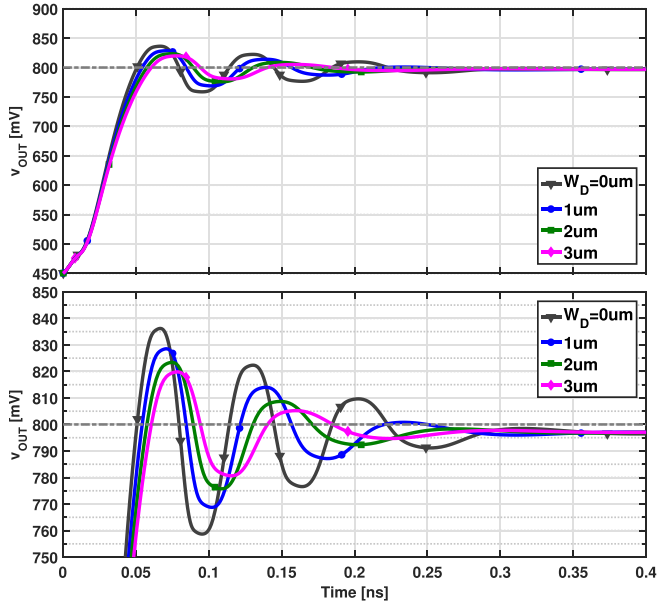


(e)

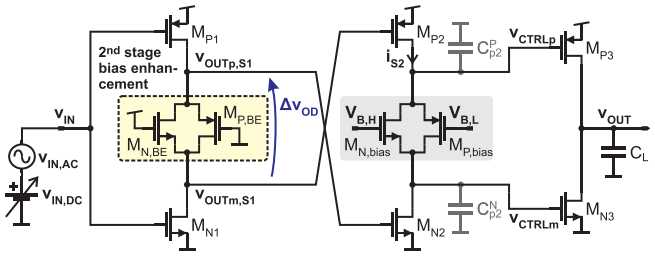
Fig. 4. Simulated performance of the baseline ringamp with DZD for varying degeneration devices width ($W_{M_{P(N),DZD}} \triangleq W_D = \{0, 1, 2, 3\}$ μm, $V_{DD} =$ 0.9 V, and $C_L = 400$ fF). (a) Simulated circuit. (b) Design parameters and performance metrics. (c) OL gain and DZ voltage versus output voltage (from dc sweep). (d) OL gain versus frequency for $V_{OUT} = 0.8$ V (from ac sweep). (e) Transient response to a 350-mV step in unity-gain feedback configuration.

to compensate the compression of the output stage close to the rails and does not rely on a specific cancellation condition of non-linear effects: as long as the amount of DZD is designed to be commensurate with the expected gain compression, the gain flatness can be improved.[2] Also, while this analysis successfully predicts the gain-boosting effect of DZD, the full operation mechanism of this technique is of large-signal nature and is not fully captured by the model in Fig. 3(d).[3]

After having discussed the basic principles behind the DZD operation, the full effects of this technique on the ringamp static and dynamic performance are now illustrated. To this purpose, the circuit in Fig. 4(a) is considered, where DZD is applied to the baseline ringamp. Fig. 4(c) shows the resulting OL gain versus output voltage characteristics for variable W_D, along with the associated DZ voltage evolutions. As expected, the effect of DZD on the static ringamp characteristic is a gain boost for output values close to the supply rails, which translates to a partial cancellation of gain compression and an extension of the OL gain flatness of the ringamp. This is accounted for by a modified $A_{S2,S3}$ gain term $A_{S2,S3}^{DZD}$, given by (10), in which the effect of DZD manifests again as an additional subtractive term in the denominator [cf. (3) and (8)].

[2]Naturally, the amount of improvement will be dependent on the relative variations of these effects across PVT, as shown in Section III-D.

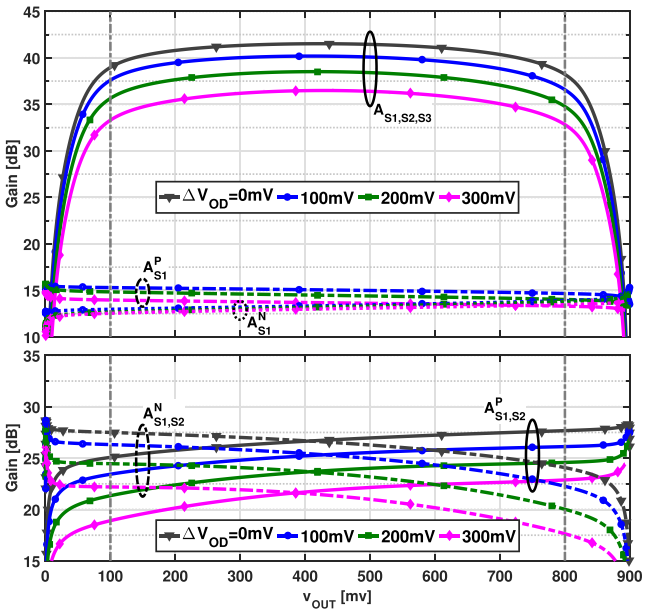
[3]Note that this model does not account for variations in the DZ voltage that result from the AP-CMOS current starvation caused by i_{DEGEN}, and that the operating point is recomputed at each point in the curves of Fig. 3(e).



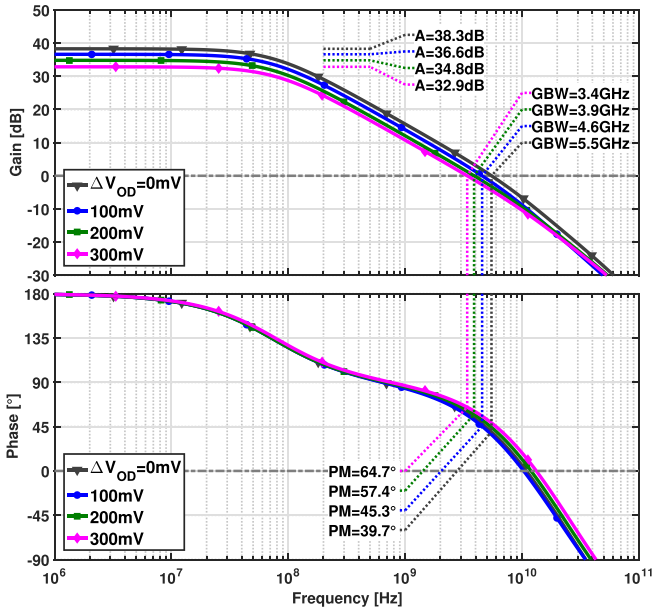
(a)

$W_{M_{P(N),BE}}$ / ΔV_{OD}	– / 0 mV	15 µm / ∼100 mV	6 µm / ∼200 mV	3 µm / ∼300 mV
$I_{DC,S1}@V_{OUTmax}$	1.64 mA	1.5 mA	1.36 mA	1.22 mA
$I_{DC,S2}@V_{OUTmax}$	483.1 µA	796 µA	1.2 mA	1.6 mA
$V_{DZ}@V_{OUTmax}$	462.4 mV	463.2 mV	463.9 mV	455.3 mV
$I_{DC,S3}@V_{OUTmax}$	21 µA	20.8 µA	20.7 µA	22.4 µA
$I_{TOTAL}@V_{OUTmax}$	2.15 mA	2.32 mA	2.54 mA	2.86 mA
$A_{OL,DC}@V_{OUTmax}$	38.3 dB	36.6 dB	34.8 dB	32.9 dB
GBW @ V_{OUTmax}	5.48 GHz	4.55 GHz	3.89 GHz	3.39 GHz
PM @ V_{OUTmax}	**39.7°**	**45.3°**	**57.4°**	**64.7°**
ΔV_{OUT} @ −1 dB ΔA_{OL}	466 mV	415 mV	421 mV	430 mV
ΔA_{OL} @ 0.7 V ΔV_{OUT}	3.38 dB	3.80 dB	3.71 dB	3.68 dB

(b)



(c)



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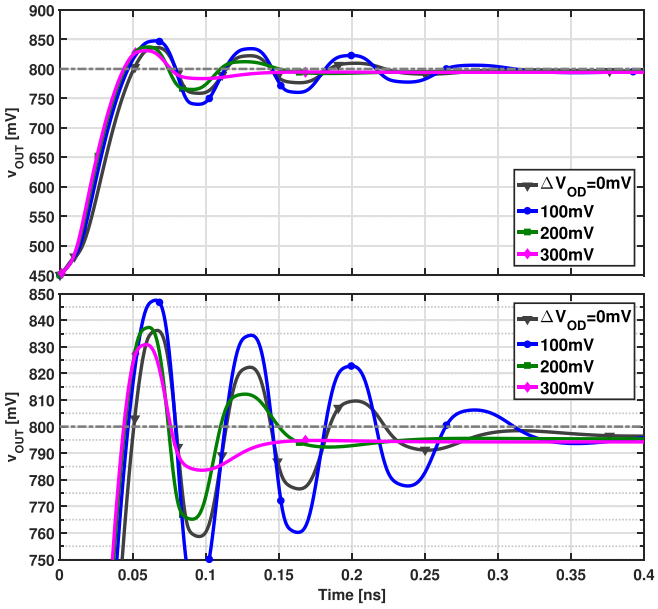


(e)

Fig. 5. Simulated performance of the baseline ringamp with bias enhancement for varying second-stage overdrive voltage ($\Delta V_{OD} = \{0, 100, 200, 300\}$ mV, $V_{DD} = 0.9$ V, and $C_L = 400$ fF). (a) Simulated circuit. (b) Design parameters and performance metrics. (c) OL gain (and its components) versus output voltage (from dc sweep). (d) OL gain versus frequency for $V_{OUT} = 0.8$ V (from ac sweep). (e) Transient response to a 350-mV step in unity-gain feedback.

The effects of DZD on the dynamic ringamp behavior are illustrated in Fig. 4(d), which shows the frequency response for several W_D values ($V_{OUT} = 800$ mV). While the gain-boosting effect is clearly seen in this figure, a more important DZD consequence becomes apparent, namely, the decrease in dominant pole frequency that follows from (5) and the DZD-induced boost in output impedance (9). Moreover, it can be seen that DZD has a negligible impact on the GBW of the ringamp, as the boosting in gain and the reduction in BW cancel out, leaving the PM unaffected. This is supported by the step response results shown in Fig. 4(e), where the different traces present similar settling behavior and differ mainly due to the different overshoot values that need to be settled.

B. Settling Improvement Through Second-Stage Bias Enhancement

Within the context of pipelined ADCs, the maximum operating frequency is often limited by incomplete settling errors

$$A_{S2,S3}^{DZD} = \frac{\left(g_{m2}^{P}+g_{m2}^{N}\right)\left(g_{m3}^{P'}+g_{m3}^{N'}\right)+g_{m3}^{P}g_{m2}^{P}\frac{r_o^B}{r_{o2}^N}+g_{m3}^{N}g_{m2}^{N}\frac{r_o^B}{r_{o2}^P}}{\frac{r_{o2}^{P'}+r_o^B+r_{o2}^{P'}}{r_{o2}^P\cdot r_{o2}^N\cdot r_{o3}}-\left[g_{m3}^{P}g_D^{N}\frac{r_o^B}{r_{o2}^N}+g_{m3}^{N}g_D^{P}\frac{r_o^B}{r_{o2}^P}+\left(g_D^{P}+g_D^{N}\right)\left(g_{m3}^{P'}+g_{m3}^{N'}\right)\right]} \tag{10}$$

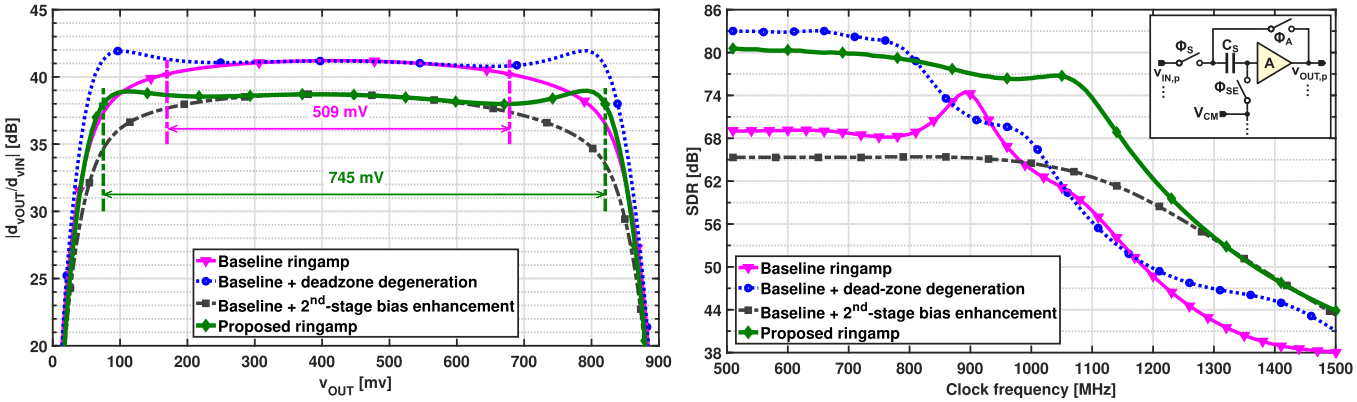


Fig. 6. Proposed ringamp simulated performance. (a) OL gain versus output voltage, compared with the baseline ringamp and with the effects of DZD and bias enhancement separately ($V_{\rm DZ} \approx 480$ mV, $V_{\rm DD} = 0.9$ V, and $C_L = 400$ fF). (b) Linearity versus clock frequency for an UGSHA using the ringamps in (a).

of the residue amplifiers. For the particular case of ringamps, this speed limitation can be improved by boosting the overdrive of the second stage, as was independently discovered in [24]. The improvement in speed comes through a deliberate *decrease* of the ringamp GBW, which, along with an increase in the nondominant poles at the second-stage output, yields an increased PM and thus reduced settling time. As shown in Fig. 5(a), in the proposed implementation this is done by adding an additional AP-CMOS arrangement in the first stage to create a voltage drop $\Delta_{V_{\rm OD}}$ that is used to drive the second stage with higher v_{GS} and thus higher overdrive,[4] which has a twofold effect. First, the increase in overdrive decreases the resistance r_{o2}^{j} of the second-stage devices, pushing the first nondominant pole of the ringamp to higher values following

$$f_{ndp} \approx \frac{1}{2\pi \left(r_{o2}^{P} || r_{o2}^{N}\right)\left(C_{p2}^{P} + C_{p2}^{N}\right)}. \tag{11}$$

Second, the increased overdrive significantly reduces the gain of the second stage, which can be intuitively explained by recalling that during the stabilization and settling phases of the ringamp transient response these devices operate in strong inversion [22] and, therefore, their intrinsic gain is inversely proportional to their overdrives voltages $v_{{\rm OD},M_{j2}}$ [25]:

$$A_{M_{j2}} \triangleq g_{m2}^{j} r_{o2}^{j} \propto \frac{1}{v_{{\rm OD},Mj2}}, \quad j = \{\rm P, N\}. \tag{12}$$

Assuming that the second stage is resized to maintain a constant DZ voltage despite the increase in overdrive,[5] neither the gain nor the resistance of the third-stage devices will be affected by the bias enhancement, so the position of the dominant pole (5) remains constant while the overall gain (1) decreases, thus yielding a reduction in GBW. Together with the increase in nondominant pole frequency (11), this reduction in GBW results in a larger PM and, therefore, a reduced settling time.

The aforementioned effects are confirmed by the simulation results reported in Fig. 5, which shows the static and dynamic behavior of the baseline ringamp with second-stage bias enhancement, for variable $\Delta_{V_{\rm OD}}$. In particular, the OL gain reduction is readily visible in Fig. 5(c), which also confirms that the dominant gain degradation occurs in the second stage, although a gain decrease in the first stage is also observed, as expected from the $V_{\rm DS}$ reduction incurred in this stage. Most importantly, the drop in gain is approximately constant across output voltage (i.e., the flatness of the gain is preserved), and as a result a negligible linearity degradation will be incurred when using this technique in a pipeline residue amplifier, if first-order gain calibration is considered [22]. Likewise, the frequency response in Fig. 5(d) confirms both the progressive reduction in GBW and the increase in nondominant pole frequency for increasing $\Delta_{V_{\rm OD}}$ along with the ensuing improvement in PM. Finally, Fig. 5(e) shows how the effects of second-stage bias enhancement translate in the time domain into a progressively improved settling behavior as $\Delta_{V_{\rm OD}}$ is increased, demonstrating the effectiveness of this technique for improving the ringamp speed through the minimization of its settling time.

C. Combined Effects of DZD and Second-Stage Bias Enhancement

In order to simultaneously achieve high speed and linearity, the two previously described techniques are exploited by the ringamp introduced in this paper. This is possible due to the minimal interaction between their operating mechanisms, as portrayed by the simulation results in Fig. 6.

The static effects of applying these techniques are summarized in Fig. 6(a), which shows the simulated OL gain versus output voltage profiles that result when using them separately and in combination. It can be observed that the use of DZD allows the 1-dB gain compression range to be extended by about 230 mV, despite an overall degradation of about 2 dB

[4]In a nutshell, the same idea of generating a voltage drop in the second stage to under-drive the third stage and enforce stability is used now in the first stage, through a wire cross-connection, to over-drive the second stage and improve settling.

[5]This can be accomplished in two ways. One option is to keep the gain devices M_{j2} unmodified and resize the AP-CMOS arrangement to reduce its resistance, which is the approach followed here. Alternatively, one can keep the AP-CMOS unmodified and reduce the sizes of the M_{j2} gain devices, which also results in an increased nondominant pole frequency due to the reduction in parasitics at the second-stage outputs. Moreover, the first-stage load is lower in this latter case, which allows the use of smaller devices in this stage and thus to reduce power consumption.

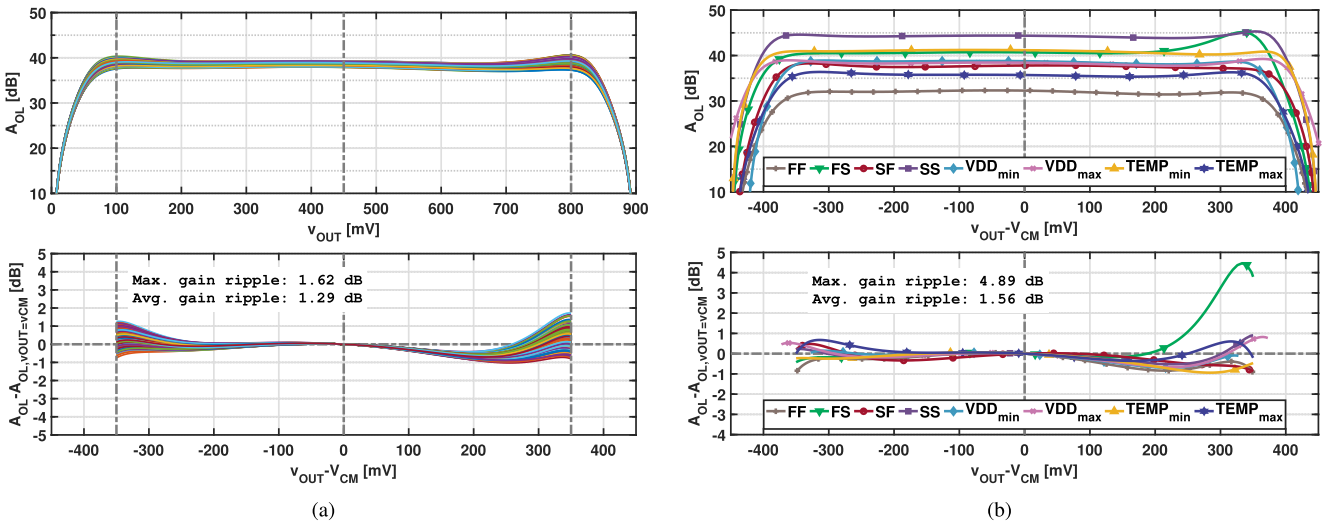


Fig. 7. Simulated raw (top) and normalized (bottom) OL gain versus output voltage considering (a) random process mismatch around the TT corner (1000 Monte Carlo points) and (b) eight PVT corners (four process corners: FF, FS, SF, SS; four environmental corners: $T = \{-40, 85\}$ °C, $V_{\mathrm{DD}} = \{0.855, 0.945\}$ V around TT). The bottom traces are normalized with respect to the gain values for $v_{\mathrm{OUT}} = V_{\mathrm{CM}}$ and drawn within an output swing extending 100 mV from the supply rails.

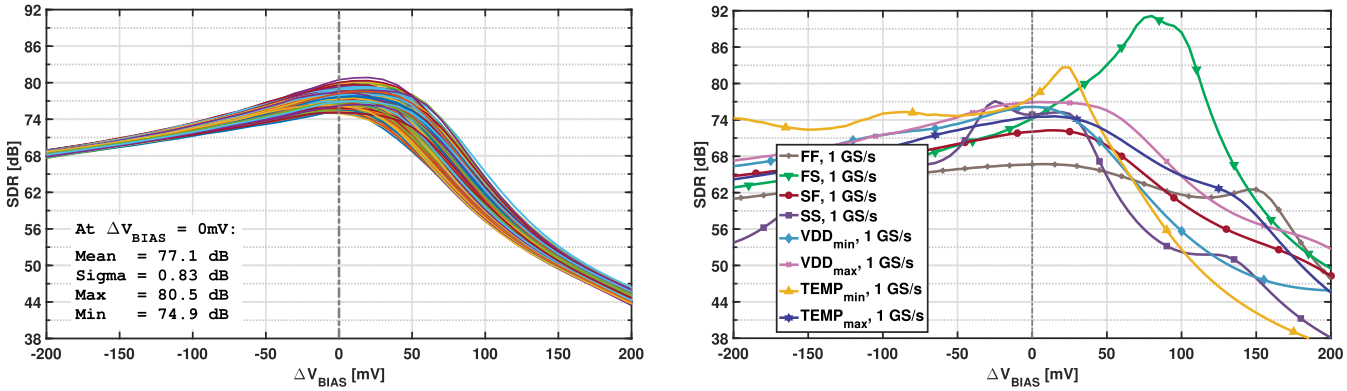
due to the second-stage bias enhancement. As previously pointed out, this degradation is essentially constant across output voltage, and the gain profile with second-stage bias enhancement exhibits the same 1-dB compression behavior as the baseline ringamp. Fig. 6(a) further confirms that this is also true if bias enhancement is applied to a ringamp with DZD, as is the case in this paper.

The dynamic effects of the aforementioned techniques are further illustrated in Fig. 6(b), where the ringamp is simulated in an ideal unity-gain sample-and-hold amplifier (UGSHA), and the output signal-to-distortion ratio (SDR) is analyzed with respect to clock frequency [22]. It can be seen that although DZD has little effect on speed, it significantly improves linearity, resulting in an SDR boost of more than 14 dB that rolls off at high frequencies due to incomplete settling, similar to the baseline case. The effects of second-stage bias enhancement are also apparent in this figure, which shows how the peak linearity with second-stage bias enhancement is extended to higher frequencies, despite a degradation in raw SDR value. When using both techniques, the 2.5-dB loss in SDR due to bias enhancement subtracts from the 14-dB boost due to DZD, resulting in a net linearity improvement of 11.5 dB, while at the same time improving speed significantly. These results demonstrate how the combined use of these techniques allows the proposed ringamp to achieve greater than 12-bit (74-dB) linearity and beyond 1 GS/s in 28-nm CMOS. Considering that this process is one of the most challenging technologies for achieving high gain and linearity due to the poor intrinsic gain achievable with respect to other planar CMOS and FinFET nodes ([26], [27]) and its low supply voltage, this demonstrates the capability of ringamps to cover a broad range of design targets for speed and linearity in any nanoscale technology.

D. Effect of Process and Environment Variations

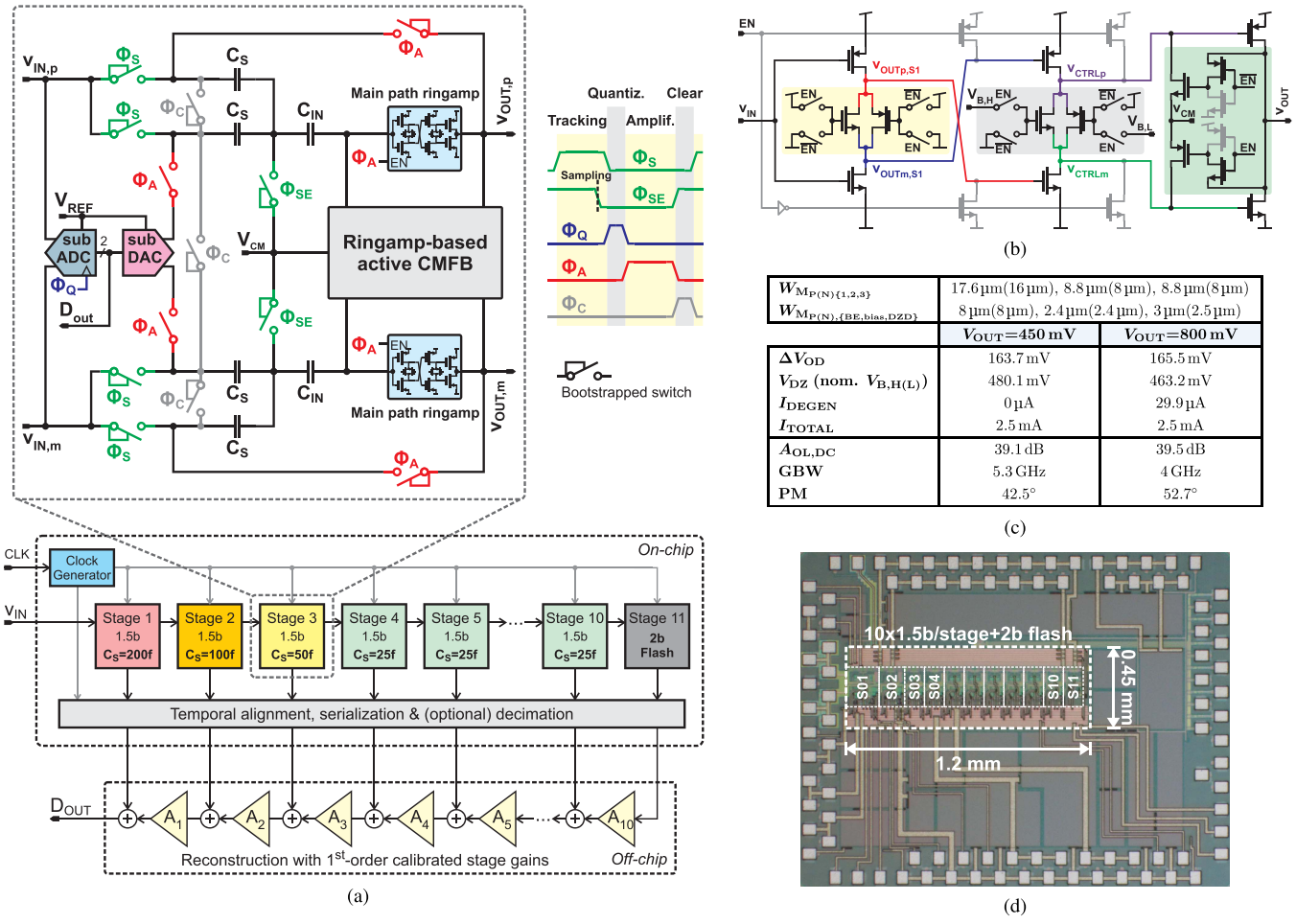
To assess the robustness of the described techniques against process and environment variations, the operation of the proposed ringamp was simulated considering: 1) random process mismatch around the typical-typical (TT) corner (1000 Monte Carlo points) and 2) eight PVT corners (four process corners: FF, FS, SF, SS; and four environmental corners: $T = \{-40, 85\}$ °C, $V_{\mathrm{DD}} = \{0.855, 0.945\}$ V around TT). Fig. 7(a) and (b) shows the effects of the aforementioned mismatch and PVT variations on the OL gain characteristic, respectively, including zoomed-in versions normalized to the gain values at mid-rail (i.e., $A_{\mathrm{OL}} - A_{\mathrm{OL}}|_{v_{\mathrm{OUT}}=V_{\mathrm{CM}}}$) and considering a swing 100 mV away from the supplies. It can be seen that the worst case gain ripple is below 2 dB across mismatch but rises up to 5 dB across corners, although in all but one corner it remains below 2 dB. The smaller amount of variation with respect to mismatch is expected, considering that neither the bias enhancement nor the DZD relies on accurate matching between devices. On the other hand, the strength of the effects introduced by these techniques (overdrive increase and gain boosting, respectively) does depend on the absolute values of threshold voltages, thus causing their increased PVT sensitivity. For example, the gain peaking seen in Fig. 7(b) for outputs close to V_{DD} in the FS corner is caused by the DZD being too strong and turning on "too early" due to the decreased value of the threshold voltage of the degenerating device $M_{N,\mathrm{DZD}}$ in this corner.

The effects of mismatch and PVT variations on the dynamic operation of the ringamp are illustrated in Fig. 8(a) and (b), respectively, which show the linearity in UGSHA configuration at 1 GS/s considering the same mismatch and PVT scenarios of Fig. 7(a) and (b). The independent variable in these plots is the deviation ΔV_{BIAS} of the ringamp bias voltages from the supply rails [i.e., $V_{B,L} = V_{\mathrm{SS}} + \Delta V_{\mathrm{BIAS}}$, $V_{B,H} = V_{\mathrm{DD}} - \Delta V_{\mathrm{BIAS}}$ in Fig. 2(a)], which can be used to tune the ringamp gain and settling properties [22]. For $\Delta V_{\mathrm{BIAS}} \sim 0$ V, the linearity stays above 12 bit (74 dB) across mismatch and above 10 bit (62 dB) across corners, although in all but one corner it remains above 11 bit (68 dB).



(a) (b)

Fig. 8. Simulated linearity versus ringamp bias voltages offset in an UGSHA configuration at 1 GS/s considering (a) process mismatch around the TT corner (1000 points) and (b) eight PVT corners (four process corners: FF, FS, SF, SS; four environmental corners: $T = \{-40, 85\}$ °C, $V_{DD} = \{0.855, 0.945\}$ V).



(a)

(b)

$W_{M_{P(N)\{1,2,3\}}}$	17.6µm(16µm), 8.8µm(8µm), 8.8µm(8µm)	
$W_{M_{P(N),\{BE,bias,DZD\}}}$	8µm(8µm), 2.4µm(2.4µm), 3µm(2.5µm)	
	V_{OUT}=450 mV	V_{OUT}=800 mV
ΔV_{OD}	163.7 mV	165.5 mV
V_{DZ} (nom. $V_{B,H(L)}$)	480.1 mV	463.2 mV
I_{DEGEN}	0 µA	29.9 µA
I_{TOTAL}	2.5 mA	2.5 mA
$A_{OL,DC}$	39.1 dB	39.5 dB
GBW	5.3 GHz	4 GHz
PM	42.5°	52.7°

(c)

(d)

Fig. 9. ADC implementation details. (a) Architecture and off-chip digital reconstruction (bottom) and structure of each 1.5-bit stage (top). (b) Detailed schematic of the signal ringamps along with (c) its relevant design parameters and performance metrics. (d) Full chip microphotograph.

Again, the increased variability across corners is explained by the dependence of the proposed techniques on the absolute values of the threshold voltages. For instance, the decreased linearity, shown in Fig. 8(b) for the FF corner, is a consequence of the larger overdrives seen by all the devices in this corner causing higher currents in the first and second stages, resulting in overdamped settling due to the increase in V_{DZ}.

The techniques leveraged by the proposed ringamp could be made tunable with a few modifications to allow the use of calibration. In particular, the DZD strength could be tuned by controlling the width of the degeneration devices or by

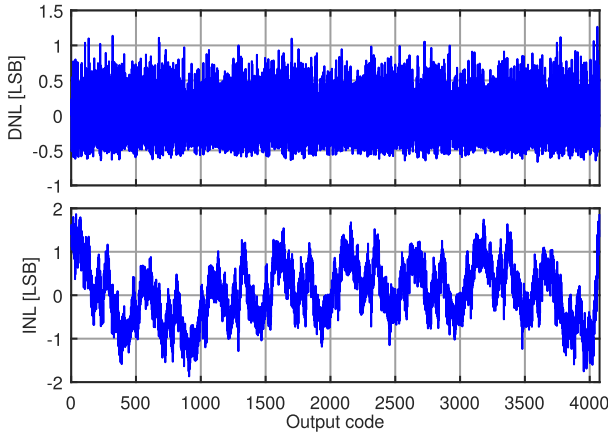


Fig. 10. Differential and integral non-linearities (code histogram method, $F_{\text{clock}} = 100$ MHz, $F_{\text{signal}} = 1$ MHz, 12-bit quantization).

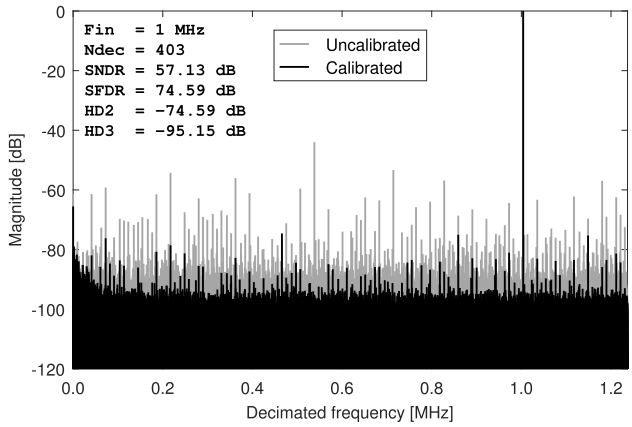


Fig. 11. Measured output spectrum for a 1-MHz full-scale input at 1 GS/s (decimation factor = 403, 32 kpoints FFT).

introducing voltage offsets at their gates to control their effective threshold (as done in the second stage of the original ringamp in [16]). Similarly, the second-stage overdrive ΔV_{OD} could be tuned by controlling the gate voltages of the bias-enhancement devices. These modifications, however, lie outside the scope of this paper and are not investigated any further.

IV. ADC Implementation

A pipelined ADC was implemented to verify the effectiveness of the proposed ringamp techniques. Moreover, in order to make a straightforward comparative assessment of the BW and linearity improvements introduced by their usage, the same pipeline architecture used in [22] to characterize the baseline ringamp performance was employed here as well, which is shown in Fig. 9(a). It is a pipeline composed of ten 1.5-bit stages followed by a 2-bit back-end flash. The stages are scaled down three times by a factor of 2 to save power, and the digital reconstruction and gain calibration are implemented off-chip using the procedure described in [22]. The structure of each stage is also shown in Fig. 9(a); it is based on the flip-around MDAC with ringamp-based CMFB described in [22], where only the signal ringamps were replaced and the rest

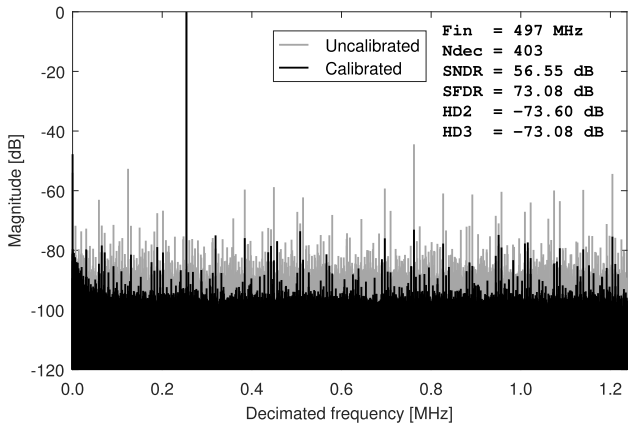


Fig. 12. Measured output spectrum for a 497-MHz full-scale input at 1 GS/s (decimation factor = 403, 32 kpoints FFT).

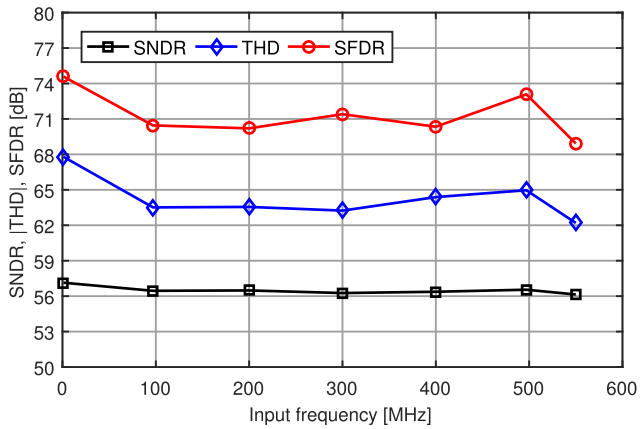


Fig. 13. Measured performance at 1 GS/s for variable input signal frequency (full-scale input amplitude, decimation factor = 403, 32 kpoints FFTs).

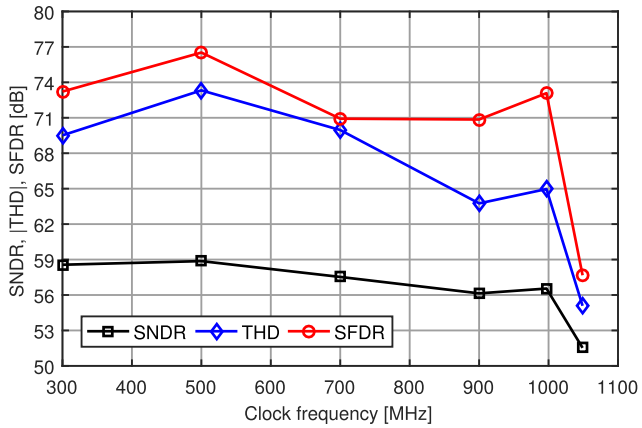


Fig. 14. Measured performance for variable clock frequency and Nyquist input (full-scale input amplitude, decimation factor = 403, 32 kpoints FFTs).

of the circuitry was left as-is (including the charge-transfer-based mechanism for programming the capacitors C_{IN} and compensating the dc offset). The ringamp noise accounts for 20% of the total stage noise, and kT/C noise for the rest.

The actual implementation of the proposed ring amplifier used in the signal path is shown in Fig. 9(b). The CMOS

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART SINGLE-CHANNEL ADCS ($ENOB_{HF} \geq 9$ BIT, $F_s \geq 400$ MS/s) [13]

		This work	[21] Lagos	[28] Moon	[2] Shibata	[7] Ali	[5] El-Chammas	[6] Ali
Architecture Residue amplifier		**Pipelined** **Ringamp**	Pipelined Ringamp	Pipelined SAR Gm cell	CT Pipelined Opamp	Pipelined Opamp	Pipelined Opamp	Pipelined Opamp
Resolution [b]		**12**	12	10	–	14	14	14
Technology [m]		**28n**	28n	28n	28n	28n	180n	65n
Supplies [V]		**0.9**	0.9	1.0	1.8/±1.0	2.5/1.8/0.9	3.3/1.8	3.3/2.5/1.2
Input range [$V_{pp,d}$]		**1.6**	1.6	–	2.0	–	2.5	2.0
Sampling rate [Hz]		**1G**	600M	500M	9G	2.5G	500M	1G
ERBW [Hz]		**>500M**	400M	–	1.125G	1.5G	700M	1G
ENOB [b]	LF in.	**9.2**	9.4	9.1	–	10.3	10.5	11.2
	Nyquist	**9.1**	9.1	9.1	10.7	10	10.3	11
SNDR [dB]	LF in.	**57.1**	58.1	56.7	–	64	64.8	69
	Nyquist	**56.6**	56.3	56.6	66	61.7	64	68
SFDR [dBc]	LF in.	**74.6**	67.5	73	79	80	93	86
	Nyquist	**73.1**	69.2	69.2	79	73	82	82
Power [W]		**24.8m**¶	14.2m¶	6m	2330m	1150m*	550m*	1200m*
FoM_W [J/c.-step]		**45f**	44.3f	22f	715f	463f	849f	585f
FoM_S [dB]		**159.6**	159.5	162.8	152.3	152.1	150.6	154.2
Area [mm^2]		**0.54**†	0.62†	0.015†	5.1†	14.4‡	2.5†	18§
Gain calibration		**1st-order, off-chip**	1st-order, off-chip	1st-order, on-chip	>1st-order on-chip	1st-order, on-chip	No	1st-order, on-chip

¶ Does not include gain calibration (performed off-chip). * Design includes a buffer for the input signal.
† Core area. ‡ Full chip area. § Core area, including on-chip digital calibration circuitry.

devices implementing the DZD and the second-stage bias enhancement are gated so that the full ringamp can be easily powered down, providing a signal-independent idle state when the ringamp is not used. The most relevant design parameters and performance metrics of the ringamp used in the first stage of the pipeline are reported in Fig. 9(c). In order to maximize overdrives and slewing power and to minimize parasitics, all the transistors are ultralow-threshold devices with minimum channel length. This first-stage ringamp achieves 39 dB of OL gain while drawing 2.5 mA from a single 0.9-V supply.

The ADC was fabricated in a 1P10M 28-nm CMOS process, occupying a core active area of 1.2 mm × 0.45 mm. A photograph of the chip is shown in Fig. 9(d). The die is pad-limited, and the area between the ADC core and the pad ring was filled with decoupling capacitance, as no on-chip buffers were included.

V. MEASUREMENT RESULTS

The performance of the implemented prototype was measured using the procedures reported in [22] for the determination of the stage reconstruction gains and the ringamp bias voltages. The pseudo-static linearity measured at 1 MS/s is shown in Fig. 10. The achieved DNL and INL (12-bit quantization) are 1.27 and 1.87 LSB, respectively.

Figs. 11 and 12 show the measured decimated spectrums at 1 GS/s with low- and close-to-Nyquist frequency inputs, respectively. To maximize SNDR and demonstrate the rail-to-rail operation of the ringamp, a 1.6-$V_{pp,d}$ input was used, utilizing 89% of the available supply range for residue processing. The effectiveness of the ringamp gain linearization is apparent from these figures, where an SFDR in excess of 70 dB is achieved after a simple first-order stage gain calibration.

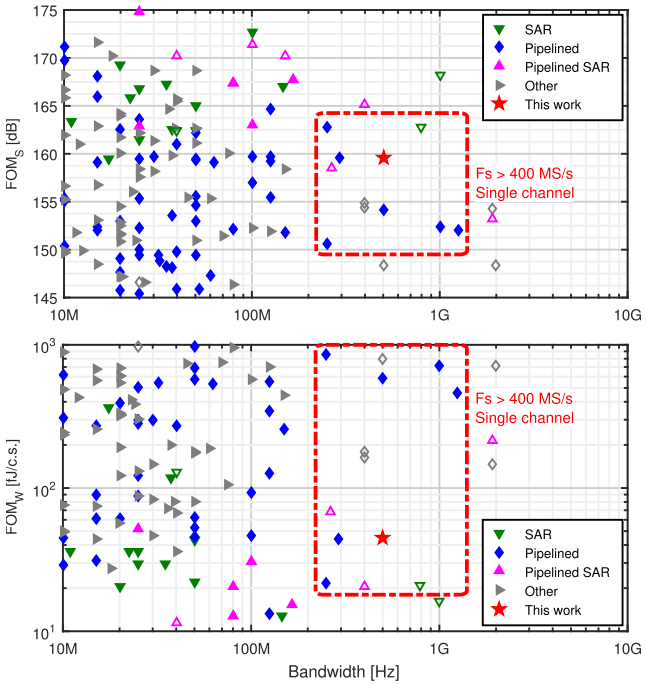


Fig. 15. Schreier (top) and Walden (bottom) FoM comparison with the ADCs published at ISSCC and VLSI conferences from 1997 to 2018 ($ENOB_{HF} \geq$ 9 bit) [13]. Unfilled symbols: implementations using time interleaving.

The measured dynamic behavior with respect to input signal and clock frequencies is reported in Figs. 13 and 14, respectively. The ADC exhibits greater than 500-MHz ERBW and operates up to 1 GS/s, after which the performance degrades due to incomplete settling. SFDR levels above 70 dB are maintained throughout these ranges, demonstrating the effectiveness of the DZD and second-stage bias enhancement for simultaneously achieving high linearity and BW.

At 1 GS/s, the ADC consumes 24.8 mW operating entirely on a 0.9-V supply, which translates into Schreier and Walden figure-of-merits (FoMs) of 159.6 dB and 45 fJ/conv.-step, respectively. Table I summarizes the measured performance and compares it against other high-performance single-channel ADCs. As illustrated by the FoM plots in Fig. 15, this work constitutes not only the highest-speed ringamp-based ADC reported to date but also the most power efficient implementation among all single-channel ADCs of any architecture with at least 800 MS/s and greater than 9 ENOB, demonstrating the potential for extending this work to achieve power-efficient, multi-GS/s implementations through the use of time interleaving.

VI. Conclusion

The effectiveness of a new ringamp architecture that exploits DZD and second-stage bias enhancement for simultaneously achieving high linearity and BW with high power efficiency has been demonstrated. These two techniques can be combined with little interdependence effects to either improve linearity or BW. A combination of both allowed the implemented design to push the power-efficiency state of the art for high-performance, single-channel ADCs.

Acknowledgment

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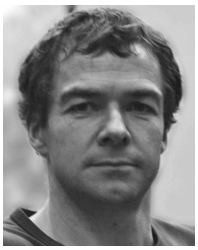

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